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Chapter 1

Introduction

This service module describes the Z-160 Base Unit. Each subassembly installed in the base unit is divided into its own service module. Each module contains its own table of contents, and is complete within itself. For example, if you wish to configure the CPU card, you would refer to the *System CPU Card Service Module*.

Service Equipment Required

The following information is provided for proper servicing of the Z-160 Portable Personal Computer. Use the recommended model numbers or equivalent substitutes.

Test Equipment

- **Oscilloscope**—DC to 100 MHz, dual trace, triggered sweep.
- **Logic Probe**—DC to 20 MHz. Capable of detecting 10 ns single pulses, and indicating logic one, logic zeroes, and high impedance states. Heath Model IT-7410.
- **Digital Voltmeter**—High impedance input, 0 to 1000 volts, 0 to 1 megohm. Heath Model SM-2215.
- **Variable Power Supply**—0 to 120 VAC RMS, 3 amperes.
- **Low Capacitance Oscilloscope Probe**—Input capacitance adjustable from 15 pF to 50 pF, 4 ns rise time. Heath Model PKW-105.
- **Video Monitor**—RGB color and monochrome composite wide band monitor. Zenith Model ZVM-135.

Tools

The following hand tools or equivalent are required for servicing:

- Long-nose pliers
- Diagonal cutters
- 1/4" blade slotted screwdriver
- #1 Phillips screwdriver
- #2 Phillips screwdriver
- Set of nut drivers
- Desoldering bulb
- Soldering iron, Heath Model GH-17A
- IC puller, Heath Part Numbers HE 490-111 and HE 490-189

Miscellaneous Supplies

- Solder, 60/40, Heath Part Number HE 331-13
- Desoldering braid, Heath Part Number HE 490-185
- Lint-free cloth

Chapter 2

Installation and Configuration

This chapter provides information for installation of the Z-160 Portable Personal Computer. There is no configuration required for the base unit. Refer to the appropriate service module to configure the power supply, disk drives, and cards.

Operating Environment

The operating environment for the computer should not exceed the temperature and operating limits of −4° to 140° F (−20° to 60° C) and 10% to 80% relative humidity.

Installation

Place the computer on a sturdy table or desk, near a grounded power receptacle. If an extension cord must be used, be sure it is rated for a minimum of 15 amps. It is important that the air and fan vents are clear of obstructions which could inhibit proper air flow. Refer to Figure 2.1 for the vent locations.

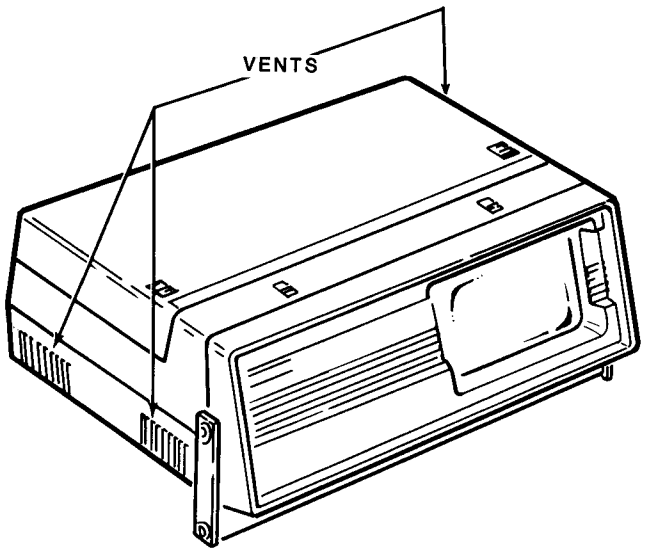

Figure 2.1. Z-160 Vent Locations

Rear Chassis Plugs and Connectors

Refer to Figure 2.2 and connect the appropriate plugs and connectors listed below. In addition to the plugs and connectors listed, there are four positions provided for optional cards. Refer to the appropriate service module for more detailed information.

Power Supply

WARNING: Be sure the power supply switch is in the OFF position.

- Plug the computer line cord into the power supply receptacle.

Floppy Disk Controller Card

- Serial connector DTE #1 (the upper of the two connectors) provides the necessary RS-232 signals for connection to a serial printer or other device.

- Optional serial connector DTE #2 (the lower of the two connectors) provides the necessary RS-232 signals for connection to a serial printer or other device. It is most commonly used for serial communication.

Video/Color/Composite Card

- A phono jack connector provides the composite monochrome output signals for a video monitor.

- A DB-9 "D" connector provides the RGB color output signals for a color video monitor.

CPU Card

- A five-pin "DIN" connector provides for connection of the keyboard.

Memory Card

- A parallel connector provides for connection to a Centronics-type parallel printer or other parallel input/output devices.

Power On

- Press the power switch located on the rear of the chassis to ON.

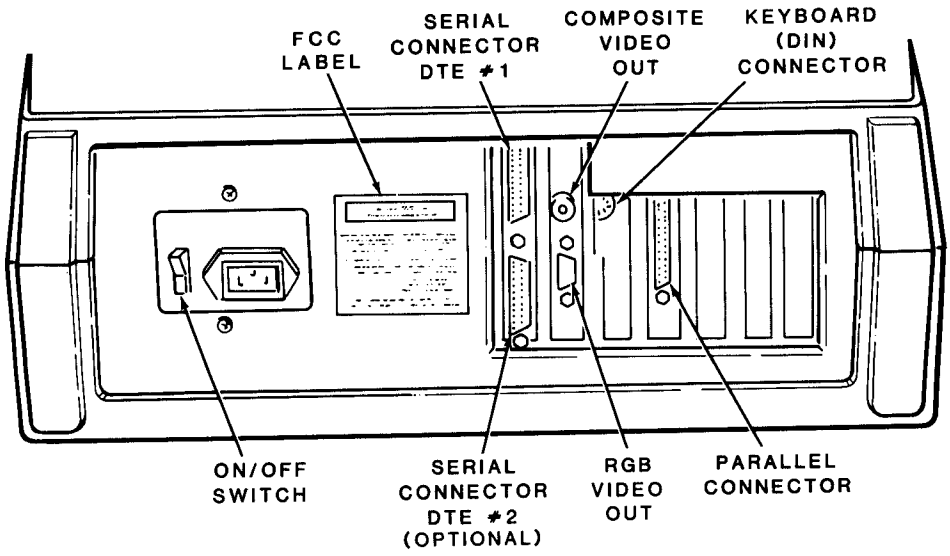

Figure 2.2. Z-160 Rear View

Bootup Procedures

The floppy disk systems come from the factory set for autoboot drive 0 (A), the left-most floppy disk drive. When power is turned on, the computer will automatically boot the system disk installed in drive A. If no disk is installed in the drive, the following error message will result:

```
+++ DISK ERROR: DRIVE NOT READY! +++
```

Autoboot can be defeated by pressing the ESC key.

The computer is software reset by pressing the CTRL, ALT, and DEL keys simultaneously. Switching the computer off and then on generates a hard reset.

The computer can be returned to the system monitor by pressing the CTRL, ALT, and INS keys simultaneously.

The computer can be configured for **no** autoboot drive 0 (A) through the use of a switch on the CPU card (refer to the *System CPU Card Service Module* for the switch settings). When in this configuration, insert the system disk, type **B**, and press the **RETURN** key after receiving the prompt.

To boot drive 1 (B), the right-most floppy disk drive, type **B1**, and press the **RETURN** key.

Chapter 3

Theory of Operation

Introduction

This chapter provides a brief theory of operation of the Z-160 Portable Personal Computer. If a more detailed theory of operation is desired, refer to the appropriate service module.

Refer to the block diagram, Figure 3.1, as you read the following description. The Z-160 Portable Personal Computer consists of the following blocks:

- Power Supply
- Backplane Board
- Keyboard
- Floppy Disk Controller Card
- Two 5-1/4" half-height drives
- CPU Card
- Video/Color/Composite Card
- Memory Card
- Video Driver Board/Video Deflection Board
- Four optional card slots

Some of the options available are:

- Bit-Mapped Video Graphics Card
- A second Memory Card

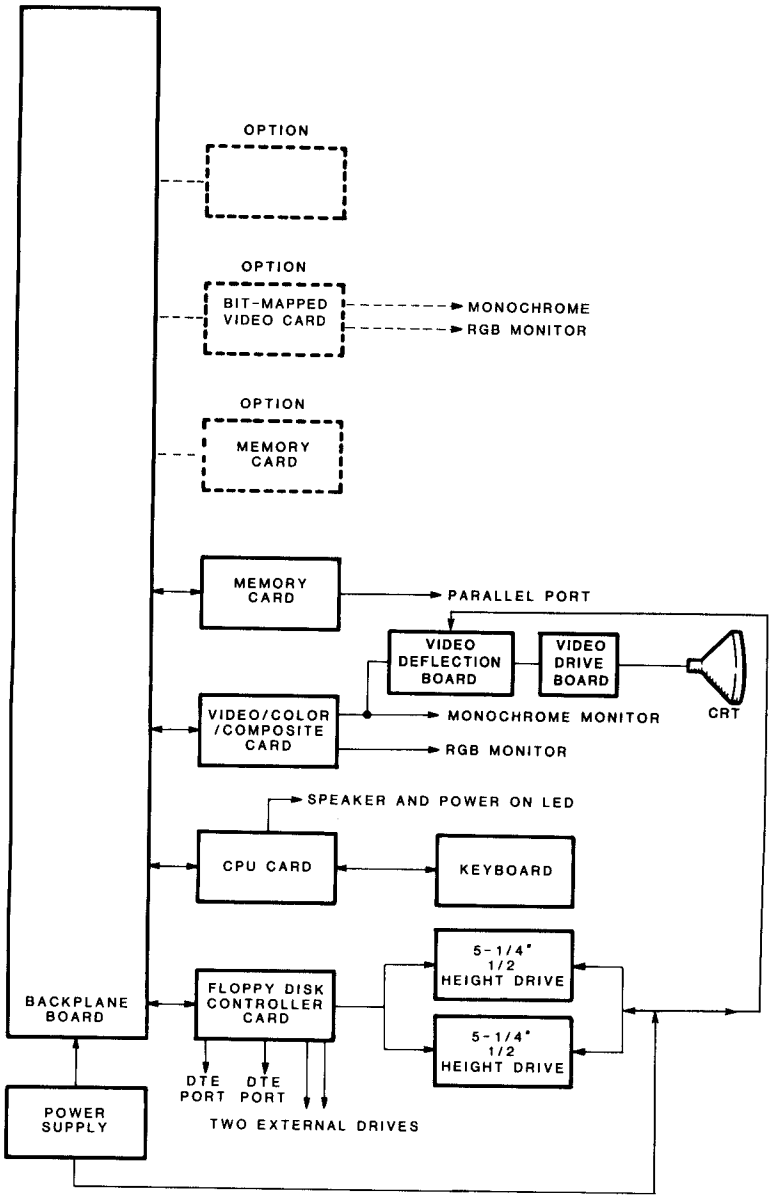

Figure 3.1. Z-160 Computer Block Diagram

System Block Descriptions

Power Supply

The power supply is an on-line, switching mode power supply. The power supply provides +12 VDC, −12 VDC, +5 VDC, and a power supply good (PSG*) signal to the backplane board, and voltages to the disk drives. The power supply is cooled by an internal fan and is protected from overvoltage, undervoltage, overcurrent, and overtemperature. This power supply is **not** serviceable.

Backplane Board

The backplane board provides bus interfacing between all cards and the power supply. Five light-emitting diodes (LEDs) and a −5 VDC regulator are located on the board. The LEDs indicate the status of the power supply.

Floppy Disk Controller Card

The floppy disk controller card provides the necessary read/write and control signals for the internal 5-1/4″ disk drive(s). A connector is provided for up to two external disk drives (not supported at this time). The floppy disk controller card also contains a serial RS-232 (DTE) output port (a second port is optional).

Disk Drives

The currently approved internal 5-1/4″ half-height drives are Shugart (Z-207-7), Mitsubishi (Z-207-71), or Matsushita. These drives use 48-TPI double-sided, double-density disks. The list of approved drives may be expanded in the future.

CPU Card

The CPU card uses an 8088 or 80C88 16-bit microprocessor with an option for an 8087 microprocessor. The CPU card controls the timing, addressing, and generation of control signals for the computer. The keyboard, speaker, and power-indicating LEDs all are interfaced to the CPU card. The CPU card contains six LEDs used as an aid in troubleshooting.

Keyboard

The keyboard communicates serially with the computer under software (firmware) control. The keyboard outputs normal ASCII characters or special function codes. The keyboard control circuits contain an oscillator circuit which provides for the bell and key click.

Video/Color/Composite Card

The video/color/composite card provides the IBM® PC-compatible composite monochrome or RGB color output signals to a monochrome or color monitor.

Memory Card

A fully populated memory card contains 320K of RAM (five banks). Associated memory card circuitry provides parity checking and refresh cycles. A parallel output port is provided on this card.

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Video Deflection Board

The video deflection board provides the vertical and horizontal deflection circuits and high voltages necessary for the CRT display.

Video Driver Board

The video driver board provides the video drive necessary for the CRT display.

Options

Options available for the computer are listed below.

Memory

An optional second memory card may be installed, providing the computer with a maximum of 640K of memory. The first memory card must be fully populated before the second memory card will be recognized, or the memory will not be differentiated.

Bit-Mapped Video Graphics Card

An optional bit-mapped video graphics card may be installed, providing high resolution bit-mapped graphics similar to those in the Z-100 family of computers.

Chapter 4

Disassembly

This chapter contains disassembly information for the Z-160 Portable Personal Computer. Refer to Figures 4.1 and 4.2 while disassembling to the appropriate level.

WARNING: Verify that the power switch is OFF and the line cord is disconnected before beginning the disassembly procedures.

CAUTION: Integrated circuits are electrostatic-sensitive devices. These devices can be damaged by static electricity.

Disassembly Procedures

Disk Drive Assembly Removal (322)

- Set the disk drive assembly to the open position.
- Push back on the front supports (375) of the assembly while pivoting it back to a vertical position.
- Disconnect two power connectors (390A and 390B) and one data cable with ground (395).
- With assembly held vertical to the base unit, lift it straight up and off.

Floppy Disk Controller Card Removal (55)

- Remove disk drive assembly.
- Remove four screws (10) and lift off top cover (5) by sliding it back until the lip clears the front panel (115), and then lift straight up.
- Unplug the small connector from the front of the CPU card (70), and the internal video display cable from the video/color/composite card (65).
- Unplug the data cable (50) from the disk controller card (55), remove screw (60), and unplug the card from the backplane (85).

Video/Color/Composite Card Removal (65)

- Remove disk drive assembly.
- Remove four screws (10) and lift off top cover (5) by sliding it back until the lip clears the front panel (115), and then lift straight up.
- Disconnect the internal video display cable and any external cables from the video/color/composite card (65).
- Remove screw (60) and unplug the card from the backplane (85).

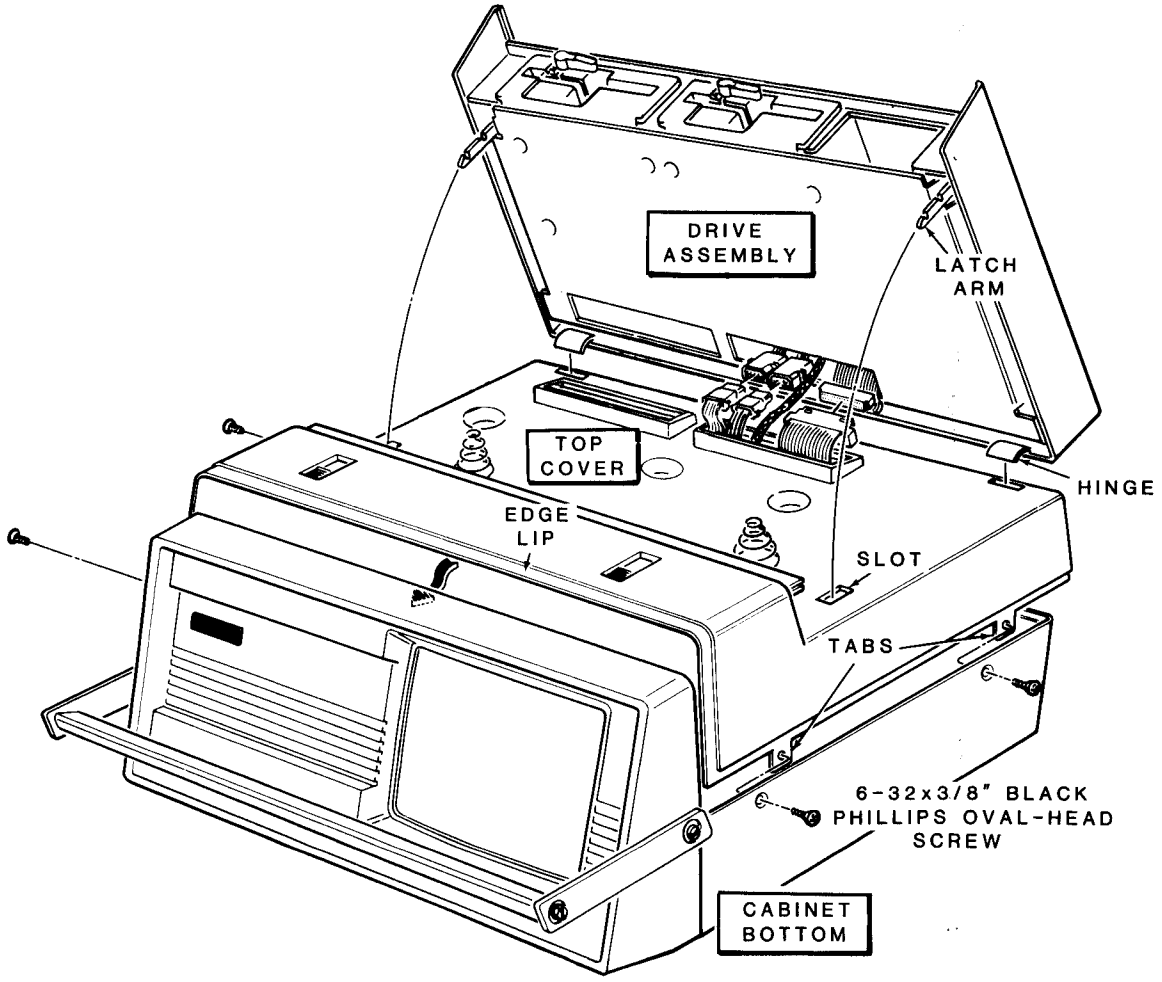

Figure 4.1. Disk Drive Assembly Removal

System CPU Card Removal (70)

- Remove disk drive assembly.
- Remove four screws (10) and lift off top cover (5) by sliding it back until the lip clears the front panel (115), and then lift straight up.
- Disconnect the external keyboard cable from the back of the CPU card (70).
- Remove screw (60) and unplug the card from the backplane (85).

Memory Card Removal (75)

- Remove disk drive assembly.
- Remove four screws (10) and lift off top cover (5) by sliding it back until the lip clears the front panel (115), and then lift straight up.
- Disconnect any external cables connected to the memory card (75).
- Remove screw (60) and unplug the card from the backplane (85).

Optional Card(s) Removal

- Remove disk drive assembly.
- Remove four screws (10) and lift off top cover (5) by sliding it back until the lip clears the front panel (115), and then lift straight up.
- Disconnect cable assemblies (if required).
- Remove screw (60) and unplug the card from the backplane (85).

Backplane Board Removal (85)

- Remove disk drive assembly.
- Remove four screws (10) and lift off top cover (5) by sliding it back until the lip clears the front panel (115), and then lift straight up.
- Disconnect cable assembly (50) from floppy disk controller card (55).
- Disconnect any external cables connected to the floppy disk controller card (55).
- Remove screw (60) and unplug the card from the backplane (85).
- Disconnect the internal video display cable and any external cables from the video/color/composite card (65).
- Remove screw (60) and unplug the card from the backplane (85).

- Disconnect the internal speaker cable and the external keyboard cable from the system CPU card (70).
- Remove screw (60) and unplug the card from the backplane (85).
- Disconnect any external cables connected to the memory card (75).
- Remove screw (60) and unplug the card from the backplane (85).
- Remove optional card(s), if installed.
- Disconnect power supply connector (95A).
- Remove six screws (90) and lift out the backplane board (85).

Power Supply Removal (95)

- Remove disk drive assembly.
- Remove four screws (10) and lift off top cover (5) by sliding it back until the lip clears the front panel (115), and then lift straight up.
- Disconnect power supply cable.
- Disconnect disk drive power cable(s) (95B and 95C).
- Remove two screws (90) from the rear and four hex nuts (100) from the bottom of the chassis.
- Remove power supply (95).

NOTE: If a replacement power supply is to be installed, remove two screws (60), J bracket (105), and two foam strips (110).

Disk Drive Removal

- Remove disk drive assembly.
- Lay the disk drive assembly bottom side up on a towel or other soft surface, and remove two screws (415) and four screws (330).
- Carefully lift the metal disk drive mounting plate (340) from the drive assembly cover (325).
- Unplug the power connector and the data cable from the desired disk drive.
- Turn the drive mounting plate over and set it down so that the top of the drive(s) is/are resting on your work surface.
- Remove the four screws (350) from the desired drive, and lift the mounting plate (340) from the drive.

Speaker Removal (260)

- Remove disk drive assembly.
- Remove four screws (10) and lift off top cover (5) by sliding it back until the lip clears the front panel (115), and then lift straight up.
- Remove floppy disk controller card (55).
- Remove video/color/composite card (65).
- Remove system CPU card (70).
- Remove memory card (75).
- Remove optional card(s), if installed.
- Cut nylon ties holding the speaker cable to the chassis (3 places).
- Remove speaker (260) by gently rocking it out of the rubber grommet (270).

CRT Removal (180)

- Remove disk drive assembly.
- Remove four screws (10) and lift off top cover (5) by sliding it back until the lip clears the front panel (115), and then lift straight up.
- Remove two screws (225) and detach the handle by gently pulling the arms (220) away from the base unit.
- Remove five screws (120) and pull off the front panel. Be careful not to pull the panel too far from the base unit or you may damage the cable going to the contrast potentiometer.
- Discharge the CRT anode and remove the anode connector from the CRT (180).
- Remove the video driver board (200C) from the rear of the CRT (180).
- Loosen the hex head screw on the yoke assembly (200B) and slide it from the neck of the CRT (180).
- While supporting the CRT (180) with your hand, remove four screws (185), four washers (190), and CRT (180).

Video Driver/Video Deflection Boards Removal (200)

NOTE: This is a hardwired assembly consisting of:
Video Deflection Board (200A).
CRT Yoke Assembly (200B).
Video Driver Board (200C).

- Remove CRT (180) (see CRT Removal).
- Remove 10-position plug at rear of video deflection board (200A).
- Remove two screws (90) and unplug the board from the two nylon retainers on its forward edge.

Chapter 5

Troubleshooting

Introduction

This computer contains a very powerful servicing aid in the form of diagnostic and system check subroutines programmed permanently into the machine's read-only memory (ROM).

These subroutines, in conjunction with the power supply diagnostic LEDs on the backplane board, and the system diagnostic LEDs on the CPU card, will test, and indicate relevant failures in a high percentage of the computer system circuitry.

Also incorporated in the ROM code are provisions for loading (booting) an operating system, such as MS™-DOS, from any disk drive in your system. DIP switches on the CPU card may be positioned to implement an autoboot at powerup, or a keyboard-initiated manual boot at the operator's discretion. Refer to the configuration section of the *System CPU Card Service Module* for DIP switch setup instructions.

NOTE: It also is recommended that the Z-100 PC Series Disk-Based Diagnostics Package, Model CB-5063-13, be utilized in cases where the foregoing aids do not localize a problem. Details on the use of this utility are provided with the diagnostics package.

™ MS is a trademark of Microsoft Corporation.

ROM Diagnostics — General

The ROM-based diagnostics are comprised basically of three types:

- Automatic checks performed at powerup;
- User or serviceman-selected tests; and
- Debugging routines to force specific operating conditions.

Power-Up Checks

The following hardware checks are automatically made when the computer is first turned on:

- Central processor unit (CPU)
- Read-only memory (ROM)
- User random access memory (RAM) (first and last 64K only)
- Interrupt control and timer circuits
- Parity RAM
- Keyboard microprocessor

NOTE: These checks are made only after a system disk is booted.

- Disk drive ready
- Disk drive seek function
- Disk controller
- Disk direct memory access (DMA) overrun
- Disk sector
- Disk cyclic redundancy check (CRC)
- Disk address mark

User-Selected Tests

In addition, the user/serviceman may menu-select the following test sequences (refer to Menu-Selected Tests in this chapter).

- Disk read
- Keyboard
- Memory
- Power-up test

Any of the test sequences will result in a test screen displaying the test name, number of passes made, and keyboard key sequence required to abort the test. In the event an error is encountered, the test also will abort and an error message will be displayed. Refer to the Automatic Power-Up Checks/Screen Error Messages section of this chapter for a description of error messages.

Unlike the memory test run by the automatic routines, which only tests the first and last 64K of RAM, the memory test selected here checks all the user RAM plus the 16K of video screen RAM.

Diagnostic LEDs

The LEDs on the backplane board and CPU card also are very useful for fault determination, and are described in the following material.

Backplane Board LEDs

Figure 5.1 shows the component layout scheme for the backplane circuit board.

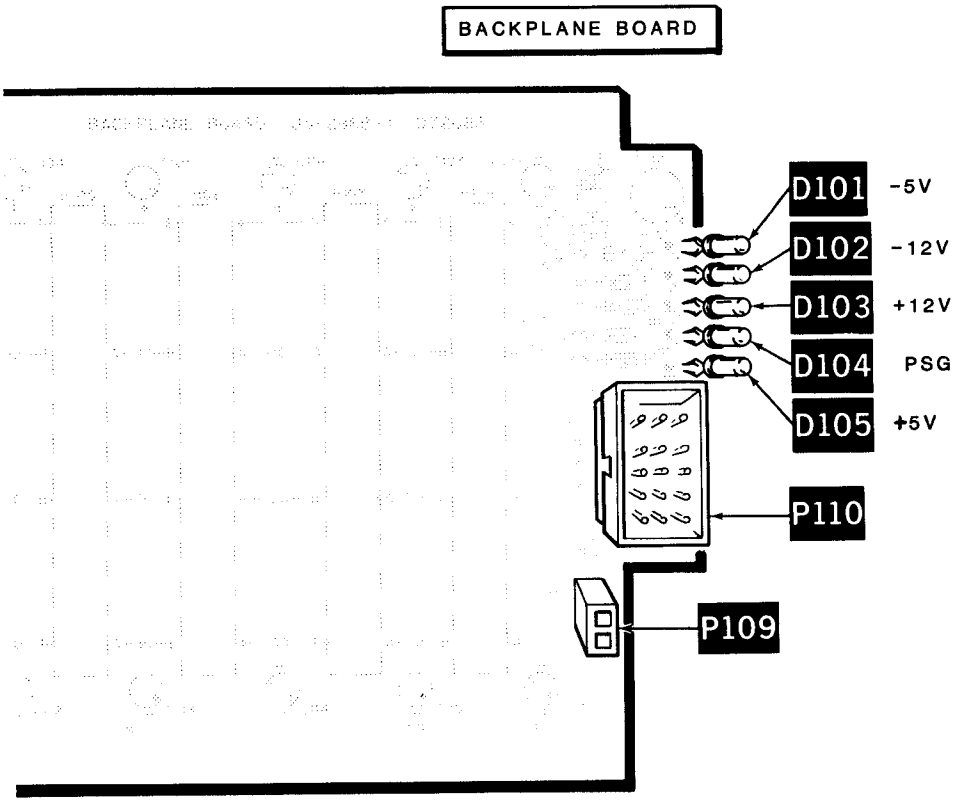

Figure 5.1. Backplane Board LED Locations

Refer to Figure 5.1 for the location of the LEDs which indicate power supply integrity, PSG, plus (+) and minus (−) 12 VDC, plus (+) 5 VDC from the power supply, and the minus (−) 5 VDC developed by the −5 VDC regulator from the (−)12 VDC input to the backplane board.

CPU Card LEDs

Refer to Figure 5.2 to identify and locate the six LEDs located on the CPU card. Table 5.1 defines these LEDs in terms of the parameters tested.

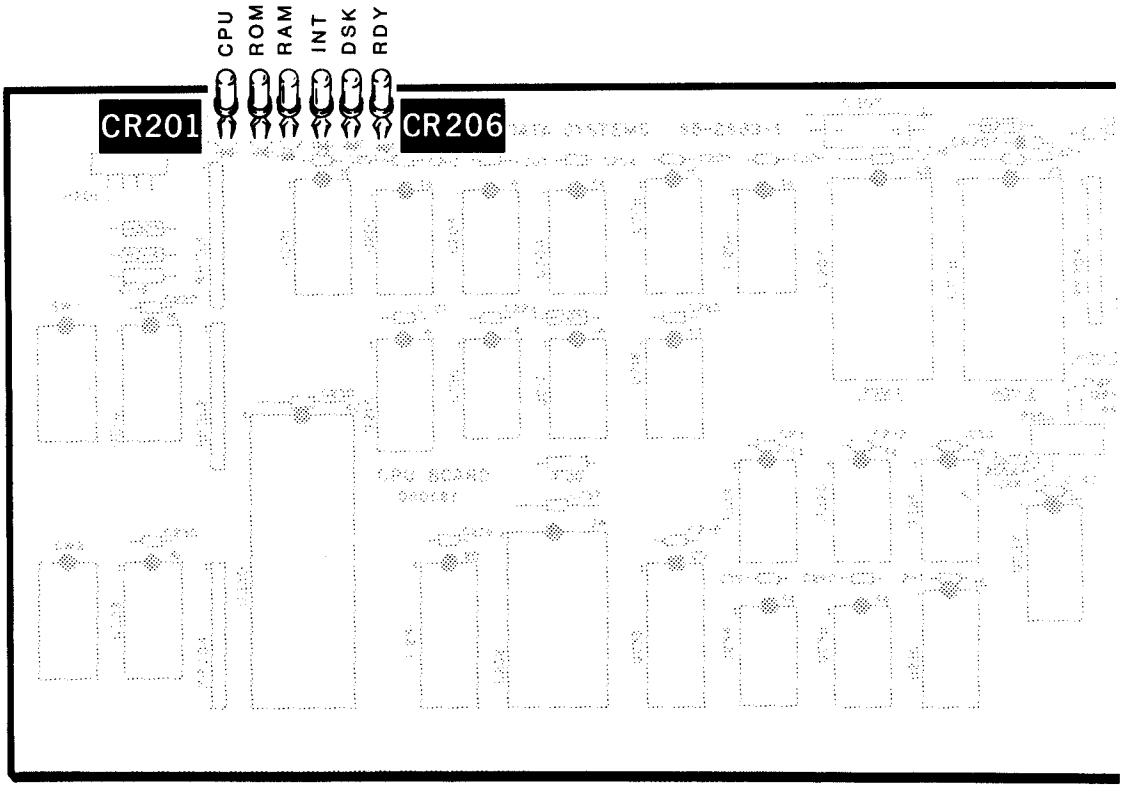

Figure 5.2. CPU Card LED Locations

Table 5.1. CPU Card LED Identification

LED NAME	FUNCTION TESTED.
CPU	Proper operation of the central processing unit on the CPU card. Lights if CPU is not responding properly.
ROM	Read-only memory. Lights if program ROM appears to be invalid.
RAM	Random access memory. Lights to indicate RAM is not storing information correctly.
INT	System clock check. Lights if clock is not running or running at incorrect frequency. Looks for an interrupt on powerup.
DSK	Disk controller. Extinguished when controller is reset. Lights if controller does not respond properly. Looks at drive A only; steps to track 30 and then to track 00.
RDY	Operating system boot indicator. Is on initially; goes out when rest of test routines are completed, the operating system is successfully booted from disk, and a DMA is begun.

The LEDs are extinguished sequentially, from the front of the card to the rear, so that more than one indicator may be on at once in the event a parameter fails before the entire automatic sequence is completed. The illuminated LED closest to the front of the CPU card identifies the failed test.

Detailed Diagnostic Operation

The following procedures define use of the various built-in diagnostic subroutines in sufficient detail for service/bench level fault isolation. In general, the procedures are presented in the sequence most likely to be of use in the normal course of problem occurrence/method of correction. Use of this information assumes the computer was operating properly prior to the malfunction.

Automatic Power-Up Checks/Screen Error Messages

The following paragraphs describe possible screen error messages which may occur at powerup, and the corrective action necessary to resolve the problem.

If the following messages appear,

```
+++ ERROR: CPU failure! +++
```

or

```
+++ ERROR: ROM checksum failure! +++
```

the CPU card may be malfunctioning. The checksum message is a result of a mismatch between a predetermined value and a value derived from the contents of system ROM. Turn the machine off, then on again. If the same message reoccurs, refer to the troubleshooting messages in the *System CPU Card Service Module*.

```
+++ ERROR: RAM failure! Address: XXXX:YYYY, Bit: N, Chip: UXXX +++
```

where U4XX is the memory card and U3XX is the video card.

or

```
+++ ERROR: Parity hardware failure! Address: XXXX:YYYY, Bit: N, Chip: UXXX +++
```

or

```
+++ ERROR: Parity failure! Address: XXXX:YYYY, Chip: UXXX +++
```

messages indicate a malfunction on the system memory card. If Zenith memory cards are installed, the chip number displayed defines which chip is at fault. The most probable reason for an error of these types is incorrect positioning, or malfunctioning, of the CPU DIP switches related to system memory size. However, if the computer was performing properly before the problem developed, switch positions probably are not at fault.

Refer to the troubleshooting section in the *Memory Cards Service Module*.

```
+++ ERROR: Timer interrupt failure! +++
```

This message indicates that the timing logic on the CPU card is erroneous, i.e., the system clock frequency is absent or incorrect, or an interrupt function on an added card has been misconfigured. First, eliminate added cards as a problem source, then refer to CPU card troubleshooting procedures in the *System CPU Card Service Module* if the cause has not been determined.

```
+++ ERROR: Invalid/No keyboard code received! +++
```

A message of this type indicates that the keyboard did not send the proper code at powerup to indicate proper functioning. The most likely cause is a disconnected keyboard. If this is not the case, refer to keyboard troubleshooting in the *Keyboard Service Module*.

```
+++ DISK ERROR: Drive not ready! +++
```

or

```
+++ DISK ERROR: Seek failure! +++
```

messages usually occur when inability to boot up an operating system is encountered, such as when no disk is in the drive or the drive door is open.

```
+++ DISK ERROR: Bad disk controller! +++
```

or

```
+++ DISK ERROR: DMA overrun error! +++
```

Errors of this nature usually indicate a malfunction of the disk controller card, but also may be forced by other defective cards in the system. If nonstandard cards have been installed, remove them and power up again, reinserting the cards one at a time until the error reappears. Then take corrective action on the last card installed. If the error is present with all nonstandard cards, remove and replace the disk controller card.

```
+++ DISK ERROR: Sector not found! +++
```

or

```
+++ DISK ERROR: CRC error! +++
```

or

```
+++ DISK ERROR: Invalid address mark detected! +++
```

These error messages normally indicate a defective drive, or an operating system was not found on the selected drive. First, try a different disk. If this error occurs often, it may be necessary to perform the alignment procedures for the affected drive, or take remedial steps to make sure the disk controller card functions properly.

No Error Message

A malfunction may occur that prevents an error message from being displayed. In cases of this type, it is best to first seek overt physical reasons for the malfunction, such as smoke, unusual heat and odors, or audible symptoms such as popping, sizzling, or crackling sounds. If none of these symptoms are in evidence, the computer cover should be removed, and the power supply LEDs on the backplane board inspected to see if any of the supply voltages are absent. Weak or extinguished LEDs may indicate that the associated voltage is nonexistent, low, or that excessive DC ripple is present on the supply line.

Refer to the troubleshooting section of the *Power Supply Service Module* if the +12, −12, +5 VDC, or the PSG LEDs appear abnormal, and to the troubleshooting section of the *Backplane Board Service Module* if the −5 VDC LED appears abnormal. The −5 VDC is derived from the −12 VDC, so if both of these LEDs appear abnormal, the power supply would be the logical starting point for fault isolation.

Menu-Selected Tests

In addition to the automatic checks, several keyboard-selected tests may be performed by calling up the test menu. Type the word **TEST** and then press the **RETURN** key at the system prompt arrow indication. The following menu will appear on the screen:

```
CHOOSE ONE OF THE FOLLOWING:

1. DISK READ TEST
2. KEYBOARD TEST
3. MEMORY TEST
4. POWER-UP TEST
5. EXIT

ENTER YOUR CHOICE:
```

Select one of the desired test sequences by number. The main advantage of testing in this fashion is that these sequences will run continuously until ESC is pressed by the operator, or an error is encountered. This makes the routines extremely useful in the event a malfunction is intermittent, time-dependent, or a result of heat buildup. An onscreen count is displayed to keep track of the number of times the particular test is run. The possible error messages are the same as those described under Automatic Power-Up Checks.

After a test is selected, a second screen appears, with the test name at top-left, the message TYPE ESC TO ABORT at bottom-left, and the test count at approximately center-screen. If the test is aborted, the message TYPE ESC TO EXIT appears at bottom-left. Pressing the ESC key returns you to the test menu. If the test is aborted by an error, an error message appears underneath the test name, and the message TYPE ESC TO EXIT appears at bottom-left.

If an error message appears, you should refer to the troubleshooting section of the service module for the card associated with the error.

Using the ROM-Based Debugging Routines

Another excellent means of fault isolation is to use the built-in program debug features of the computer. While these routines are primarily designed for finding and clearing errors in programs, some of the commands and features provide an efficient means of narrowing the field of search in difficult fault-isolation situations. Use of these aids assumes a knowledge of programming the 8088 microprocessor at the assembly level, and an understanding of terminology associated with this level of programming, such as "flag", "register", "pointer", "bit", "byte", etc.

The commands and features of the debugging package comprise a substantial subset of the Microsoft® DEBUG utility supplied with MS-DOS. Among the more useful utilities included are the abilities to:

- Boot an operating system from a disk drive;
- Change video and scrolling modes;
- Display the contents of memory;
- Input or output values to or from I/O ports;
- Search memory for a byte pattern;
- Execute a program;
- Single step a program;
- Set program breakpoints.

NOTE: Because of the interrupt-driven nature of the keyboard, user-written programs must incorporate commands to enable interrupts, or the keyboard information will not be recognized by the 8088 microprocessor. Programs performing I/O through the ROM-ware should meet this requirement, as the ROM routines automatically enable interrupts for short periods of time.

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In the descriptions of the commands which follow, certain shorthand notations are used to indicate specific syntax requirements. The braces, brackets, and bars do not actually appear in the commands, but delimiters, such as commas, spaces, and colons which appear within these symbols, may appear in the commands.

Items in brackets — [*item*] — are optional.

Items in braces, separated by vertical bars — {DOG | CAT | EDIT} — represent choices. One, and only one, choice may be specified.

Items in lower case italics — *parameter* — are mandatory, and may take one of these two forms. If the item is uppercase, it represents a specific key to be pressed. If the item is lowercase, it means the user must specify a parameter or group of parameters. Examples:

RETURN — press the specified key (in this case, the RETURN key).

port — you specify the *port* address.

Items followed by an ellipsis — ... — means that several items of the same type may be specified. Example:

string is: "*CHARACTER*[*CHARACTER*]..."

would define a character string composed of one or more specified characters.

Command Summary

To use the debug routines, the system prompt arrow must be displayed, which means the disk operating system either must not be booted up, or you must exit the operating system. The following commands will then be available.

? *RETURN*

where RETURN is the RETURN key. This is the help command. It displays a list of commands, including a syntax diagram, and usage examples.

B[*drive*][:*part*] *RETURN*

where drive is: {0 | 1 | 2 | 3 | }
and part is any number up to 7.

and RETURN is the RETURN key. The command summary reads the operating system boot code from disk and executes it. If an error is detected, an error message is displayed (see error message information in preceding text). The default drive is drive 0.

Example: **B3** ***RETURN*** would boot from drive 3.

C *RETURN*

Displays color bar chart for video monitor alignment.

where RETURN is the RETURN key.

D *address*[{L*length* | ,*offset*}]

where *length* is a hexadecimal number between 0000 and FFFF.

Displays the contents of a block or portion of memory in hexadecimal and ASCII. If the ASCII value represents a nonprinting character, an ASCII period (.) is displayed. If *length* is specified, the display will consist of *length* number of bytes.

Example 1: `D1234:5678 L200` would display, in hexadecimal (hex) and ASCII, the contents of 200 (hexadecimal) locations starting at memory address 179B8.

Example 2: `D3312:0,13E` would display the contents starting at memory address 33120 and ending at address 3325E.

E *address RETURN*
then {{ *SPACE* | *number* }... | *RETURN* }

Examines and/or changes the contents of a memory location. Displays the value of a memory-byte and requests user input. If a "-" is entered, the contents of the previous memory location is shown, and if a *SPACE* is used, the next byte is displayed. If instead of the hyphen or space, a hex number from 00 to FF is entered, this value will replace the contents at *address*.

Example: `E0:100` interrogates memory address 100.

F *range, list RETURN*

where *list* is: {*number* | *string*} [*number* | *string*]...
string is: "*character* [*character*]..."
and *character* is any printing character from keyboard

Fill specified *range* of memory with data contained in *list*. Data is recirculated until specified range is filled.

Example: `F1800:0, 3FFF, 05, 04, 03, 02, 01, "Ignition!"` would fill 3FFF memory locations with data 5, 4, 3, 2, 1 "Ignition!", starting at address 18000.

`G [address] [,breakpoint]... RETURN`

where *breakpoint* is an offset from the 8088 CS register, in the range 0000 to FFFF.

The "Go" command initiates program execution with up to eight breakpoints. When a breakpoint is encountered, the routine saves the processor status for the "R" and "G" commands and displays the 8088 microprocessor register contents.

Example: `G 5000:3ACD` executes a user-program beginning at 53ACD.

`H offset,offset RETURN`

performs hex arithmetic on the two offset values. Returns the sum and difference.

Example: `H 43C7,99FA` would return DDC1 for the sum, and 5633 for the difference.

`I port RETURN`

where *port* is a value between 000 and 3FF, returns the contents of the specified port.

Example: `I 3FE` would return the contents of input port 3FE.

`M range,address RETURN`

moves the block of memory specified by *range* to the destination *address*. The move is implemented in a fashion which prevents overlapping moves from overwriting other data.

Example: `M 3219:FEDC, FFFF, 3905:0` moves FFFF bytes of data from 4206C to 39050.

O *port, value RETURN*

where *value* is a number between 00 and FF, writes a value to the specified port address.

Example: **O 3, FB** would write the value FB to output port 3.

R [*register_name*] *RETURN*

where *register_name* is one of the following valid 8088 microprocessor register names: AX, BX, CX, DX, SI, DI, BP, SP, SS, CS, DS, ES, IP, PC, or FL. IP and PC both refer to the instruction pointer. The instruction pointer examines or modifies the specified register, depending on the form of the command. If no register is specified, all register contents are displayed. If a single register is specified, the contents of that register are displayed and the user prompted for input. If a valid hex number is entered, the specified register's contents are changed to that value.

The FL (flag) register contents are not displayed in hex, but as a two-letter abbreviation representing the specific flag's condition, as defined in Table 5.2.

Table 5.2. Flag Register Messages

FLAG	ON	OFF
Overflow	OV (overflow)	NV (no overflow)
Direction	DN (down)	UP (up)
Interrupts	EI (enabled)	DI (disabled)
Sign	NG (negative)	PL (plus)
Zero	ZR (zero)	NZ (not zero)
Auxiliary Carry	AC (carry)	NA (no carry)
Parity	PE (even)	PO (odd)
Carry	CY (carry)	NC (no carry)

To change a given flag register, any of the abbreviations may be entered at the 'R' user-input prompt. For example, entering 'NG PO' would set the sign flag and reset the parity flag. If more than one abbreviation is entered for the same flag, the flag condition will conform to the last entry.

S *range, list RETURN*

searches the specified *range* for a string composed of *list*.

Each time the string is found, the starting address of the string is displayed.

Example: S 2400:15, 8CD, "Alpha" would scan 8CD bytes of memory beginning at 24015 for the string Alpha.

T [*address*] [,*value*] *RETURN*

traces a user program. Single steps through the program beginning at *address*, displays the 8088 microprocessor register contents as each instruction is executed. *Value* determines how many times to execute before returning control to the user. Default is one execution. The default address is the current address.

TEST *RETURN*

performs extended diagnostics. This command results in the menu display covered under Menu-Selected Tests, discussed earlier in this chapter.

U *range*

disassembles program in range.

V {*M video_mode* | *S scroll_mode*}

is used to set the current video mode or scroll mode. Table 5.3 shows the various video modes obtainable with the V M command.

Table 5.3. Video Mode Selection

CODE	MODE
0	40 columns × 25 rows (monochrome).
1	40 columns × 25 rows (color).
2	80 columns × 25 rows (monochrome).
3	80 columns × 25 rows (color).
4	320 × 200 resolution graphics (color). Text in 40 × 25.
5	320 × 200 resolution graphics (monochrome). Text in 40 × 25.
6	640 × 200 resolution graphics (monochrome). Text in 80 × 25.
7	IBM monochrome board.

Example: `V M6` would select high resolution graphics.

Table 5.4 indicates the scroll modes obtainable with the V S command. The scroll mode determines the manner in which information on the screen is handled once the screen is full.

Table 5.4. Scrolling Mode Selection

CODE	SCROLL MODE
0	Software (compatible) scroll mode. Information is scrolled by actually moving screen memory contents. It also is the default scrolling mode, as some applications packages may not function using the other modes.
1	Hardware (jump) scrolling. This mode, though incompatible with some applications packages, is faster than the software mode. May be used only when in 80 × 25 or the graphics video modes.
2	Smooth scrolling. Usable only in 40 × 200 graphics mode. Moves characters upward in small segments, resulting in a more pleasing and readable display.

Example: `V S1` selects hardware (jump) scrolling.
`V M6 S2` selects high resolution graphics with smooth scrolling.

Special Keys

Table 5.5 defines the keyboard keys and associated functions recognized by the monitor ROM. These keys permit certain editing operations, and control the format of the screen display.

Table 5.5. Special Keys

KEY	FUNCTION
BACK SPACE	Press to correct typographical errors prior to command line execution (i.e. before RETURN is pressed). Backs up and deletes one character each time pressed.
RETURN	Executes the command line.
, or Space	Used as delimiters interchangeably between elements of a command.
SCROLL LCK or CTRL S	Pause screen output until depressed a second time.
CTRL NUM LCK	Halts computer operation until any other key is pressed.
CTRL SCROLL LCK or CTRL C	Terminates any executing command and returns control to user.
CTRL ALT DEL	A three-key combination which results in a power-on reset. System reinitializes and power-up diagnostics are performed.
CTRL ALT INS	A three-key sequence used to interrupt execution of a program, or return to the monitor ROM, usually during the debugging process. The keyboard-activated equivalent of a program break point. User may then modify or examine 8088 microprocessor registers, I/O ports, or memory contents. To restart program execution at the point interrupted, the G command is entered, without *address*.

Chapter 6

Reassembly

This chapter contains assembly information for the Z-160 Portable Personal Computer. Refer to Figures 6.1 and 6.2 while reassembling the computer.

WARNING: Verify that the power switch is OFF and the line cord is disconnected before beginning the reassembly procedures.

CAUTION: Integrated circuits are electrostatic-sensitive devices. These devices can be damaged by static electricity.

Reassembly Procedures

Video Driver/Video Deflection Boards/ CRT Yoke Installation (200)

NOTE: This is a hardwired assembly consisting of:
Video Deflection Board (200A).
CRT Yoke Assembly (200B).
Video Driver Board (200C).

- Position the video deflection board (200A) so that the end with the 10-position connector is toward the rear of the base unit, and secure it by snapping the two nylon posts into the front mounting holes and securing the rear with two screws (90).
- Install the 10-position plug at the rear of the board and replace the CRT (180).
- Install the top cover by carefully lowering it into the base unit while positioning the front lip under the edge of the front panel (115), and the bottom tabs inside the base unit. As you are lowering the top cover, route the disk drive power cables (95A and 95B) and the disk controller data cable (50) through the center slot at the back of the cover. Secure with four screws (10).
- Install the disk drive assembly.

CRT Installation (180)

CAUTION: The anode socket on the CRT may have a residual charge still on it. Be careful not to touch this connector while installing the CRT.

- Install the CRT (180) into the chassis and secure with four screws (185), four washers (190), and the CRT grounding clip (195). Verify that the CRT grounding clip (195) is properly positioned against the CRT (180).

NOTE: The yoke assembly (200B) may have to be slid onto the neck of the CRT while you are positioning the CRT in the chassis.

- Slide the yoke assembly (200B) onto the neck of the CRT and secure it by gently tightening the clamping screw.
- Plug the video driver board (200C) onto the back of the CRT (180).
- Discharge the CRT anode and connect the high voltage lead.
- Install the front panel (115) with five screws (120).
- Install the handle with two screws (225), two washers (230), and two spacers (235).
- Install the top cover by carefully lowering it onto the base unit while positioning the front lip under the edge of the front panel (115), and the bottom tabs inside the base unit. As you are lowering the top cover, route the disk drive power cables (95A and 95B) and the disk controller data cable (50) through the center slot at the back of the cover. Secure with four screws (10).
- Install the disk drive assembly.

Speaker Installation (260)

- Install speaker (260) into grommet (355).
- Secure the speaker cable along the lower front chassis rail with nylon ties.
- Install any optional cards and secure with screw (60).
- Install memory card (75) and secure with screw (60).
- Install system CPU card (70) and secure with screw (60).
- Plug the speaker connector into the system CPU card (70).
- Install video/color/composite card (65) and secure with screw (60).
- Install floppy disk controller card (55) and secure with screw (60).
- Connect cable assembly (50) to the floppy disk controller card (55).

- Install the top cover by carefully lowering it onto the base unit while positioning the front lip under the edge of the front panel (115), and the bottom tabs inside the base unit. As you are lowering the top cover, route the disk drive power cables (95A and 95B) and the disk controller data cable (50) through the center slot at the back of the cover. Secure with four screws (10).
- Install the disk drive assembly.

Disk Drive Installation

- Position the disk drive on your work surface so that the bottom side (the side opposite the drive logic board) is up.
- Position the drive mounting plate (340) so that the four holes on the disk drive line up with the desired four holes of the mounting plate.
- Secure the disk drive to the drive mounting plate with four screws (350), four washers (380), and four spacers (360).
- Turn over the drive mounting plate with the disk drive(s) mounted on it, and plug the data cable (395) and drive power extension cable (390) into the disk drive unit(s).
- Position the cables so they protrude through the center-most hole at the rear of the disk drive mounting plate.
- Position the drive assembly cover (325) upside down on your work surface, and lower the drive mounting plate with the disk drive(s) into the cover.
- Secure the disk drive mounting plate to the cover with four screws (330), and two screws (415).
- Install the disk drive assembly onto the base unit.

Power Supply Installation (95)

- Place the power supply (95) in position at the rear of the chassis, and secure with two screws (90) at the rear, and four hex nuts (100) in the base.
- Plug the power supply connector (95A) into the receptacle on the backplane (85).
- Install the top cover by carefully lowering it onto the base unit while positioning the front lip under the edge of the front panel (115), and the bottom tabs inside the base unit. As you are lowering the top cover, route the disk drive power cables (95A and 95B) and the disk controller data cable (50) through the center slot at the back of the cover. Secure with four screws (10).
- Install the disk drive assembly.

Backplane Board Installation (85)

- Place the backplane board (85) in the chassis so that the end with the power connector is towards the power supply (95).
- Secure the backplane board with six screws (90), and plug the power supply connector (95A) into the backplane power receptacle.
- Install any optional cards and secure with screw (60).
- Install memory card (75) and secure with screw (60).
- Install system CPU card (70) and secure with screw (60).
- Plug the speaker connector into the system CPU card (70).
- Install video/color/composite card (65) and secure with screw (60).
- Install floppy disk controller card (55) and secure with screw (60).
- Connect cable assembly (50) to the floppy disk controller card (55).
- Install the top cover by carefully lowering it onto the base unit while positioning the front lip under the edge of the front panel (115), and the bottom tabs inside the base unit. As you are lowering the top cover, route the disk drive power cables (95A and 95B) and the disk controller data cable (50) through the center slot at the back of the cover. Secure with four screws (10).
- Install the disk drive assembly.

Optional Card(s) Installation

- Install optional card(s) and secure with screw(s) (60).
- Install the top cover by carefully lowering it onto the base unit while positioning the front lip under the edge of the front panel (115), and the bottom tabs inside the base unit. As you are lowering the top cover, route the disk drive power cables (95A and 95B) and the disk controller data cable (50) through the center slot at the back of the cover. Secure with four screws (10).
- Install the disk drive assembly.

Memory Card Installation (75)

- Install memory card (75) and secure with screw (60).
- Install the top cover by carefully lowering it onto the base unit while positioning the front lip under the edge of the front panel (115), and the bottom tabs inside the base unit. As you are lowering the top cover, route the disk drive power cables (95A and 95B) and the disk controller data cable (50) through the center slot at the back of the cover. Secure with four screws (10).
- Install the disk drive assembly.

System CPU Card Installation (70)

- Install system CPU card (70) and secure with screw (60).
- Connect speaker cable to the system CPU card (70).
- Install the top cover by carefully lowering it onto the base unit while positioning the front lip under the edge of the front panel (115), and the bottom tabs inside the base unit. As you are lowering the top cover, route the disk drive power cables (95A and 95B) and the disk controller data cable (50) through the center slot at the back of the cover. Secure with four screws (10).
- Install the disk drive assembly.

Video/Color/Composite Card Installation (65)

- Install video/color/composite card (65) and secure with screw (60).
- Install the top cover by carefully lowering it onto the base unit while positioning the front lip under the edge of the front panel (115), and the bottom tabs inside the base unit. As you are lowering the top cover, route the disk drive power cables (95A and 95B) and the disk controller data cable (50) through the center slot at the back of the cover. Secure with four screws (10).
- Install the disk drive assembly.

Floppy Disk Controller Card Installation (55)

- Install floppy disk controller card and secure with screw (60).
- Connect cable assembly (50) to the front plug on the floppy disk controller card (55).
- Install the top cover by carefully lowering it onto the base unit while positioning the front lip under the edge of the front panel (115), and the bottom tabs inside the base unit. As you are lowering the top cover, route the disk drive power cables (95A and 95B) and the disk controller data cable (50) through the center slot at the back of the cover. Secure with four screws (10).
- Install the disk drive assembly.

Disk Drive Assembly Installation

- While holding the disk drive assembly at a right angle to the base unit, lower the assembly onto the back of the base unit, engaging the hinges with the holes at the rear of the base unit.
- While supporting the unit in the vertical position, connect two power connectors (390A and 390B), one data cable (50), and one ground strap (51).
- Position the cables and the connectors so the disk drive assembly can be lowered down onto the base unit.
- While taking care not to pinch any of the cables at the rear of the unit, carefully pivot the disk drive assembly down onto the base. Push the front supports back as the drive is lowered to the operating position, and guide the ends of the front supports into the holes in the top of the base.

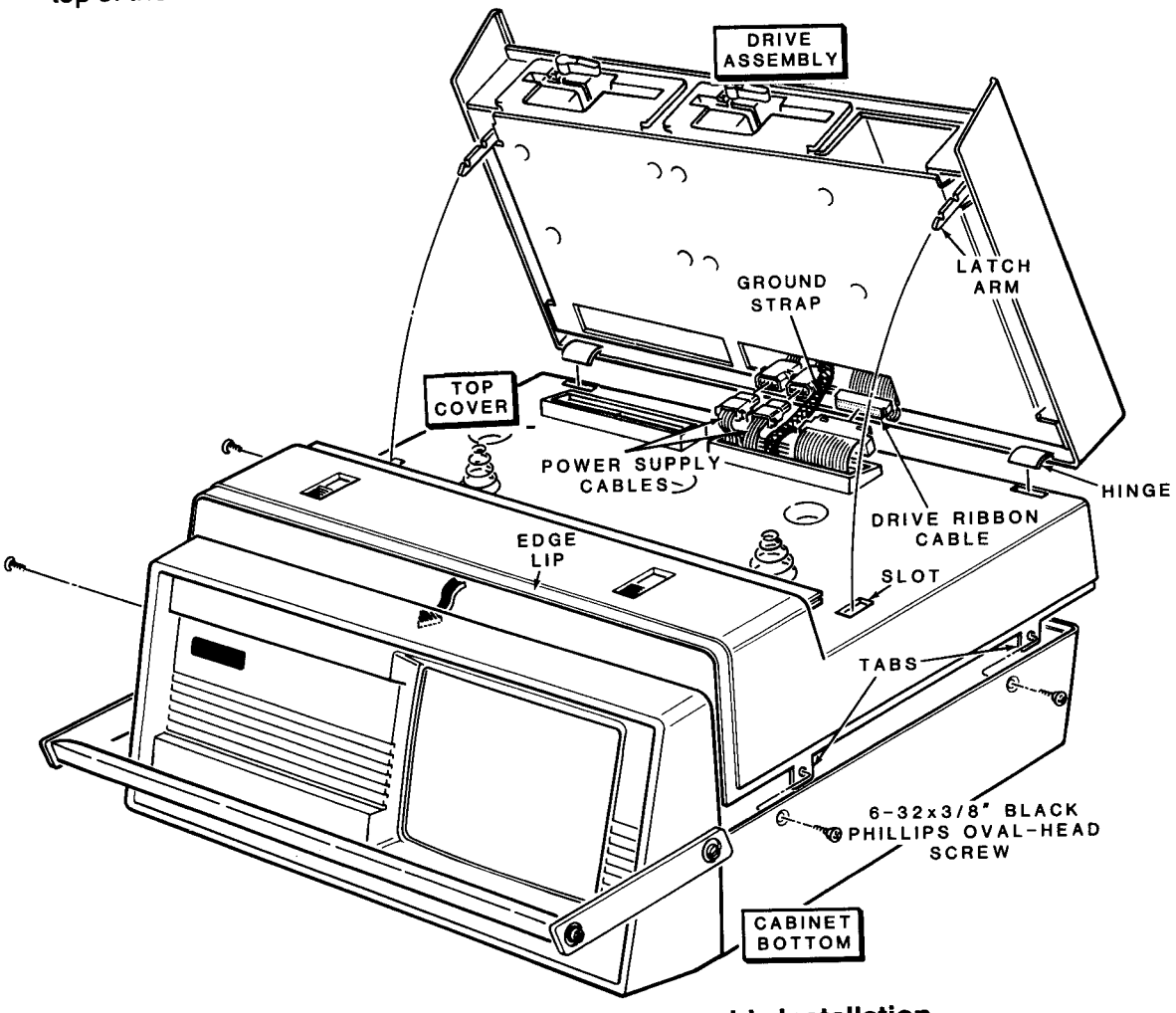

Figure 6.1. Disk Drive Assembly Installation

Chapter 7

Parts List

Introduction

This chapter includes two exploded views of the Z-160 Portable Personal Computer and an accompanying parts list to assist in the identification of replacement parts. Adjacent to the exploded view item numbers on the parts list are the part number and description which must be supplied when ordering the replacement part. Refer to the appropriate card service module if a card component is to be replaced.

Z-160 Computer Parts List

The Z-160 Computer is Part Number HE 181-5150. Refer to the foldouts, at the end of this module for identification of replacement parts.

ITEM NUMBER	ZDS PART NUMBER	DESCRIPTION
5	HE 92-840	Cabinet top
10	HE 250-1515	Screw, oval, Phillips 6-C × .750″
15	HE 258-758	Spring spiral
20	HE 94-640	Disk door
25	HE 252-178	Nut, push on
30	HE 204-2800	Bracket, board support
35	HE 250-1285	Screw, panhead Phillips 6-AB × .375″
40	HE 73-142	Foam
45	HE 73-203	Insulator
50	HE 134-1325	Cable assembly, floppy disk
55	HE 181-4647	Floppy disk controller card
60	HE 250-1325	Screw, panhead, Phillips 6-32 × .250″
65	HE 181-4937	Video/color/composite card
70	HE 181-4646	System CPU card
	or	
	HE 181-5326	System CPU card
75	HE 181-4648	128K memory card
	or	
	HE 181-4931-1	192K memory card
	or	
	HE 181-5304	256K memory card
	or	
	HE 181-5324	320K memory card

ITEM NUMBER	ZDS PART NUMBER	DESCRIPTION
80	HE 204-2721	Bracket, blank
85	HE 181-4936	Backplane board
90	HE 250-1280	Screw, panhead, Phillips 6-32 × .375″
95	HE 234-434	Power supply
100	HE 252-756	Nut, hex lock 6-32 × .312″
105	HE 204-2846	Bracket, air blockage
110	HE 73-199	Insulator
115	HE 92-814	Cabinet front
120	HE 250-1310	Screw, slotted 8-32 × .750″
125	HE 255-823	Spacer
130	HE 462-330	Knob
145	HE 10-1192	Linear, control 500 Ω
150	HE 252-159	Nut
155	HE 254-14	Washer
160	HE 6-560-12	Resistor, 56 Ω
165	HE 205-1924	Plate
170	HE 301-2	Sheet, aluminum
175	HE 250-1409	Screw, panhead, Phillips 4-BT × .375″
180	HE 234-196	CRT
185	HE 250-1264	Screw, slotted 8-32 × .375″
190	HE 354-45	Washer, flat #8

Parts List

ITEM NUMBER	ZDS PART NUMBER	DESCRIPTION
195	080-02377	CRT ground clip
200	HE 181-5149	CRT video deflection/driver board assembly
205	HE 92-821	Cabinet bottom
210	HE 252-760	Nut, hex locking
215	HE 75-710	Insulator spacer
220	HE 94-647	Handle end
225	HE 250-1505	Screw, Phillips 10-32 × .625"
230	HE 253-98	Washer #10
235	HE 255-825	Spacer
240	HE 253-86	Washer
245	HE 253-71	Washer, spring
250	HE 211-93	Handle
255	HE 250-1504	Screw 10-B × 1.000
260	HE 401-176	Speaker
265	HE 134-1449	Speaker cable
270	HE 73-124	Grommet
275	HE 204-2761	Bracket, front
280	HE 74-41	Foam tape
285	HE 94-641	5-section card guide
290	HE 94-642	3-section card guide
295	HE 181-5148	Contrast cable
300	HE 252-758	Nut, grip
305	HE 204-2762	Cover mounting bracket
310	HE 75-710	Insulator spacer
315	HE 134-1455	Cable assembly (video)
320	HE 200-1485-1	Chassis
325	HE 92-819	Top, disk drive
330	HE 250-1322	Screw 6-BT × .625"
335	HE 255-46	Hinge, half
340	HE 207-71-1	Chassis, base
345	HE 150-163 or HE 150-168 or HE 150-192	5-1/4, 1/2-height drive, Shugart 5-1/4, 1/2-height drive, Mitsubishi 5-1/4, 1/2-height drive, Matsushita (JA 551-2)
350	HE 810-8 or HE 250-1280	Screw, metric (Shugart drive) Screw, 6-32 × .375 (Mitsubishi drive)
355	HE 73-6	Grommet
360	HE 255-822	Spacer
365	HE 94-646	Storage box
370	HE 258-761	Spring
375	HE 94-639	Latch arm
380	HE 253-21	Washer #6
385	HE 258-757	Spring, expansion
390	HE 134-1476	Cable assembly, drive power extension
395	HE 134-1490	Cable assembly, disk drive data
400	HE 181-4935	Keyboard
405	HE 134-1397	Cable assembly, coiled keyboard
410	HE 89-65	Line cord
415	HE 250-1431	Screw, flat Phillips 6-AB × .375
420	HE 432-1077	Ground connector, 2-terminal
425	HE 252-3	Nut, hex head 6-32
430	HE 254-1	Washer, #6 internal tooth
435	HE 181-5106-1	Resistor/cable assembly
440	HE 92-815	Cover, front storage compartment
445	HE 134-1460	Cable assembly, disk drive extension

SERVICE MODULE

Power Supply

Z-100 PC Series Computers

585-60-01

860-45

ZENITH data systems

The purpose of this page is to make sure that all service bulletins are entered in this manual. When a service bulletin is received, annotate the manual and list the information in the record below.

Record of Service Bulletins

SERVICE BULLETIN NUMBER	DATE OF ISSUE	CHANGED PAGE(S)	PURPOSE OF SERVICE BULLETIN	INITIALS

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Abbreviations

CSA	Canadian Standards Association
FCC	Federal Communications Commission
KHz	Kilohertz
ms	millisecond
mV	millivolt
PSG	Power Supply Good
TTL	Transistor-Transistor Logic
UL	Underwriters Laboratories
VAC	Voltage Alternating Current
VDC	Voltage Direct Current
VDE	German Engineers Association

Chapter 1

Introduction and Specifications

Introduction

WARNING: Do not attempt to service the power supply. Serious or fatal injury may result.

This module provides information on the power supply. The power supply as a unit is **NOT SERVICEABLE.** The power supply contains proprietary information. Therefore, there is no disassembly, parts list, reassembly, or schematic included with this module. The specifications for the power supply are listed below.

Specifications

Part Number:	HE 234-434.
AC Input:	100-130 VAC, 60 Hz. 200-260 VAC, 50 Hz. Switch selectable.
DC Outputs:	+5 V (±3%), +12 V (+5, −4%), −12 V (+5, −4%).
Temperature Range:	10 to 32°C. 47 to 89°F.

Chapter 2

Configuration

Refer to Figure 2.1 while reading the following.

The voltage switch at the rear of the computer is located through the small window on the power supply that is covered with plastic. The voltage switch is normally set for 115 VAC. If this computer is to be operated on 240 VAC line voltage, use a small-bladed screwdriver and break the plastic window over the 115 VAC position of the switch. Then slide the switch so that 240 VAC is visible on the switch. Connect the appropriate line cord.

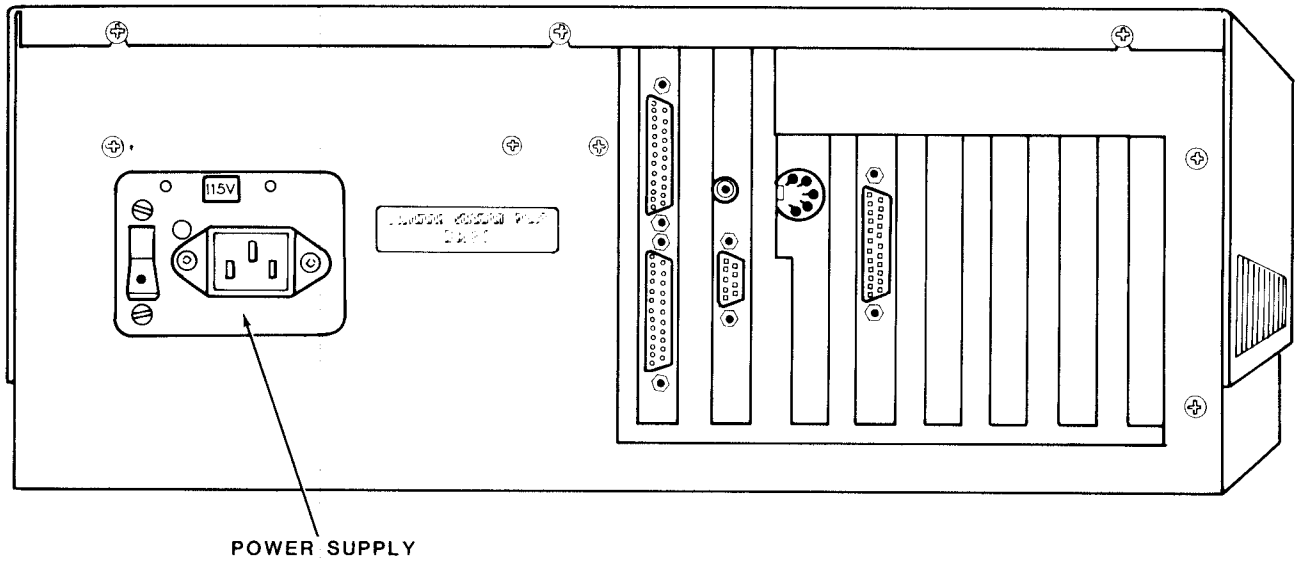


Figure 2.1. Power Supply Rear View

Chapter 3

Theory of Operation

Introduction

Refer to Figure 3.1 while reading the following.

The power supply provides regulated voltages used by the various components within the Z-100 PC Series Computers. The power supply is located toward the rear and to the right of the chassis, and uses a quasi square wave switching regulator to produce three regulated output voltages. This unit complies with FCC, VDE, CSA, and UL regulations.

Outputs

All outputs from the precision-regulated power supply are electrically isolated from the main voltage and share a common ground, which is the chassis of the power supply.

The voltages output to disk drive connectors P1 and P2 have special requirements for output ripple frequency components in the frequency range of 60 to 120 KHz. To obtain these low levels, a low pass filter is added to the regular output leads of P1 and P2. The output ripple is measured with an oscilloscope with a bandwidth of 3 KHz. Component frequency of the output ripple of the 5-volt or 12-volt outputs should **NOT** exceed 2 mV peak between the frequencies of 60 KHz to 120 KHz. Connector P3 supplies the output voltages to the backplane board.

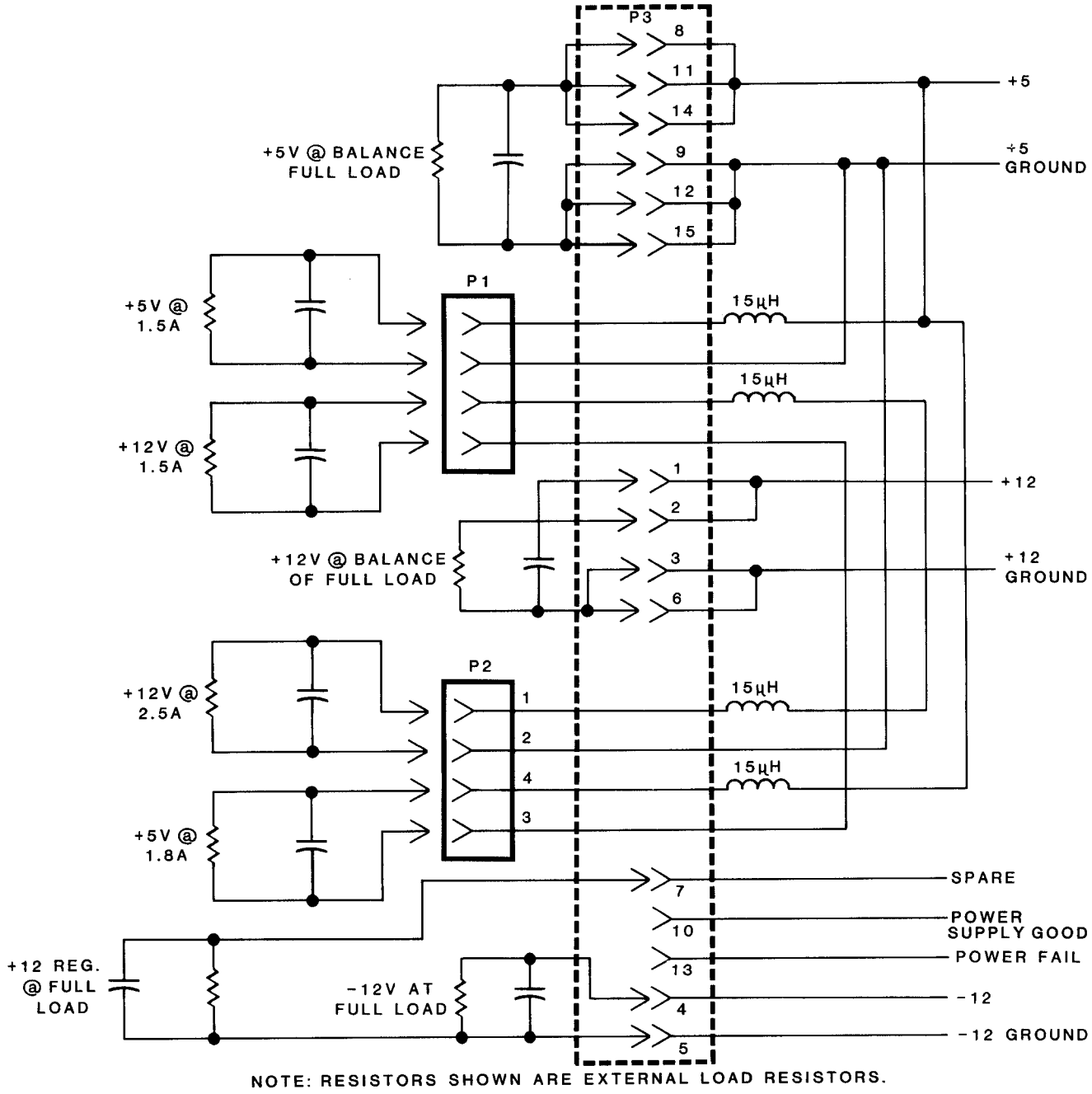


Figure 3.1. Power Supply Output

Power Supply Good (PSG) Signal

The PSG logic signal is an open collector TTL-compatible output which is used by external circuits to determine if the output voltages are valid and within specification. Upon power up, PSG shall remain high until all the DC output voltages stay within specification for a minimum of 70 to 130 ms, after which time PSG will go low. If any voltage is not within this normal limit plus 1% of nominal voltage (refer to Specifications), PSG will go high. PSG will not return to a low condition until outputs have met the same conditions as those required at initial power application.

Operation at No Load

The power supply is capable of operating under the adverse condition of no load without damage. If the power supply shuts down, it will require a manual reset by turning the power supply off, waiting 5 seconds, and then turning it back on. The output voltage may seek a value between ground and 50% over nominal. Output voltages will not exceed the peak rating of the output circuit components.

Chapter 4

Troubleshooting

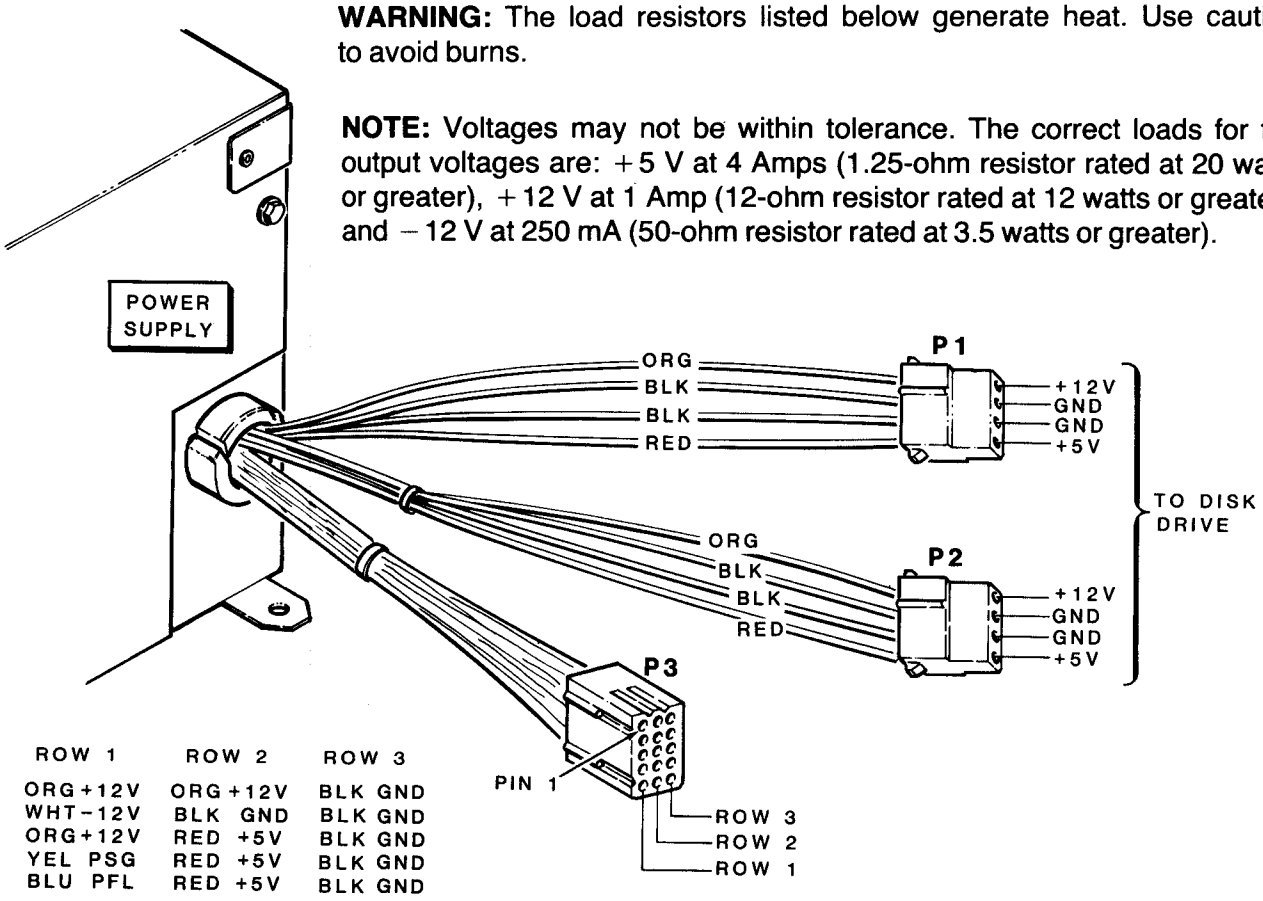
Refer to Figure 4.1 while reading the following.

Measure the power supply outputs with the disk drive connectors disconnected, and connector P3 connected to the backplane board. Measure the voltages at the test points on the backplane board, and refer to Figure 4.1 for the power supply voltages.

Measure the ripple voltage with an oscilloscope. If the power supply voltages are normal, measure the voltage with the disk drives connected. This will indicate if the circuit cards or disk drives are loading down the power supply.

WARNING: The load resistors listed below generate heat. Use caution to avoid burns.

NOTE: Voltages may not be within tolerance. The correct loads for the output voltages are: +5 V at 4 Amps (1.25-ohm resistor rated at 20 watts or greater), +12 V at 1 Amp (12-ohm resistor rated at 12 watts or greater), and −12 V at 250 mA (50-ohm resistor rated at 3.5 watts or greater).



ROW 1	ROW 2	ROW 3
ORG +12V	ORG +12V	BLK GND
WHT −12V	BLK GND	BLK GND
ORG +12V	RED +5V	BLK GND
YEL PSG	RED +5V	BLK GND
BLU PFL	RED +5V	BLK GND

Figure 4.1. Power Supply Connectors

SERVICE MODULE

Backplane Board

Z-100 PC Series Computers

585-64-01

860-45

ZENITH data systems

The purpose of this page is to make sure that all service bulletins are entered in this manual. When a service bulletin is received, annotate the manual and list the information in the record below.

Record of Service Bulletins

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Abbreviations

CLK	Clock
CPU	Central Processing Unit
DC	Direct Current
DMA	Direct Memory Access
GND	Ground
I/O	Input/Output
LED	Light-Emitting Diode
mA	Milliamperes
MHz	Megahertz
NMI	Non-Masked Interrupt
ns	nanosecond
PSG	Power Supply Good
ROM	Read-Only Memory
VDC	Volts Direct Current

Chapter 1

Introduction and Specifications

Introduction

The backplane board in the Z-100 PC Series Computer contains five supply voltage diagnostic LEDs, a −5 VDC regulator, and the eight IBM®-compatible bus connectors, P101 through P108, into which the remainder of the computer's cards are inserted for intersystem communication. A power supply interface connector, P110, and a +12 VDC connector, P109, also are contained on this board. P109 supplies +12 VDC to an internal video monitor on some models.

Diagnostics

The LEDs on the backplane board aid the user in determining whether or not a fault lies in the DC power generation circuits. The five LEDs on this board indicate the overall integrity of the power supply, and the presence or absence of the four individual operating supply voltages: +12 VDC, −12 VDC, +5 VDC, and −5 VDC.

−5 Volt Regulator

The only supply voltage actually generated on this board is the −5 VDC. The specifications for this supply are as follows:

- **Input:** −7.3 to −25 VDC, filtered by 2.2 μF.
- **Output:** −4.8 to −5.2 VDC, at 100 mA, filtered by 47 μF.
- **Load:** 1 mA to 100 mA, short-circuit protected.
- **Ambient Temperature:** 0 to +70°C.
  32 to 158°F.

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Signal Bus

The eight-connector array on this board is basically an input/output (I/O) extension of the microprocessor bus. The bus interface is implemented via a 62-pin edge connector on the card or device which plugs into one of the eight backplane sockets. The bus supplies the following:

- Eight bits of bidirectional data;
- Twenty address lines to access up to 1 megabyte of memory. The maximum user memory is 640K of 64K devices, or 768K using 256K devices;
- Six levels of interrupt;
- Control lines for memory and I/O read and write;
- Clock and timing control lines;
- A channel check line for device error reporting or parity error reporting by existing and add-on memory. A non-masked interrupt (NMI) is supplied to the central processing unit (CPU) when this line is active;
- Operating power consisting of + and −5 VDC, + and −12 VDC, and ground;
- An I/O CH RDY line for use by slow acting peripherals;
- Capability of addressing up to 64K I/O ports;

A complete listing of the signal names and their functions is presented in the "Detailed Circuit Description," Chapter 3.

Chapter 2

Theory of Operation

Refer to Figure 2.1, the backplane board block diagram, for the following description.

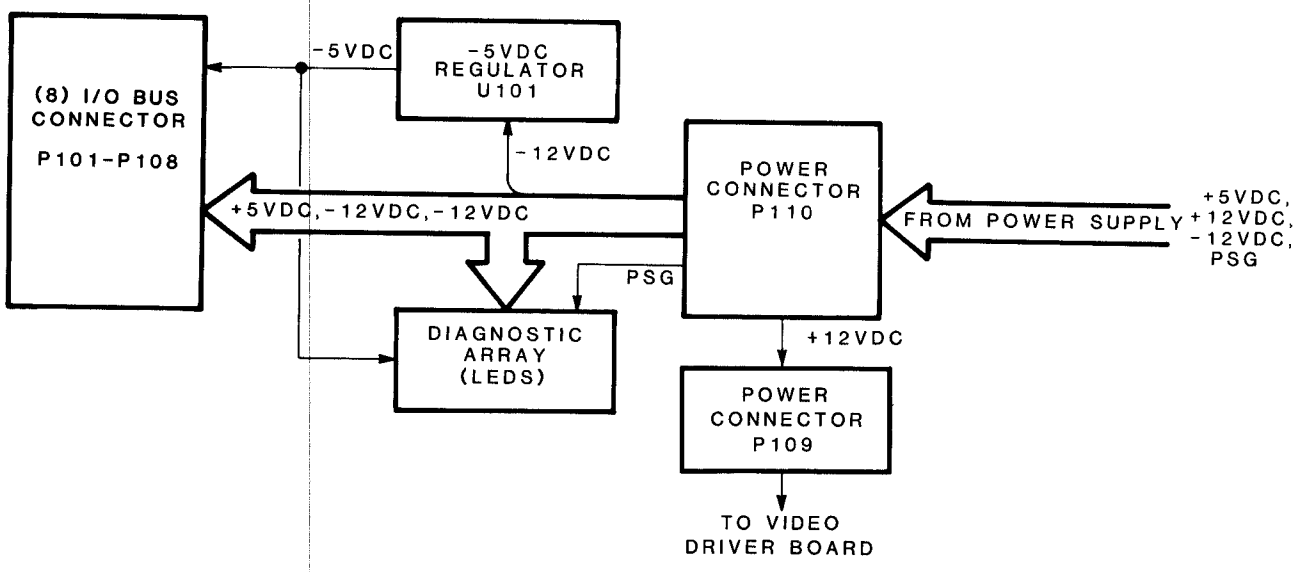


Figure 2.1. Backplane Board Block Diagram

Power Connector

P110 from the power supply delivers the operating supply voltages for the cards which plug into the backplane board connectors, and for the diagnostic LED array contained on the backplane board. System ground, +5 VDC, +12 VDC, and −12 VDC are routed to the backplane board by this connector. To increase the current carrying capability on the heavier loaded supply busses and the ground return, more than one pin on the connector is used for the same supply bus. Ground and +5 VDC are contained in the middle layer of the printed circuit board.

P109 supplies +12 VDC to the video driver board.

−5 Volt Regulator

The −5 volt supply is derived from −12 VDC from the power supply, which is applied to a solid-state voltage regulator, U101. The −5 VDC is then applied to the parallel bus connectors, and to its respective diagnostic LED circuit.

Diagnostic LEDs

Five green light-emitting diodes (LEDs) are incorporated to indicate the power supply is good, and the presence or absence of +5 VDC, −5 VDC, +12 VDC, and −12 VDC. Suitable current-limiting resistors are connected inline with the LEDs to provide the appropriate operating voltage and current to the devices. The LEDs are on (lit) when the parameter associated with a device is at or near its stated value, and off when the associated parameter is deficient.

Backplane I/O Connectors

Eight 62-pin edge-type socket connectors are provided by the backplane board to interconnect the CPU card, the memory card, the video card, and the disk controller card with the appropriate edge connector, as well as any other cards which may be added for system enhancement or expansion. The optional connectors are identical and are wired in parallel so that, functionally, any card may be inserted at any connector location.

Chapter 3

Detailed Circuit Description

Refer to the backplane board schematic for the following circuit description.

Power Distribution

P110, the backplane power connector, connects +5 VDC, +12 VDC, − 12 VDC, the power supply good (PSG) signal, and ground to the backplane board. Ground is connected to pins 3, 5, 6, 9, 12, and 15. +5 VDC comes in on pins 8, 11, and 14. −12 VDC appears on pin 4. +12 VDC is applied to pins 1 and 2. The PSG signal is on pin 10. Pins 7 and 13 are not used.

+5 VDC, +12 VDC, and −12 VDC are fed through to B3, B9, and B7, respectively, on the parallel signal bus connectors, P101 through P108, and also are applied to their respective LEDs. −12 VDC also is fed to the input, pin I of U101, the −5 VDC regulator. Ground (GND) is routed to the signal bus, pins B1, B10, and B31. The PSG signal is connected to the cathode of D104, the PSG LED.

−5 VDC Regulation

U101, the −5 volt regulator, accepts the −12 VDC on its input, drops and regulates it, and sends the −5 VDC output, pin O, to bus pin B5, and to R101, the dropping resistor for the −5 volt LED. The G pin of U101 connects to system ground to serve as a return path for the regulator circuit. C119 and C117 filter and decouple the −12 VDC input. C118 filters the −5 VDC output to reduce the ripple to an acceptable level.

Diagnostic Circuitry

The diagnostic LEDs, D101 through D105, indicate the integrity of the four DC voltages and the PSG signal. R101 through R105 act as voltage-dropping and current-limiting resistors to obtain the 2.5 volts, 20 mA required for safe illumination of the LEDs. R101 and R102 connect to the cathodes of D101 and D102, while the anodes are returned to ground, the proper configuration for sensing of negative-polarity voltages. R103 and R105 connect to D103 and D105 anodes, and the cathodes return to ground, to properly sense the +5 and +12 VDC signals.

+5 VDC is connected to R104, which is, in turn, series-connected to the anode of D104, the PSG LED. Upon power up, a few hundred milliseconds are allowed to stabilize the power supply outputs. Up until this point, pin 10 of P110, which is also the cathode of D104, is at approximately +5 VDC, keeping the LED extinguished. If at the end of the delay time all the supply voltages are normal, sensing circuitry in the power supply pulls pin 10 nearly to ground potential, lighting D104 to indicate proper power supply operation.

Signal Bus

The signal bus consists of eight identical 62-pin edge connector sockets, P101 through P108. The connectors are arranged with 31 pins labeled A1 through A31 on one side, and 31 pins labeled B1 through B31 on the other. There is a one-to-one electrical correspondence between identical pin numbers on each connector.

Capacitors C101, C103, C105, C107, C110, C112, C114, and C116 are connected between +5 VDC and ground as filtering. They are physically located between every other pair of backplane signal connectors at the top and bottom of the board.

Table 3.1 defines the signals which appear on the backplane signal bus connectors.

Table 3.1. I/O Bus Signal Names

PIN	SIGNAL	DEFINITION
A1	I/O CHCK*	I/O channel check. Provides the CPU with parity error status for memory or other I/O devices. Active-low indicates error.
A2	D7	Data bit 7
A3	D6	Data bit 6
A4	D5	Data bit 5
A5	D4	Data bit 4
A6	D3	Data bit 3
A7	D2	Data bit 2
A8	D1	Data bit 1
A9	D0	Data bit 0
A10	I/O CHRDY	I/O channel ready. Used by slower peripherals to ensure data is not lost during read and write operations. May be held low (not ready) up to 10 CLK cycles (2.1 μs).
A11	AEN	Address enable. Assigns control of read and write operations to the DMA controller.
A12	A19	Address bit 19
A13	A18	Address bit 18
A14	A17	Address bit 17
A15	A16	Address bit 16
A16	A15	Address bit 15
A17	A14	Address bit 14
A18	A13	Address bit 13

Table 3.1 (Continued). I/O Bus Signal Names

PIN	SIGNAL	DEFINITION
A19	A12	Address bit 12
A20	A11	Address bit 11
A21	A10	Address bit 10
A22	A9	Address bit 9
A23	A8	Address bit 8
A24	A7	Address bit 7
A25	A6	Address bit 6
A26	A5	Address bit 5
A27	A4	Address bit 4
A28	A3	Address bit 3
A29	A2	Address bit 2
A30	A1	Address bit 1
A31	A0	Address bit 0
B1	GND	Ground
B2	RESET	When high, resets, or initializes system logic devices.
B3	+5 VDC	+5 VDC bus
B4	IRQ2	Interrupt request 2. Not used, but available for assignment to a user-selected device.
B5	−5 VDC	−5 VDC bus
B6	DRQ2	DMA request 2. Assigned to floppy disk controller.

Table 3.1 (Continued). I/O Bus Signal Names

PIN	SIGNAL	DEFINITION
B7	−12 VDC	−12 VDC bus
B8	N.C.	No connection
B9	+12 VDC	+12 VDC bus
B10	GND	Ground
B11	MEMW*	Memory write. When low, causes data on data bus to be stored in memory.
B12	MEMR*	Memory read. When low, causes memory to drive data onto the data bus.
B13	IOW*	I/O write. When low, instructs an I/O device to read the data on the data bus.
B14	IOR*	I/O read. When low, instructs an I/O device to drive its data onto the data bus.
B15	DACK3*	DMA acknowledge 3. Assigned to the Winchester drive controller.
B16	DRQ3	DMA request 3. Assigned to the Winchester drive controller.
B17	DACK1*	DMA acknowledge 1. Not used. Available for user assignment.
B18	DRQ1	DMA request 1. Available.
B19	DACK0*	DMA acknowledge 0. Assigned to timer #1. Initiates memory refresh cycle.
B20	CLK	System clock 4.77 MHz.
B21	IRQ7	Interrupt request 7. Assigned to parallel interface.
B22	IRQ6	Interrupt request 6. Assigned to floppy disk controller.

Table 3.1 (Continued). I/O Bus Signal Names

PIN	SIGNAL	DEFINITION
B23	IRQ5	Interrupt request 5. Assigned to Winchester drive controller.
B24	IRQ4	Interrupt request 4. Assigned to serial port #1 (fixed).
B25	IRQ3	Interrupt request 3. Assigned to serial port #2 (configurable).
B26	DACK2*	DMA acknowledge 2. Assigned to floppy disk controller.
B27	T/C	Terminal count. Goes high when terminal count for any DMA channel is reached.
B28	ALE	Address latch enable. Generated by bus controller to indicate valid processor addresses to the I/O channel.
B29	+5 VDC	+5 VDC bus.
B30	OSC	Oscillator. A high-speed clock: 14.31818 MHz. Provides the basic timing for the system.
B31	GND	Ground.

Chapter 4

Troubleshooting

General Troubleshooting

If you have encountered problems with the computer and indications point to the backplane board as the source of the difficulty, proceed to isolate the fault in the following manner.

If a spare backplane board is available, attempt to clear the problem by direct substitution of the board. If the difficulty does not reappear, the removed backplane board is at fault.

If a backup backplane board is not available, attempt to isolate the fault by the step-by-step checks which follow. Fault-isolation is divided into two categories: power supply related problems, and signal bus problems.

DC Voltages and Diagnostics

If one or more of the backplane LEDs is extinguished, it may indicate a power supply or −5 volt regulator problem, or that the LED itself is defective.

If you suspect that one or more of the DC voltages is absent or deficient, use a voltmeter and make the following checks. The computer must be on, and the meter set to a suitable range for the voltage being measured.

DC Voltage Checks

Turn the computer on and perform the following:

1. Connect the common lead of the voltmeter to ground by connecting it to one of the ground pins on P110: pin 3, 6, 5, 9, 12, or 15.

2. Set the polarity of the meter to positive and probe pin 1 of P110. Meter should read +12 VDC (+5%, −4%).

3. Probe pin 10 of P110. Voltage should be +5 VDC (±3%).

4. Set the polarity of the meter to negative and probe pin 4 of P110. Voltage should be −12 VDC (+5%, −4%).

If any of the voltages are missing or low, the power supply is suspect. Refer to the troubleshooting section of the power supply module.

If a voltage is present, but its LED is not lit, perform the following steps:

1. Turn off the computer, and set the meter to read ohms. Check the value of the resistor associated with the LED that was out. R102 and R103 should read approximately 1500 ohms, and R105 should read 560 ohms.

2. If the resistor checks good, replace the LED in question.

If the previous checks do not indicate a problem, perform the following checks:

1. Set the voltmeter to read negative polarity, and turn the computer back on.

2. Probe pin O (output) of U101. Meter should read approximately −5 VDC (±5%). If it does not, replace U101. If replacing U101 does not restore −5 VDC, check the other components associated with U101: C117, C118, and C119.

3. If −5 VDC is present but D101 is not lit, perform LED checks as outlined previously.

Check the PSG signal. If the power supply is functioning properly, there should be approximately zero volts on pin 10 of P110, and D104 should be lit. If zero volts is indicated but PSG LED is not lit, turn off the computer and check the resistance of R104 with an ohmmeter. It should read 560 ohms. If the resistor checks good, replace D104.

If the power supply checked good and one or more of the voltages is now deficient, the supply is, more than likely, being loaded down by one of the cards. Remove the cards one at a time until the deficient voltage returns to normal, then refer to the troubleshooting section for that card.

Backplane Connector Fault Isolation

If you have reason to suspect a defective backplane signal bus connector of causing a problem, perform the following:

1. Turn off the computer, and swap cards in the suspect location; e.g., remove the video card and replace it with the CPU card.

2. Turn the computer back on and perform several operations to determine if the problem still is present, or has changed in nature.

If the same problem still is present, it is probable that the cause is on a card whose function is related to the nature of the problem. Consult the troubleshooting section for the affected card.

If the nature of the difficulty has changed, try to relate the symptoms to the particular cards used in a given location to pinpoint the defective backplane connector.

Once the suspect location has been determined, turn off the computer and visually inspect the edge connector in that location for physical damage, poor solder connections, corroded contacts, etc. If no discrepancy is noted, connector replacement is indicated.

Chapter 5

Parts List

Introduction

Contained in this chapter are a component view of the backplane boards, part numbers HE 181-4656 and HE 181-4936, and the related parts list. Refer to Figure 5.1 for location of parts and components.

This chapter also includes a Semiconductor Identification Index for additional information on the semiconductor devices.

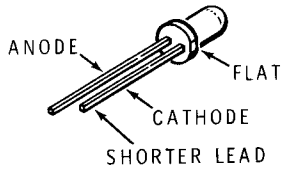
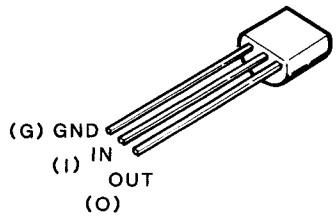
Component Parts List

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
Capacitors		
C101	HE 25-928	33 μF electrolytic
C102	Not Used	
C103	HE 25-928	33 μF electrolytic
C104	Not Used	
C105	HE 25-928	33 μF electrolytic
C106	Not Used	
C107	HE 25-928	33 μF electrolytic
C108	Not Used	
C109	Not Used	
C110	HE 25-928	33 μF electrolytic
C111	Not Used	
C112	HE 25-928	33 μF electrolytic
C113	Not Used	
C114	HE 25-928	33 μF electrolytic
C115	Not Used	
C116	HE 25-928	33 μF electrolytic
C117	HE 21-769	.01 μF ceramic
C118	HE 25-883	47 μF electrolytic
C119	HE 25-924	2.2 μF electrolytic
Diodes		
D101	HE 412-642	LED, 2.5 V, 20 mA
D102	HE 412-642	LED, 2.5 V, 20 mA
D103	HE 412-642	LED, 2.5 V, 20 mA
D104	HE 412-642	LED, 2.5 V, 20 mA
D105	HE 412-642	LED, 2.5 V, 20 mA

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
Integrated Circuits		
U101	HE 442-665	Regulator, voltage, −5 V
Interfaces		
P101	HE 432-1351	Connector, edge, 62-pin
P102	HE 432-1351	Connector, edge, 62-pin
P103	HE 432-1351	Connector, edge, 62-pin
P104	HE 432-1351	Connector, edge, 62-pin
P105	HE 432-1351	Connector, edge, 62-pin
P106	HE 432-1351	Connector, edge, 62-pin
P107	HE 432-1351	Connector, edge, 62-pin
P108	HE 432-1351	Connector, edge, 62-pin
P109	HE 432-943	Connector, 2-pin
P110	HE 432-1376	Connector, power, 15-pin
Resistors		
R101	HE 6-561-12	560 Ω, film
R102	HE 6-152-12	1500 Ω, film
R103	HE 6-152-12	1500 Ω, film
R104	HE 6-561-12	560 Ω, film
R105	HE 6-561-12	560 Ω, film

Semiconductor Identification Index

This section will aid you in identifying the semiconductor devices installed on the backplane board by cross referencing, where applicable, the Zenith/ Heath part numbers with generic device numbers. The components are listed in numerical order, along with any applicable device number and device lead configuration.

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
412-642	SG205D	D101-D105 Green LED 2.5 V, 20 mA	
442-665	79L05	U101 Voltage regulator – 5 VDC	

SERVICE MODULE

Keyboard

Z-150 PC Desktop Computers
Z-160 PC Portable Computers

585-61-04

860-45

ZENITH data systems

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Abbreviations

ASCII	American Standard Code for Information Interchange
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
Hex	Hexadecimal
I/O	Input/Output
LED	Light-Emitting Diode
LSB	Least-Significant Bit
mA	Milliampere
MSB	Most-Significant Bit
RAM	Random Access Memory
ROM	Read-Only Memory
VDC	Volts Direct Current

Chapter 1

Description and Specifications

Introduction

This service module provides keyboard information for the Z-150 PC Desktop Computer and the Z-160 PC Portable Computer. This chapter includes the description and specifications of the keyboard.

Description

Refer to Figure 1.1. The keyboard is packaged in a low-profile enclosure with a tilt adjustment for 5-degree (Z-150 only) or 15-degree orientations.

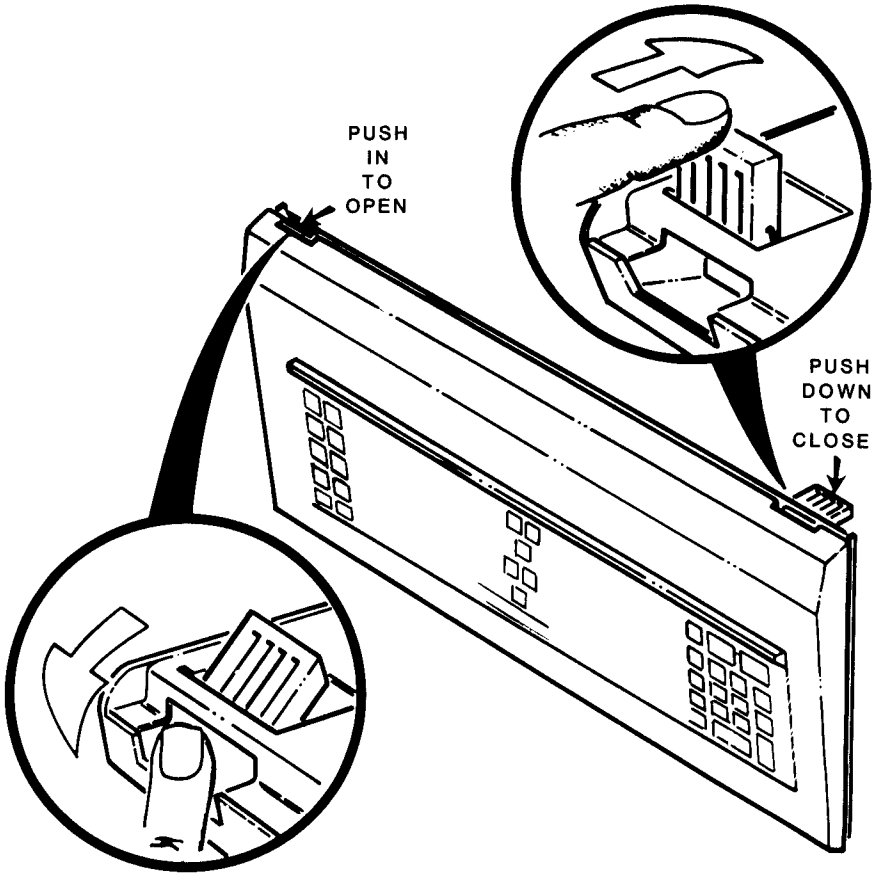


Figure 1.1. Z-150 Desktop Computer Keyboard

Description and Specifications

Refer to Figure 1.2. The keyboard contains 83 keys laid out in three major groupings. The central portion of the keyboard consists of a standard (QWERTY) typewriter keyboard layout. On the left side, arranged as a 2 × 5 block, are 10 function keys. These keys are user-defined by software. On the right side is a 16-key, keypad area. This area also is defined by software, but contains legends for the functions of numeric entry, cursor control, and calculator pad screen edit.

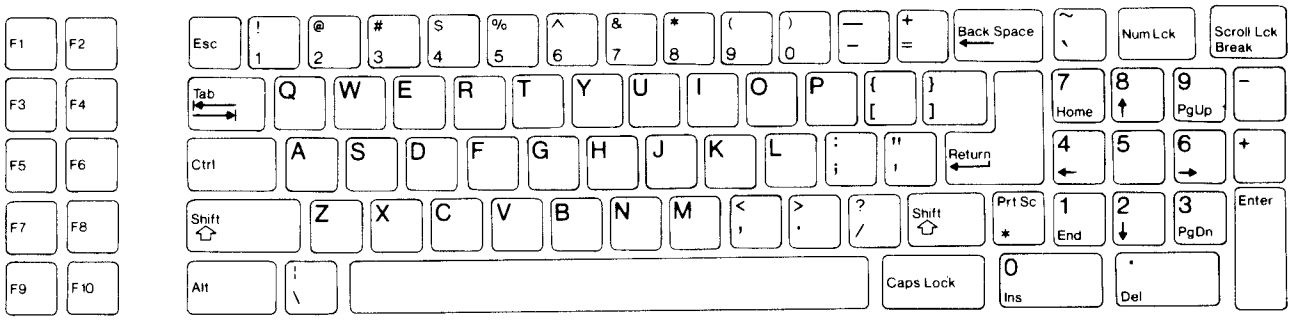


Figure 1.2. Keyboard Key View

The keyboard interface is defined so system software has the maximum flexibility in defining keyboard operation. This is accomplished by having the keyboard return specific hexadecimal (hex) codes rather than ASCII codes. In addition, all keys except control keys can be event driven and generate both make and break codes. For example, key 1 produces hexadecimal 01 when pressed and hexadecimal 81 when released. The keyboard input/output (I/O) driver can produce code either with or without control keys (SHIFT, CTRL, ALT) pressed, or under event driven conditions, as required by the application.

Specifications

Keys:	84 keys
Modes:	Extended function capabilities
Microprocessor:	8748 microcomputer or 8048 or 8031 (8048 emulator)
Operating Environment:	60° to 90°F (16° to 32°C) 10 to 80% relative humidity
Contacts:	Single-pole, single-throw
Maximum Ratings:	+5 VDC, 100 mA

Chapter 2

Installation and Configuration

Installation

Refer to Figure 2.1. The keyboard is attached to the Z-100 PC Series Computers via a coiled serial interface cable connected to the rear of the CPU card.

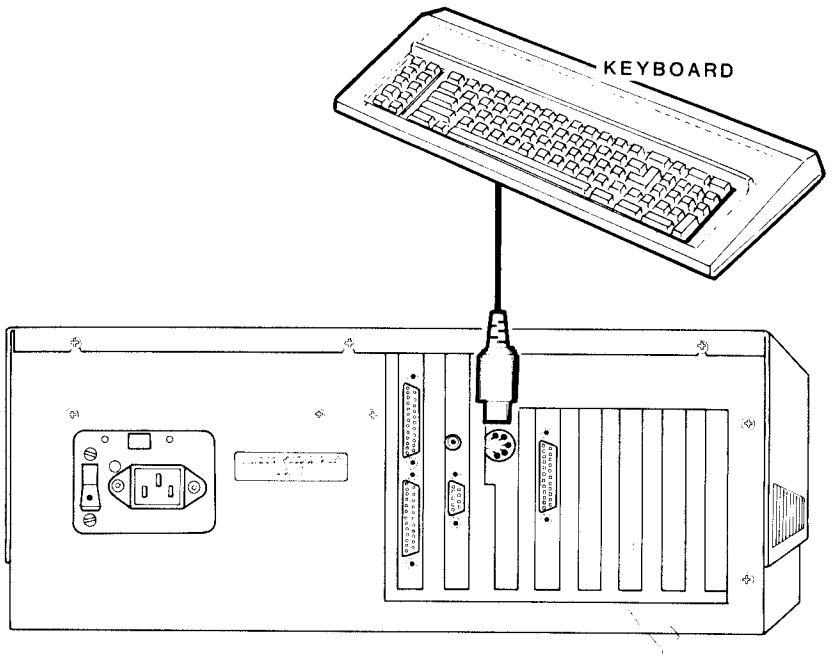


Figure 2.1. Keyboard Installation

NOTES:

1. The floppy disk serial I/O card may or may not have two serial connectors as shown in Figure 2.1.
2. The three-card computer design combines the floppy disk serial I/O card with the video card and will have one serial connector, one RGB connector, and one composite-monochrome video out jack (not illustrated).
3. The two-card computer design combines the memory-parallel output card with the CPU card. This new card (also not illustrated) will have the parallel connector and the keyboard connector on it.

Configuration

The keyboard cable is a coiled, shielded, five-wire cable. The cable interface contains power (+5 VDC), ground, two bidirectional signal lines, and a keyboard reset line (disabled). The cable is either permanently attached at the keyboard end and plugs into the CPU via a DIN connector, or is separate from the keyboard depending on the model (refer to "Parts List," Chapter 9).

Chapter 3

Operation

Keyboard Codes

The keyboard sends hex codes to the CPU card. Refer to Table 3.1 for the list of hex codes corresponding to the key(s) pressed.

For most keys, the value received will be the least-significant byte of the key code shown in the table. For instance, 2C7AH would be received as 7AH.

However, keys where the least-significant byte is 0 will generate two bytes, the first having a value of zero (0) to indicate a special key and the second being the code of the key itself. Thus, function key F10 (which generates 7100H in hardware) will generate 00H followed by 71H.

The table is arranged as follows: main keyboard by row, followed by function keys in order.

Table 3.1. Keyboard Codes (Hardware)

KEY	NOT SHIFTED	SHIFTED	CONTROL	ALT	CAPS LOCK
ESC	011BH	011BH	011BH	-----	011BH
! 1	0231H	0221H	-----	7800H	0231H
@ 2	0332H	0340H	0300H	7900H	0332H
# 3	0433H	0423H	-----	7A00H	0433H
$ 4	0534H	0524H	-----	7B00H	0534H
% 5	0635H	0625H	-----	7C00H	0635H
↑ 6	0736H	075EH	071EH	7D00H	0736H
& 7	0837H	0826H	-----	7E00H	0837H
* 8	0938H	092AH	-----	7F00H	0938H
(					

Table 3.1 (Continued). Keyboard Codes (Hardware)

KEY	NOT SHIFTED	SHIFTED	CONTROL	ALT	CAPS LOCK
9)	0A39H	0A28H	-----	8000H	0A39H
0 —	0B30H	0B29H	-----	8100H	0B30H
- +	0C2DH	0C5FH	0C1FH	8200H	0C2DH
= BACK SPACE ~	0D3DH 0E08H	0D2BH 0E08H	----- 0E7FH	8300H -----	0D3DH 0E08H
` NUM LCK SCROLL LCK	2960H -----	297EH -----	----- (Note 2)	----- -----	2960H -----
BREAK	-----	-----	(Note 3)	(Note 4)	-----
TAB	0F09H	0F00H	-----	-----	0F09H
Q	1071H	1051H	1011H	1000H	1051H
W	1177H	1157H	1117H	1100H	1157H
E	1265H	1245H	1205H	1200H	1245H
R	1372H	1352H	1312H	1300H	1352H
T	1474H	1454H	1414H	1400H	1454H
Y	1579H	1559H	1519H	1500H	1559H
U	1675H	1655H	1615H	1600H	1655H
I	1769H	1749H	1709H	1700H	1749H
O	186FH	184FH	180FH	1800H	184FH
P	1970H	1950H	1910H	1900H	1950H
{ [	1A5BH	1A7BH	1A1BH	-----	1A5BH
}]	1B5DH	1B7DH	1B1DH	-----	1B5DH
7 HOME	4700H	4737H	7700H	(Note 5)	4737H
8 (up arrow)	4800H	4838H	-----	(Note 5)	4838H
9 PGUP	4900H	4939H	8400H	(Note 5)	4939H
-	4A2DH	4A2DH	-----	-----	4A2DH
CTRL	-----	-----	-----	-----	-----
A	1E61H	1E41H	1E01H	1E00H	1E41H
S	1F73H	1F53H	1F13H	1F00H	1F53H
D	2064H	2044H	2004H	2000H	2044H

Table 3.1 (Continued). Keyboard Codes (Hardware)

KEY	NOT SHIFTED	SHIFTED	CONTROL	ALT	CAPS LOCK
F	2116H	2146H	2106H	2100H	2146H
G	2267H	2247H	2207H	2200H	2247H
H	2368H	2348H	2308H	2300H	2348H
J	246AH	244AH	240AH	2400H	244AH
K	256BH	254BH	250BH	2500H	254BH
L	266CH	264CH	260CH	2600H	264CH
: ;	273BH	273AH	-----	-----	273BH
" '	2827H	2822H	-----	-----	2827H
RETURN	1C0DH	1C0DH	1C0AH	-----	1C0DH
4 (left arrow)	4B00H	4B34H	7300H	(Note 5)	4B34H
5	-----	4C35H	-----	(Note 5)	4C35H
6 (right arrow)	4D00H	4D36H	7400H	(Note 5)	4D36H
+	4E2BH	4E2BH	-----	-----	4E2BH
(left) SHIFT	-----	-----	-----	-----	-----
Z	2C7AH	2C5AH	2C1AH	2C00H	2C5AH
X	2D78H	2D58H	2D18H	2D00H	2D58H
C	2E63H	2E43H	2E03H	2E00H	2E43H
V	2F76H	2F56H	2F16H	2F00H	2F56H
B	3062H	3042H	3002H	3000H	3042H
N	316EH	314EH	310EH	3100H	314EH
M	326DH	324DH	320DH	3200H	324DH
< ,	332CH	333CH	-----	-----	332CH
> .	342EH	343EH	-----	-----	342EH
? /	352FH	353FH	-----	-----	352FH
(right) SHIFT	-----	-----	-----	-----	-----
PRT SC *	372AH	(Note 1)	7200H	-----	372AH
1 END	4F00H	4F31H	7500H	(Note 5)	4F31H
2 (down arrow)	5000H	5032H	-----	(Note 5)	5032H
3 PGDN	5100H	5133H	7600H	(Note 5)	5133H
ENTER	540DH	540DH	540AH	-----	540DH

Table 3.1 (Continued). Keyboard Codes (Hardware)

KEY	NOT SHIFTED	SHIFTED	CONTROL	ALT	CAPS LOCK
ALT	-----	-----	-----	-----	-----
| \	2B5CH	2B7CH	2B1CH	-----	2B5CH
(space bar)	3920H	3920H	3920H	3920H	3920H
CAPS LOCK	-----	-----	-----	-----	-----
0 INS	5200H	5230H	-----	(Note 5)	5230H
DEL	5300H	532EH	-----	-----	532EH
F1	3B00H	5400H	5E00H	6800H	3B00H
F2	3C00H	5500H	5F00H	6900H	3C00H
F3	3D00H	5600H	6000H	6A00H	3D00H
F4	3E00H	5700H	6100H	6B00H	3E00H
F5	3F00H	5800H	6200H	6C00H	3F00H
F6	4000H	5900H	6300H	6D00H	4000H
F7	4100H	5A00H	6400H	6E00H	4100H
F8	4200H	5B00H	6500H	6F00H	4200H
F9	4300H	5C00H	6600H	7000H	4300H
F10	4400H	5D00H	6700H	7100H	4400H

NOTES:

1. Pressing SHIFT-PRT SC will cause the contents of the screen to be sent to the printer.
2. Pressing CTRL-NUM LCK will temporarily halt the execution of a program.
3. Pressing CTRL-BREAK will halt the execution of a program and exit back to the system. This key sequence sends a special code of 0000H.
4. Pressing ALT-BREAK will empty the keyboard (type ahead) buffer.
5. This function is used for entering special keycodes. If you want to enter a special keycode, press and hold the ALT key, and then enter the three-digit keycode (in decimal) on the numeric (calculator) portion of the keyboard. When you release the ALT key, the desired code will be generated. For example, to generate the hexadecimal code 7B (decimal 123), press and hold the ALT key, then enter 1, 2, and 3 on the calculator portion of the keyboard, then release the ALT key. The actual code generated will be preceded by 38H, the scan code of the ALT key. Therefore, the complete generated code for ALT-123 is 387BH.

Special Function Key Combinations

The following key combinations are used for special purposes by the computer firmware (MFM-150 monitor ROM).

CTRL-ALT-DEL:	Resets the computer.
CTRL-ALT-INS:	Returns control to the MFM-150 monitor.
CTRL-ALT-RETURN:	Enters the MFM-150 monitor debug program and displays the CPU register contents.
ESC:	Aborts booting of disk.

Chapter 4

Theory of Operation

Introduction

This chapter includes a brief theory of operation. If a more detailed circuit description is desired, refer to Chapter 5 of this module.

Theory of Operation

Refer to Figure 4.1. The keyboard uses a microcomputer (Intel 8048) performing the keyboard scan functions. Additional keyboard functions are: key debounce, buffering of up to 256 key scan codes, maintaining bidirectional serial communications with the CPU, and executing the handshaking protocol required by each code transfer.

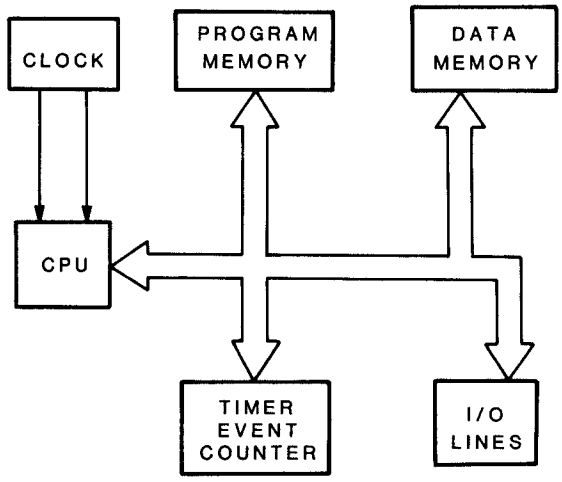


Figure 4.1. Keyboard Block Diagram

Chapter 5

Detailed Circuit Description

Introduction

This chapter provides a detailed circuit description and pin definitions of the microcomputer. Refer to the schematic while reading the following.

Circuit Description

The keyboard is a strobe scanning keyboard, controlled by microcomputer U107. U107 performs keyboard matrix scanning, setting and resetting of LEDs, actuation of the audio transducer, and serial communication with the computer.

All keys except NUM LCK (key 69) and CAPS LOCK (key 58) are configured in a general matrix consisting of 11 scan lines and 8 sense lines. A keyswitch and diode are arranged at each crossover point. The diodes prevent the generation of phantom keys due to multiple closures.

A 6.00 MHz crystal is connected between XTAL and XTAL 2 for the internal control and timing references of U107. Capacitors C1 and C2 are used for stability purposes.

Port bits P10 (LSB) through P13 (MSB) of U107 control the scan lines. The port bits drive U105 and U106 (dual one-of-four decoders) with the selected scan line being driven low. After setting a scan line, the sense lines are checked for a key closure.

Resistors R9 through R16 are used for pull-ups of the sense lines. The active low sense lines are buffered by U103 and U104 to provide static immunity for the microprocessor which is a NMOS device. The sense lines are read by bits D0 through D7.

The outputs P23 and P24, when directed by U107, are driven by U101, lighting the NUM LCK LED (key 69) and CAPS LOCK LED (key 58). Resistors R1 and R2 are LED bias resistors.

Port bit P22 drives the audio transducer, with U101 and R4 providing the current path. Diode D1 is used as a current shunt and R3 is the bias resistor.

U102 buffers the input/output data and clock. Resistors R5 and R6 are pull-up resistors for U102. Capacitors C3, C4, and C5 are line filters.

The KYBRST* line is tied high through resistor R7, thereby eliminating a keyboard hard reset.

J1 provides jumper selectability of either masked ROM (8048) or EPROM (8748) versions of U107. Production keyboards are jumpered for masked ROMs.

The filter of C6 through C14 provides the required filtering of the +5 VDC input.

Power of approximately 5 VDC is applied to the keyboard through pin 1.

Table 5.1. 8048/8748 Pin Definitions

DESIGNATION	PIN	DESCRIPTION
Vss	20	Circuit GND potential
Vdd	26	Low power standby pin
Vcc	40	Main power supply; +5 V during operation
PROG	25	Output strobe for I/O expander
P10 – P17 Port 1	27-34	8-bit quasi-bidirectional port
P20 – 27 Port 2	21-24	8-bit quasi-bidirectional port
	35-38	P20-P23 contain the four high order program counter bits during an external program memory fetch, and serve as a 4-bit I/O expander bus for the 8243.

Table 5.1 (Continued). 8048/8748 Pin Definitions

DESIGNATION	PIN	DESCRIPTION
DB0 – DB7 BUS	12-19	True bidirectional port which can be written or read synchronously using the $\overline{RD}$, $\overline{WR}$ strobes. The port also can be statically latched. Contains the 8 low order program counter during an external program memory fetch, and receives the addressed instruction under the control of $\overline{PSEN}$. Also contains the address and data during an external RAM data store instruction, under control of ALE, $\overline{RD}$, and $\overline{WR}$.
T0	1	Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CLK instruction.
T1	39	Input pin testable using the JT1 and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction.
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low.)
$\overline{RD}$	8	Output strobe activated during a BUS read. Can be used to enable data onto the bus from an external device. Used as a read strobe to external data memory. (Active low.)
$\overline{RESET}$	4	Input which is used to initialize the processor. (Active low.)
$\overline{WR}$	10	Output strobe during a bus write. (Active low.) Used as a write strobe to external data memory.
ALE	11	Address latch enable. This signal occurs once during each cycle. The negative edge of ALE strobes addresses into external data and program memory.

Table 5.1 (Continued). 8048/8748 Pin Definitions

DESIGNATION	PIN	DESCRIPTION
$\overline{PSEN}$	9	Program store enable. This output occurs only during a fetch to external program memory. (Active low.)
$\overline{SS}$	5	Single step input can be used in conjunction with ALE to "single step" the processor through each instruction. (Active low.)
EA	7	External access input which forces all program memory fetches to reference external memory. Useful for emulation and debug, and essential for testing and program verification. (Active high.)
XTAL1	2	One side of crystal input for internal oscillator.
XTAL2	3	Other side of crystal input.

Chapter 6

Disassembly

Disassembly Procedure

The following is the disassembly sequence for the keyboard. Refer to Figure 6.1. The Z-160 disassembly sequence is similar; for an accurate representation refer to Figure 9.2.

- Place the keyboard face down on a soft cloth.
- Remove four 6 × 3/8″ screws and bottom panel.
- Remove six 6 × 1/4″ screws and two washers.
- Remove rubber strain relief (keyboard cable connector in the Z-160) from slot.
- Remove wired keyboard.

Disassembly

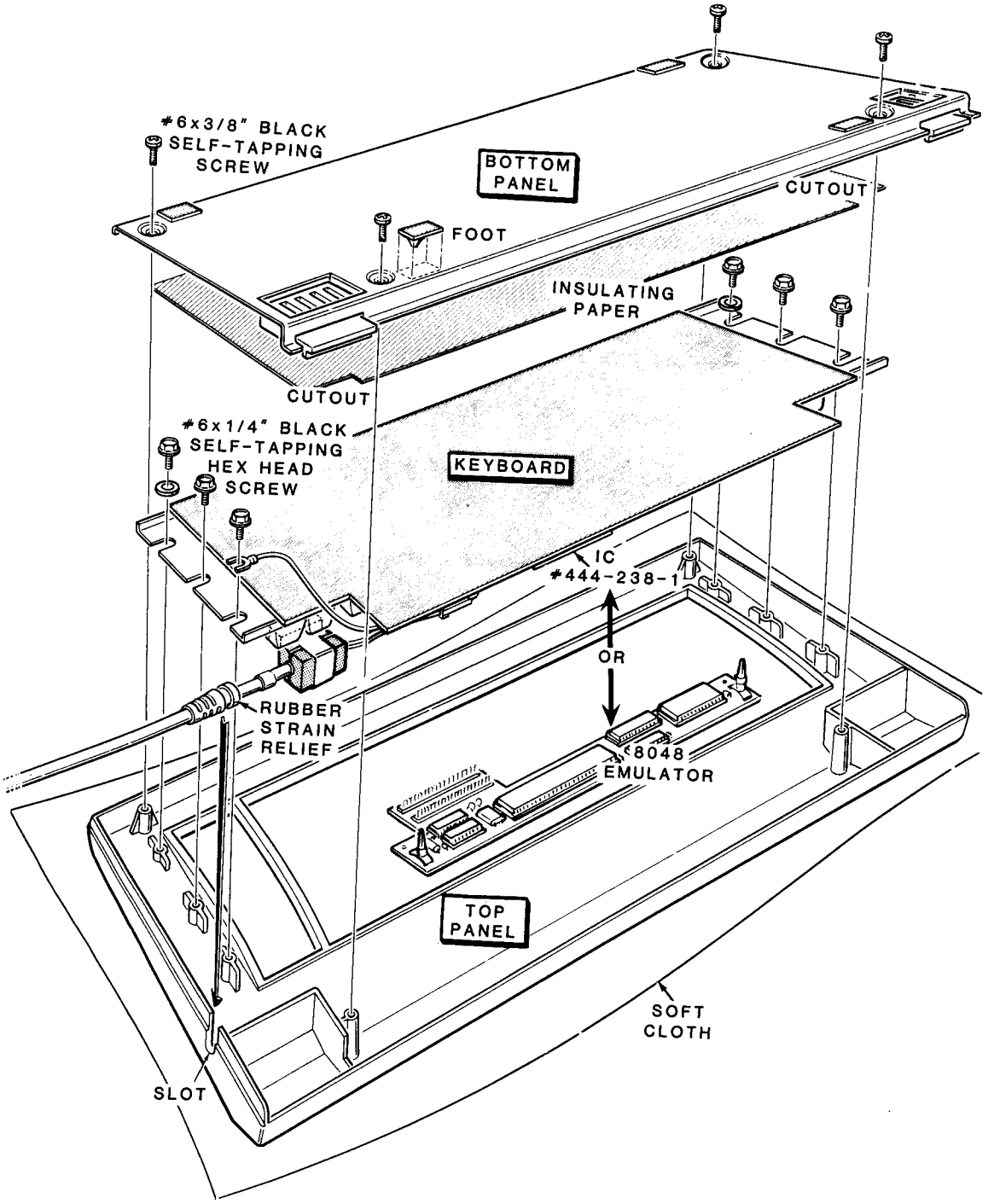


Figure 6.1. Keyboard Disassembly

Chapter 7

Troubleshooting

The microcomputer in the keyboard performs several functions when requested by the CPU, including a power-on self-test. This diagnostic CRC (Cyclic Redundancy Check) uses an algorithm to check the microcomputer ROM, tests memory, and checks for stuck keys. If a problem exists with the keyboard, an interrupt is generated to the CPU and a message is displayed on the video monitor.

Chapter 8

Reassembly

Reassembly Procedure

The following is the reassembly sequence for the keyboard. Refer to Figure 8.1. The Z-160 reassembly sequence is similar; for an accurate representation refer to Figure 9.2.

- Place the keyboard cabinet face down on a soft cloth.
- Install rubber strain relief (keyboard cable connector in the Z-160) into slot.
- Install wired keyboard into cabinet and secure with six 6 × 1/4" screws and two washers.
- Install the bottom panel and secure with four 6 × 3/8" screws.

Reassembly

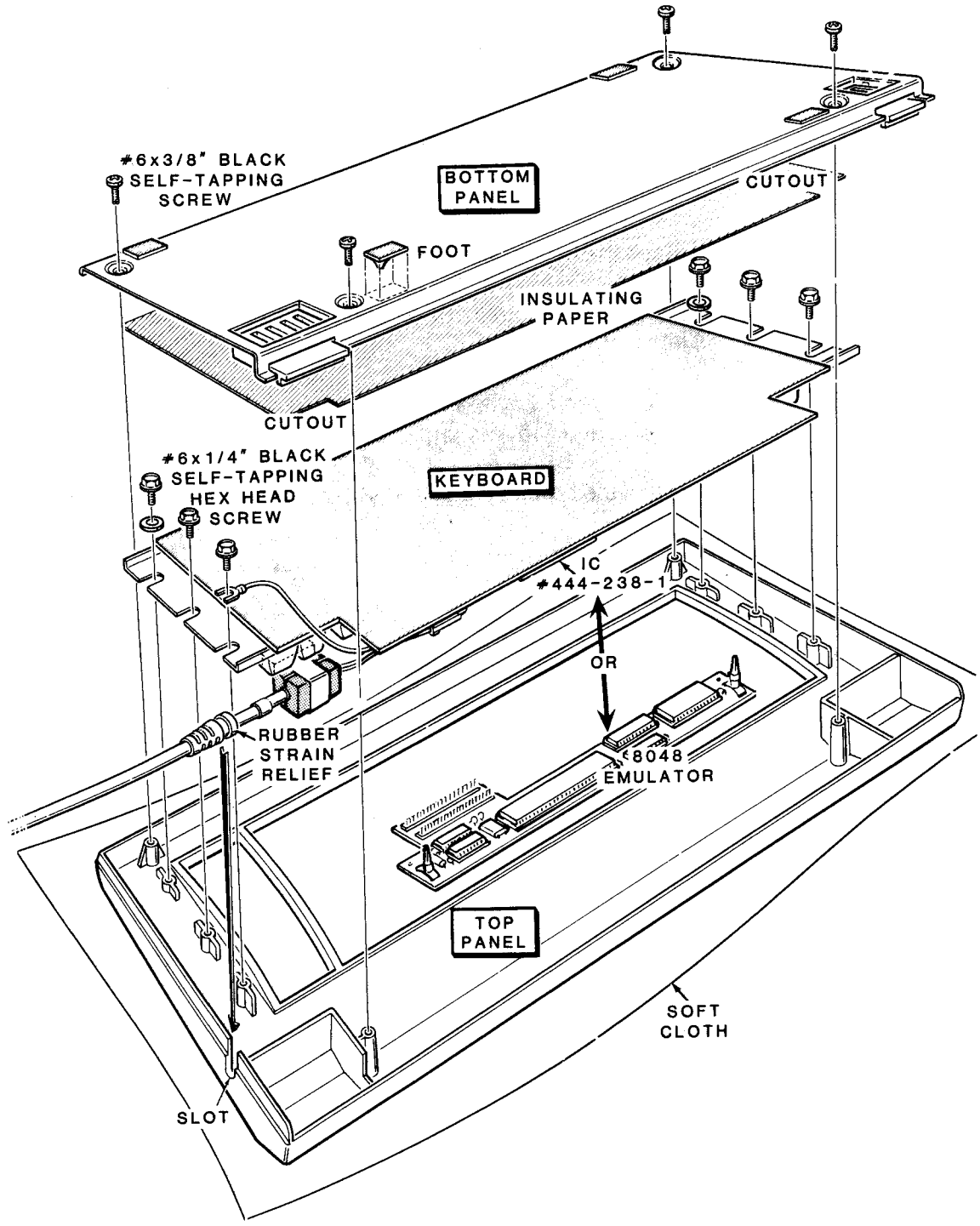


Figure 8.1. Keyboard Reassembly

Chapter 9

Parts List

Replacement Parts

This chapter includes a parts list of the keyboard components supplied by Zenith Data Systems only. Refer to Figure 9.1 for Z-150 part identification. The Z-150 Desktop Computer keyboard wired and tested part number is HE 181-5599. The Z-160 Portable Computer keyboard wired and tested part number is HE 181-4935-1. Refer to Figure 9.2.

CAUTION: This board contains electrostatic-sensitive devices (ESD). Exercise extreme care when handling these devices to prevent damage.

Keyboard Assembly Z-150

ITEM NUMBER	ZDS PART NO.	DESCRIPTION
5	HE 205-1923-1	Bottom plate
10	HE 250-1434	Screw, pan head Phillips 6-BT × .375"
15	HE 266-1220	Support leg
20	HE 258-759	Spring, leg return
25	HE 75-138	Insulator
30	HE 75-851	Insulator
35	HE 163-16	Wired keyboard
	with	
	HE 134-1473	Keyboard cable
40	HE 250-1521	Screw, slotted 6-AB × .250"
45	HE 444-238-1	Keyboard microcomputer (see Y101)
	or	
	HE 444-314	Keyboard microcomputer (see Y101)
	or	
	HE 187-5305	8048 emulator
50	HE 253-60	Washer
55	HE 260-713	Strain relief
60	HE 92-803	Molded cabinet
65	HE 485-54	Plug, button

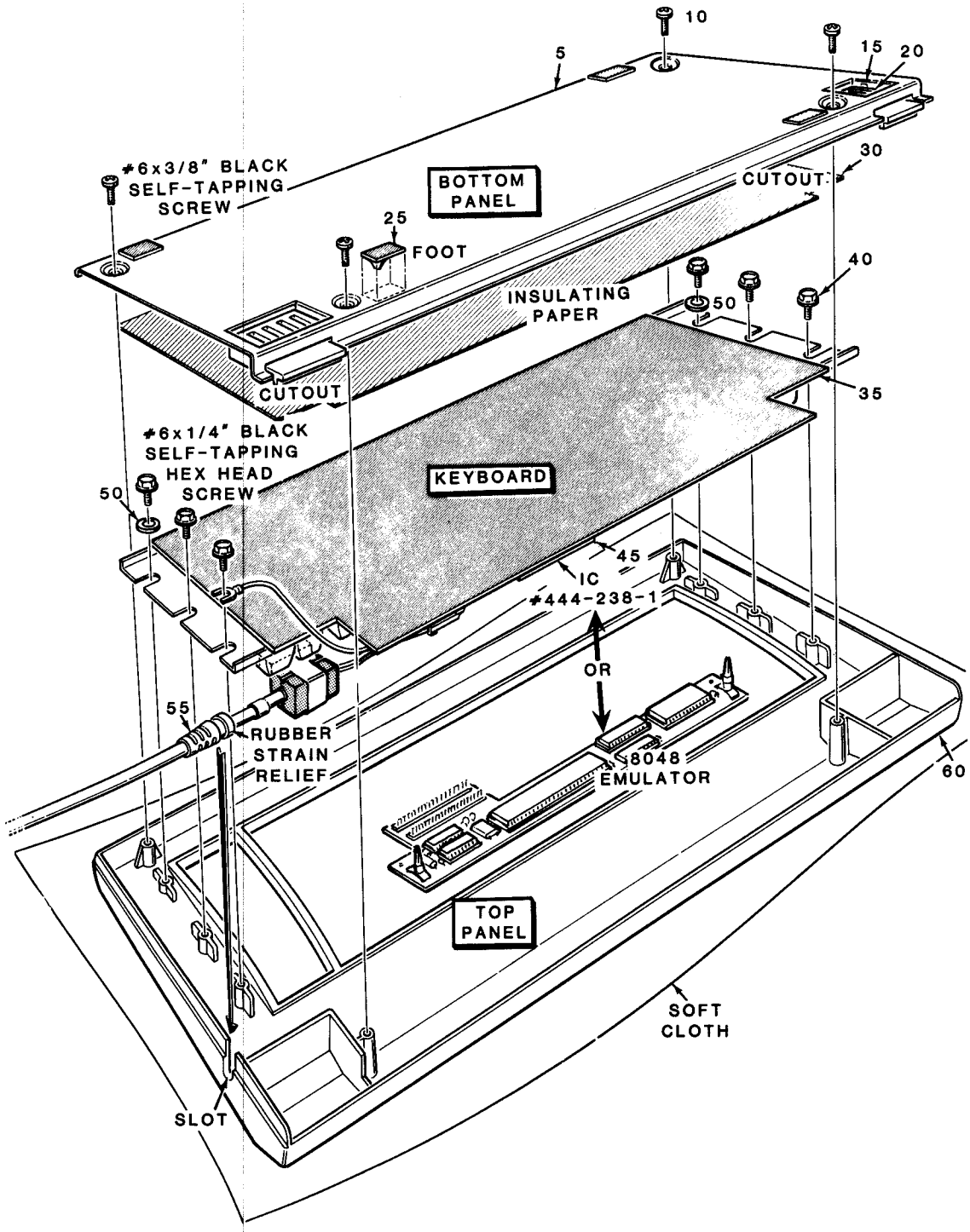


Figure 9.1. Z-150 Desktop Computer Keyboard—Exploded View

Keyboard Assembly Z-160

ITEM NUMBER	ZDS PART NO.	DESCRIPTION
5	HE 92-823	Keyboard bottom
10	HE 250-1434	Screw, pan head Phillips 6-BT × .375″
15	HE 94-643	Support leg
20	HE 453-360	Shaft
25	HE 161-16	Keyboard assembly
30	HE 250-1508	Screw, pan head slotted 6-32 × .187″
35	HE 134-1448	Cable assembly
40	HE 444-238-1	Keyboard microcomputer (see Y101)
	or	
	HE 444-314	Keyboard microcomputer (see Y101)
	or	
	HE 187-5305	8048 emulator
45	HE 92-322	Keyboard top
50	HE 94-644	Slide
55	HE 94-645	Slide latch
60	HE 252-178	Nut, push on
65	HE 134-1397	Keyboard cable assembly, coiled

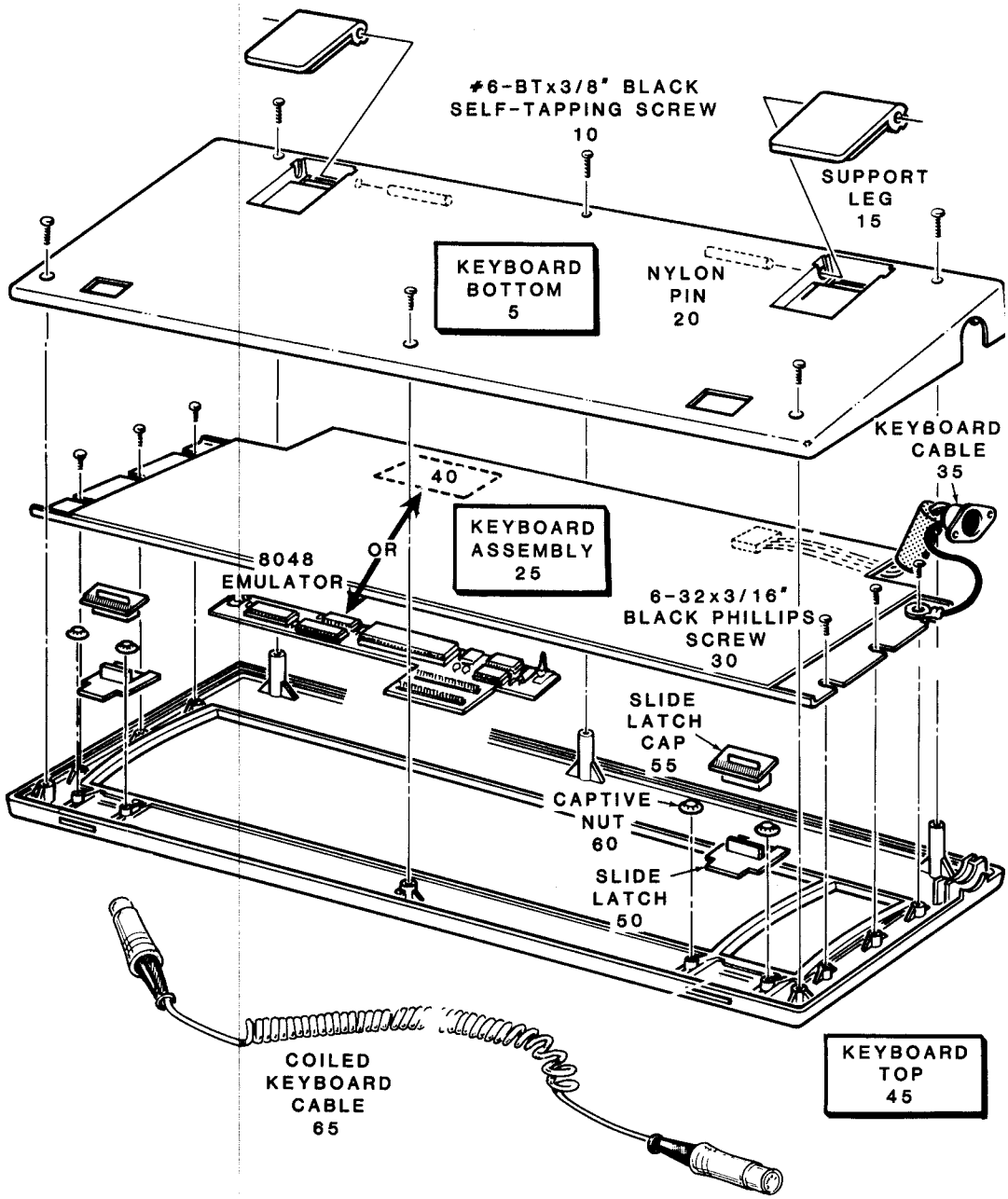


Figure 9.2. Z-160 Portable Computer Keyboard—Exploded View

Keyboard Components Z-150 and Z-160

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
Capacitors		
C1	HE 21-705	10 pF
C2	HE 21-757	22 pF
C3	HE 21-147	47 pF
C4	HE 21-147	47 pF
C5	HE 21-147	47 pF
C6	HE 25-162	33 μF
C7	HE 27-73	.047 μF
C8	HE 21-95	6 × 0.1 μF
C9	HE 21-95	6 × 0.1 μF
C10	HE 21-95	6 × 0.1 μF
C11	HE 21-95	6 × 0.1 μF
C12	HE 21-95	6 × 0.1 μF
C13	HE 21-95	6 × 0.1 μF
C14	HE 25-863	4.7 μF
Diode		
D101	HE 56-56	IN4149
Crystal		
Y101	HE 404-647 or HE 404-689	6.000 MHz (use only with keyboard microcomputer HE 444-238) 3.58 MHz (use only with keyboard microcomputer HE 444-314)
Resistors		
R1	HE 6-221-12	220 Ω
R2	HE 6-221-12	220 Ω
R3	HE 6-101-12	100 Ω
R4	HE 6-472-12	4.7 KΩ
R5	HE 6-202-12	2 KΩ
R6	HE 6-202-12	2 KΩ
R7	HE 6-202-12	2 KΩ
R8	HE 6-472-12	4.7 KΩ
R9	HE 6-472-12	4.7 KΩ
R10	HE 6-472-12	4.7 KΩ
R11	HE 6-472-12	4.7 KΩ
R12	HE 6-472-12	4.7 KΩ
R13	HE 6-472-12	4.7 KΩ
R14	HE 6-472-12	4.7 KΩ
R15	HE 6-472-12	4.7 KΩ
R16	HE 6-472-12	4.7 KΩ
R17	HE 6-472-12	4.7 KΩ

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
Integrated Circuits		
U101	HE 443-967	Hex inverter buffer/driver
U102	HE 443-811	Buffer, tri-state
U103	HE 443-991	Hex buffer/converter
U104	HE 443-991	Hex buffer/converter
U105	HE 443-1036	Dual one-of-four decoder
U106	HE 443-1036	Dual one-of-four decoder
U107	HE 444-238-1 or HE 444-314	Microcomputer
Miscellaneous		
	HE 485-54	Dummy plug for side exit
	HE 473-29	Audio transducer

8048 Emulator

Part Number HE 181-5305. Refer to Figure 9.3.

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
Capacitors		
C1	HE 21-786	.1 μF
C2	HE 21-786	.1 μF
C3	HE 21-786	.1 μF
C4	HE 21-786	.1 μF
C5	HE 21-786	.1 μF
C6	HE 21-786	.1 μF
C7	HE 21-707	36 pF
C8	HE 21-707	36 pF
C9	HE 25-866	22 pF

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
Integrated Circuits		
U1	HE 443-802	Quad, multiplexer 2-input, tri-state
	or	
	HE 443-1037	
	HE 434-299	Socket
U2	HE 443-802	Quad, multiplexer 2-input, tri-state
	or	
	HE 443-1037	
	HE 434-299	Socket
U3	HE 443-1119	Microprocessor
	HE 434-253	Socket
U4	HE 443-872	Hex inverter
	HE 434-298	Socket
U5	HE 443-837	8-bit tri-state latch
	HE 434-311	Socket
U6	HE 444-320	Emulator ROM
	HE 434-312	Socket
Crystal		
Y1	HE 404-647	

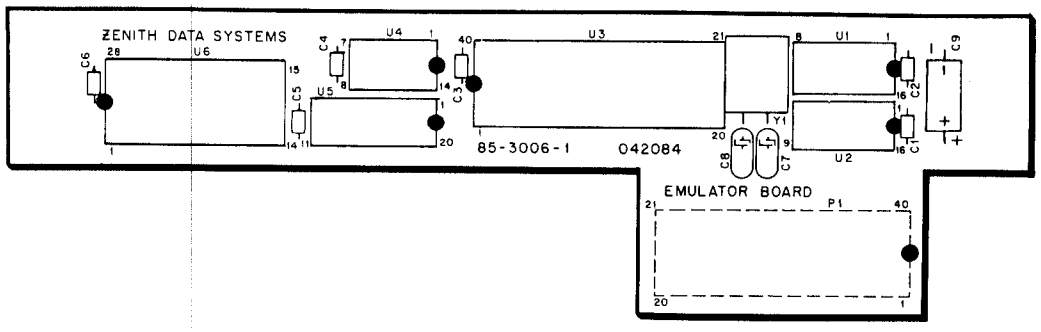
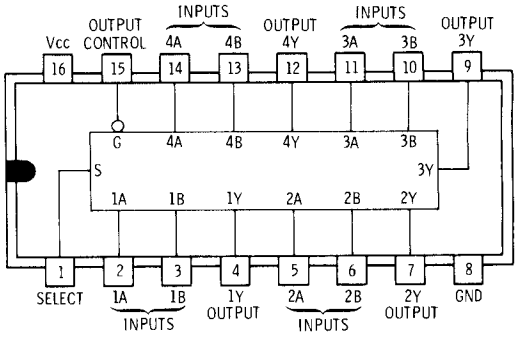
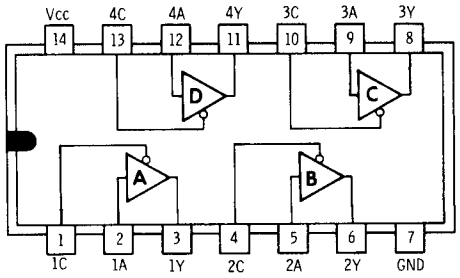


Figure 9.3. 8048 Emulator Board—Component View

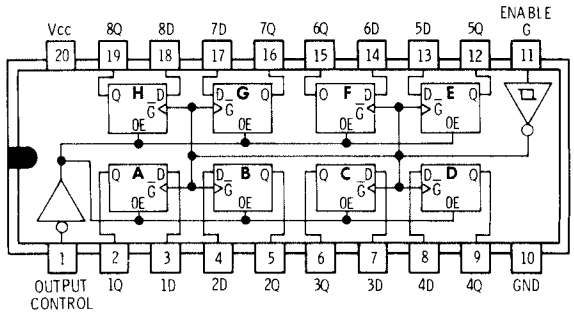
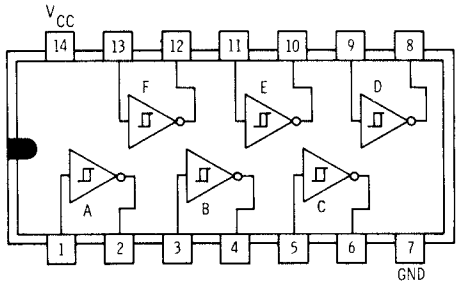
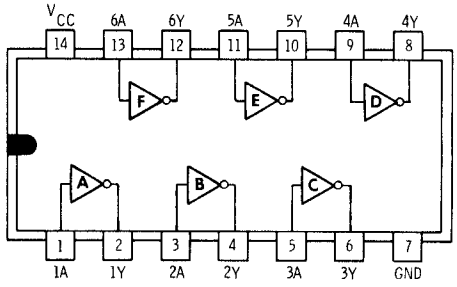
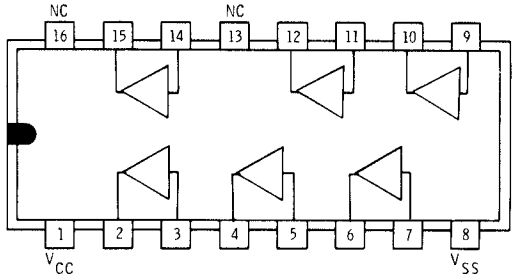
Semiconductor Identification

This section will help to identify the various semiconductor devices installed on the keyboard. The components are listed in ascending numerical order, along with the device number (where applicable), and device lead configuration. The Zenith/Heath part numbers are cross-referenced, where applicable, with generic/alternate device numbers.

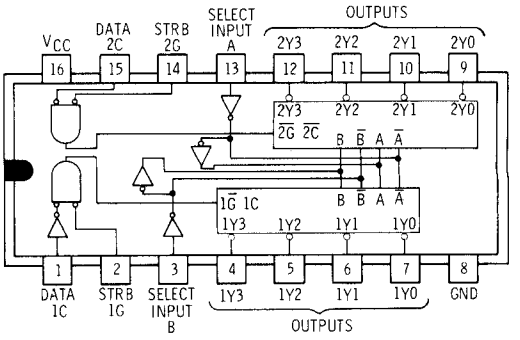
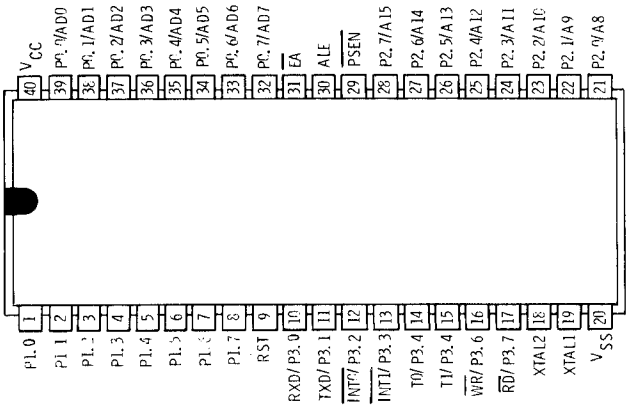
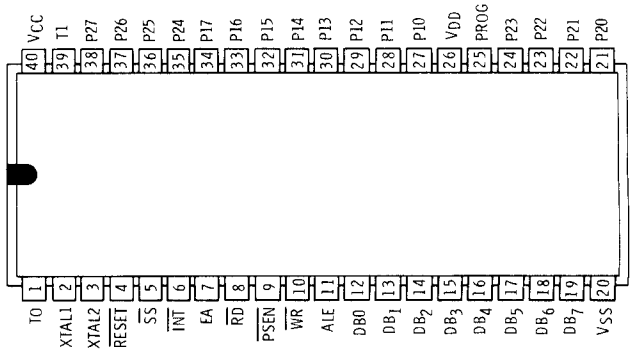
Part Number Index

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
HE 443-802 or HE 443-1037	74LS257 74ALS257	U1, U2 Quad multiplexer 2-input tri-state	
HE 443-811	74LS125	U102 Buffer tri-state	

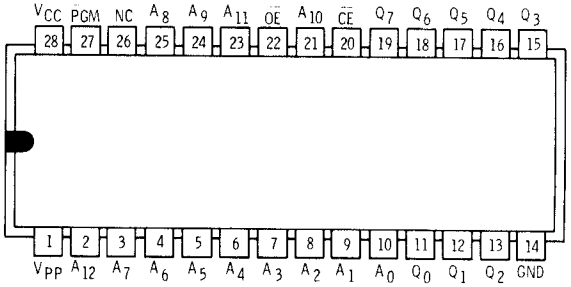
Parts List

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
HE 443-837	74LS373	U5 8-bit tri-state latch	
HE 443-872	74LS14	U4 Hex inverter	
HE 443-967	7406	U101 Hex inverter buffer/driver	
HE 443-991	MC14050B	U103, U104 Hex buffer/converter	

Parts List

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
HE 443-1036	74LS156	U105, U106 Dual one-of-four decoder	
HE 443-1119	8031	U3 Microprocessor	
HE 444-238-1 or HE 444-314	8048/8748	U107 Microcomputer	

Parts List

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
HE 444-320		U6 ROM	

SERVICE MODULE

System CPU Card

Z-100 PC Series Computers

585-62-02

860-45

ZENITH data systems

The purpose of this page is to make sure that all service bulletins are entered in this manual. When a service bulletin is received, annotate the manual and list the information in the record below.

Record of Field Service Bulletins

SERVICE BULLETIN NUMBER	DATE OF ISSUE	CHANGED PAGE(S)	PURPOSE OF SERVICE BULLETIN	INITIALS

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St. Joseph, Michigan 49085

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Chapter 1

Introduction

This service module describes the function of the Central Processing Unit (CPU) card used in the Z-100 PC Series Computers. The card described is the HE-181-5059 CPU card which contains a Harris 80C88 microprocessor. This module also can be used to service the HE-181-4646 CPU card, which is identical to the other card except that it uses an Intel 8088 microprocessor and does not contain one flip-flop required for timing with the 80C88. This flip-flop is noted on the schematic enclosed in this service module.

The CPU card is the heart of the computer system. It contains the "brains" of the system, a Harris 80C88 CMOS microprocessor. This device makes all of the decisions and controls all of the functions of the computer, based on communications to and from the keyboard and peripherals. The actions of the microprocessor are governed by machine language instructions which are contained in either the firmware stored in read-only memory (ROM), or the software transferred from disk and temporarily stored in the random access memory (RAM).

The 80C88 communicates with the rest of the system via three separate busses (groups of lines), as shown in Figure 1.1. The address bus defines which device is being talked to. The data bus carries the actual message to or from the addressed device. The control bus determines what type of operation (read, write, input/output, etc.) is to be performed and also is used to control the timing of the exchange.

The 80C88 is a 16-bit microprocessor, based on CMOS construction, which utilizes the same instruction set and operates similarly to the NMOS Intel 8088. The 80C88 has 16-bit internal architecture for all registers, internal data paths, arithmetic logic unit (ALU), and instruction codes. However, the 80C88 communicates with the rest of the system through an 8-bit data bus. The microprocessor uses a 20-bit address bus which provides over 1,000,000 separate addressing locations. Additionally, the 80C88 can address over 64,000 input/output (I/O) locations through its 16-bit I/O port addressing.

The CPU operates at a frequency of 4.77 MHz. This frequency is generated by the clock driver (8284), U211. This frequency is derived by dividing the crystal oscillator frequency (14.31818 MHz) by 3.

The CPU card was designed so that an optional coprocessor (Intel 8087) may be added to the card to speed arithmetic operations.

The 80C88 also is supported by four channels of 20-bit direct memory access (DMA). Three of the four DMA channels are available on the I/O bus to support high speed data transfer between I/O devices and memory without processor intervention. The fourth DMA channel is programmed to refresh the system dynamic RAM.

The CPU card also contains three independent 16-bit programmable interval timers. One of the timers is used to request refresh cycles from the DMA. Another timer provides updates to the time-of-day clock. The other timer is used to support the tone generation for the audio speakers. Each timer has a minimum resolution of 1.05 microseconds.

A programmable interrupt controller provides the 80C88 with eight prioritized interrupt levels.

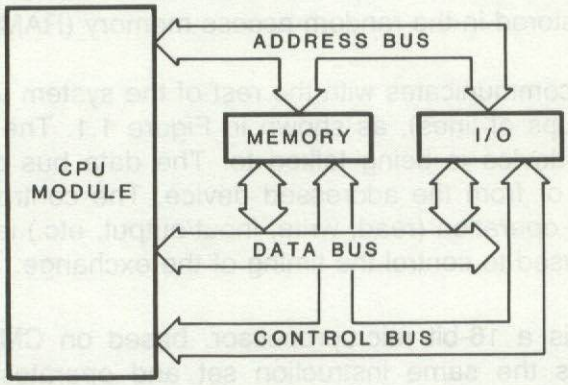

Figure 1.1. CPU Busses

Chapter 2

Configuration

For instructions on removing the card from the computer, refer to the *Base Unit Service Module.*

Dual Inline Package Switches

Two dual inline package (DIP) switches, each containing eight individual switch sections, are used to select specific operation modes. Switch SW1 selects the I/O options and can be configured to select the number of 5.25-inch drives, columns in the display, base memory size, and tells the CPU if the optional 8087 coprocessor is installed.

Switch SW2 selects the extended options and may be configured to select 50 or 60 Hz line frequency for the video display, manual or auto-boot of the disk drives, and informs the CPU of the presence of add-on memory.

The setting of these switches is read by the CPU as either a logic zero (switch section in the closed "ON" position), or a logic one (switch section in the open "OFF" position). Figure 2.1 identifies and illustrates the physical configuration of both DIP switches SW1 and SW2. The configuration of the DIP switches is described in Tables 2.1 through 2.3.

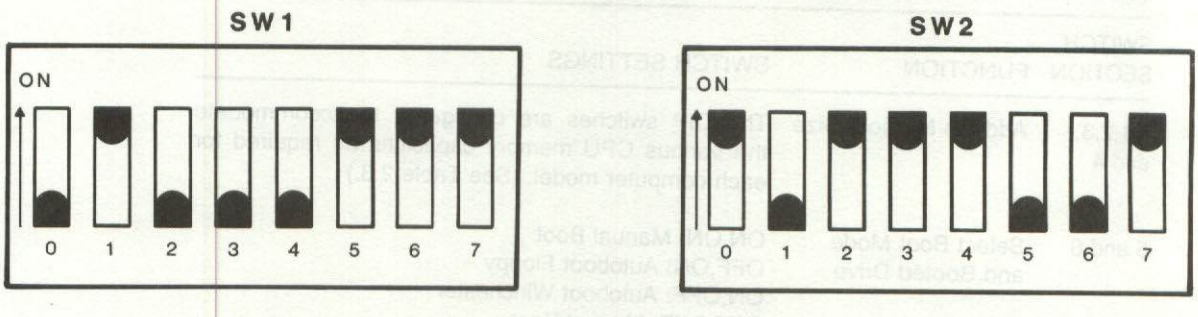

Figure 2.1. DIP Switches

Table 2.1. SW1 DIP Switch Configuration

SWITCH SECTION	FUNCTION	SWITCH SETTINGS
0	Floppy Disks Attached	ON: No Floppy Drives Attached OFF: Floppy Drives are Attached
1	8087 Installed	ON: Not Installed OFF: 8087 Present
2 and 3	Base Memory Size	OFF,OFF: 64K **NOTE:** Sections 2 and 3 are always set to this position.
4 and 5	Column Display Type	ON,ON: Reserved OFF,ON: 40 × 25 ON,OFF: 80 × 25 OFF,OFF: Monochrome Video
6 and 7	Number of 5.25-inch Drives Installed	ON,ON: 1 Drive OFF,ON: 2 Drives ON,OFF: 3 Drives OFF,OFF: 4 Drives

Table 2.2. SW2 DIP Switch Configuration

SWITCH SECTION	FUNCTION	SWITCH SETTINGS
0,1,2,3, and 4	Add-On Memory Size	The DIP switches are configured to accommodate the various CPU memory capacities as required for each computer model. (See Table 2.3.)
5 and 6	Select Boot Mode and Booted Drive	ON,ON: Manual Boot OFF,ON: Autoboot Floppy ON,OFF: Autoboot Winchester OFF,OFF: Manual Boot
7	Line Frequency Select for CRT Screen Sweep	ON: 60 Hz Display OFF: 50 Hz Display*

*Not Recommended

Chapter 3

Basic Theory of Operation

Block Diagram

A simplified block diagram of the CPU card is shown in Figure 3.1. This block diagram represents the major functions of the CPU card. Refer to this block diagram for the discussions in this chapter.

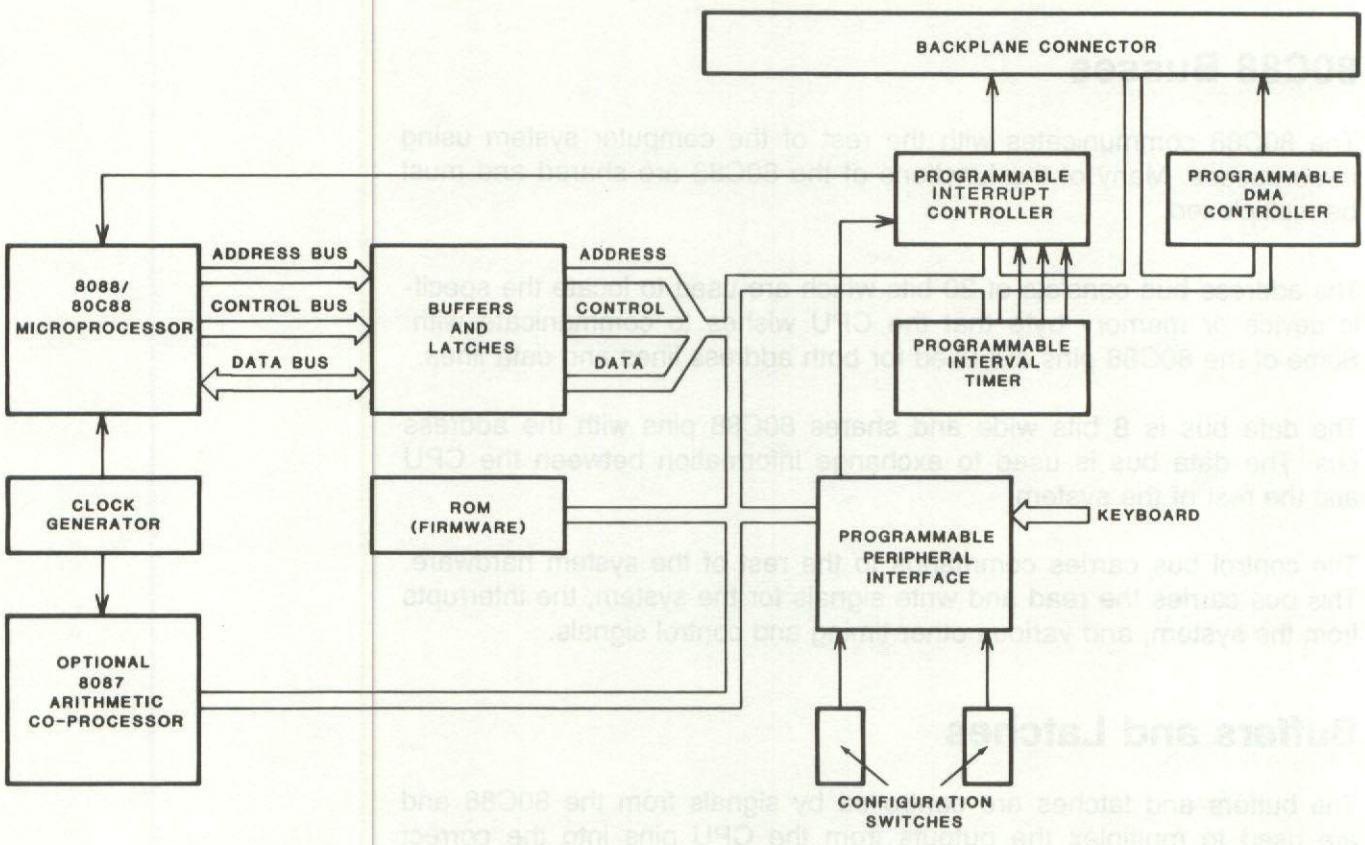

Figure 3.1. CPU Card Block Diagram

80C88 Microprocessor

The 80C88 is a microprocessor manufactured using CMOS technology. This device has 16-bit internal architecture, but uses an 8-bit data bus to communicate with other devices.

The microprocessor is the heart of the computer system. It takes inputs from the peripherals or keyboard and calculates solutions or controls the system, based on those inputs.

80C88 Busses

The 80C88 communicates with the rest of the computer system using three busses. Many of the functions of the 80C88 are shared and must be multiplexed.

The address bus consists of 20 bits which are used to locate the specific device or memory byte that the CPU wishes to communicate with. Some of the 80C88 pins are used for both address lines and data lines.

The data bus is 8 bits wide and shares 80C88 pins with the address bus. The data bus is used to exchange information between the CPU and the rest of the system.

The control bus carries commands to the rest of the system hardware. This bus carries the read and write signals for the system, the interrupts from the system, and various other timing and control signals.

Buffers and Latches

The buffers and latches are controlled by signals from the 80C88 and are used to multiplex the outputs from the CPU pins into the correct busses. These devices also control the direction of the data flow and buffer the data and address lines so that more than a few integrated circuits (ICs) can be driven by the various busses.

Table 2.3. SW2 Memory Size Switch Section Settings

0	1	2	3	4		NUMBER OF BYTES
ON	ON	ON	ON	ON	=	64K
ON	OFF	ON	ON	ON	=	128K
ON	ON	OFF	ON	ON	=	192K
ON	OFF	OFF	ON	ON	=	256K
ON	ON	ON	OFF	ON	=	320K
ON	OFF	ON	OFF	ON	=	384K
ON	ON	OFF	OFF	ON	=	448K
ON	OFF	OFF	OFF	ON	=	512K
ON	ON	ON	ON	OFF	=	576K
ON	OFF	ON	ON	OFF	=	640K

Jumper Connector Configuration

A row of jumper connectors is located in the center of the CPU card (Figure 2.2). The jumper connectors configure the monitor ROMs. The jumpers may be configured as follows:

- A jumper connected between pins 5 and 10 informs the CPU that ROM 1 is a 256K device.
- A jumper connected between pins 4 and 9 informs the CPU that ROM 1 is a 128K device.
- A jumper connected between pins 3 and 8 informs the CPU that ROM 2 is a 256K device.
- A jumper connected between pins 2 and 7 informs the CPU that ROM 2 is a 128K device.
- A jumper connected between pins 1 and 6 informs the CPU that a RAM chip is installed into the ROM 2 socket. The card normally is supplied with no RAM installed.

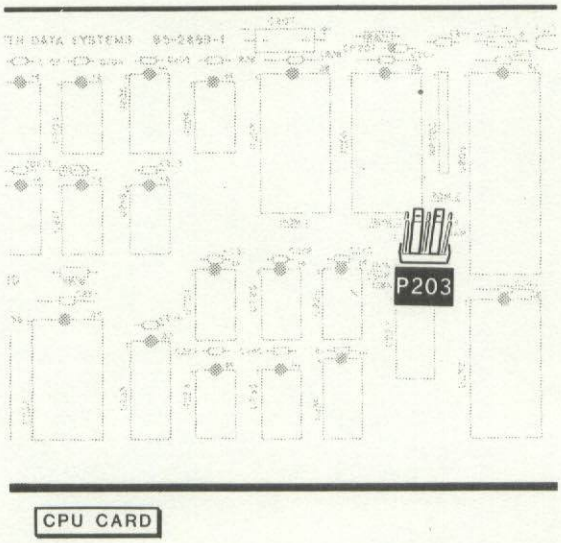

Figure 2.2. Jumper Connections

Clock Generator

The clock generator provides the clock signals to the microprocessor which are used to establish the system timing.

The first stage of the clock generator is an oscillator which operates at a frequency of 14.31818 MHz. This frequency is divided by 3 internally to provide a 4.77 MHz square wave output for the microprocessor and the coprocessor clocks.

The clock generator also provides the timing for the DMA actions by dividing each clock pulse into sections. During part of the clock period, the DMA can be active. During the remainder of the time period, the microprocessor can control the data bus.

Optional 8087 Arithmetic Coprocessor

The 8087 may be installed onto the CPU card as an option. The 8087 is an ALU processor which contains expanded 80-bit registers, an expanded instruction set, and internal logic to perform complex floating decimal point mathematical operations with fewer program instructions.

The 80C88 can perform all of the operations of the 8087 but requires many more steps and, therefore, much more time. When installed, the 8087 increases the system throughput.

ROM (Firmware)

The ROM memory located on the CPU card contains the instructions which control the fundamental operation of the microprocessor. These instructions tell the CPU how to read the keyboard, perform basic time delays, and similar functions. The instructions for power-up checks and more complete diagnostics also are contained on these ROMs.

Programmable Interval Timer

The programmable interval timer contains three independent counters which are used by the computer system to generate specific time delays. These timers are used to update the system time-of-day clock, refresh the system dynamic memory, and provide the frequency used as a tone generator for the system audio speakers.

When a counter reaches its terminal count, an interrupt signal is issued. Each counter has its own interrupt output.

Programmable Interrupt Controller

The programmable interrupt controller is used to prioritize the system interrupts. This device accepts up to eight interrupt inputs from other parts of the system, assigns each input a priority in which it will be processed, and then directs the CPU to the address of the next instruction in the interrupt routine.

Programmable DMA Controller

Because memory can be read and written to more rapidly than the CPU is capable of performing these functions, the programmable DMA controller is used to control the busses to obtain this information while the CPU is not in control of the busses. This process speeds the exchange of data.

Clock Generator

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Programmable Peripheral Interface

The programmable peripheral interface is used to communicate with the keyboard and to read the states of the configuration switches. This device relieves the CPU of the responsibility of frequently checking for keyboard entries. When a key is pressed, this device sends a system interrupt to the programmable interrupt controller, which informs the CPU that a key has been pressed. On powerup, the configuration switches are checked through this device.

Configuration Switches

The configuration switches are used to inform the CPU of the computer system configuration so that the CPU knows how to best utilize the installed hardware. For further details, refer to Chapter 2.

Backplane Connector

The backplane connector is used to connect the CPU busses to the rest of the system and to carry other timing, control, and interrupt signals.

I/O operations are identical to memory operations except for the state of the M/IO* signal. When this line is high, memory is being addressed. When it is low, I/O is being addressed. This also can be determined by the state of lines S0, S1, and S2. The function of these pins is defined in Table 4.2.

Table 4.2. Strobe S0, S1, and S2 Decoding

S0	S1	S2	FUNCTION	8288 OUTPUT
0 (LOW)	0	0	Interrupt Acknowledge	INTA*
0	0	1	Read I/O Port	IOR*
0	1	0	Write I/O Port	IOW*
0	1	1	Halt	None
1	0	0	Code Access	None
1	0	1	Read Memory	MEMR*
1	1	0	Write Memory	MEMW*
1	1	1	Idle	None

Memory Organization

The memory is processed internally by the 8088 as 16 memory segments each 64K-bytes long. This is because the CPU uses two separate registers to store the address. A 4-bit register, called the segment register, defines the most-significant 4 bits of the address. The lower 16 bits of the address are stored in a separate register.

Interrupt Operation

There are two types of interrupt used with the 8088/80C88. The non-maskable interrupt cannot be ignored by the device, while some instructions can tell the CPU to ignore maskable interrupts. In all cases, the basic operation of the interrupt is the same.

When a device generates an interrupt, a logic high is placed on the appropriate interrupt line (NMI for non-maskable or INTR for maskable interrupts). When the CPU completes its current instruction, it stores the contents of its program counter in memory.

If the interrupt is a maskable interrupt, the INTA* line is brought low and the interrupting device must respond by sending an 8-bit type number to the data bus. The CPU will then execute the first instruction found at the address corresponding to the interrupt type. The interrupt program must end with a return command (RET), which causes the CPU to return to the operation which was interrupted.

If the interrupt is a non-maskable interrupt, the CPU is driven to the address of a type two interrupt. In all cases, the non-maskable interrupt has priority over the maskable interrupt. When both types of interrupt occur at the same time, the non-maskable interrupt will be processed first. A non-maskable interrupt also must end with a return command.

Chapter 4

IC Operation Description

This chapter describes the operation of the most complex ICs on the CPU card. The chapter provides descriptions similar to those found in data sheets for the components, and provides general information on the operation of the ICs. Specific functions of the ICs used on the CPU card are described in Chapter 5. An understanding of these devices may be helpful in understanding the specific functional descriptions found in Chapter 5.

8088/80C88 Operation

General

The 8088 is a microprocessor manufactured using NMOS technology. The 80C88 is functionally identical to the 8088, but is fabricated using CMOS technology. The instruction set is identical for the two devices, as is the internal architecture. The timing of the interrupt signals is slightly different between the 8088 and the 80C88. The 80C88 requires a timing flip-flop on the interrupt line and, therefore, is not directly interchangeable with the 8088 (which does **not** require the flip-flop).

These devices have 16-bit internal architecture, but communicate through eight data lines. Twenty address lines provide over 1,000,000 memory address locations. Additionally, this microprocessor can address 64K I/O locations.

In the Z-100 PC Computer Series, a 4.77 MHz clock is used to drive the CPU. The clock pulses are used to provide timing of the signals inside the chip. Several clock pulses are required to execute an operation.

The microprocessor must be told what to do for each operation. These instructions are contained either on the ROM located on the CPU card, or are transferred from disk to the RAM located on the dynamic memory card. If no instruction is received, the microprocessor becomes lost.

Pinouts

The pinout of the 8088/80C88 is shown in Figure 4.1. The function of each pin is discussed in Table 4.1.

Table 4.1. CPU Pin Functions

PIN NO.	SIGNAL NAME	FUNCTION
1	GND	Ground
2-7	A8-A14	These are the middle address lines and are used only for addressing.
9-16	AD0-AD7	These lines are multiplexed and share the functions of low-order addresses and the data lines. At the beginning of a read or write cycle they are used for the low-order address, and later are used to transfer data into the CPU.
17	NMI	This pin is used to signal the CPU that a non-maskable interrupt has occurred. A low to high transition of this line is acknowledged by the CPU. Operation of the interrupts is discussed in the text of this chapter.
18	INTR	A high on this pin signals the CPU that a maskable interrupt has occurred. Operation of the interrupts is discussed in the text of this chapter.
19	CLK	The 4.77 MHz square wave from the clock generator is connected to the CPU here. This signal is used to control all of the timing of the CPU.
20	GND	Ground
21	RESET	This signal causes the CPU to immediately terminate its present activity. It is used to force the system to begin the power-up sequence.
22	READY	This signal is an acknowledgment from the addressed memory or I/O device that it will complete the requested data transfer. This signal normally is used with low speed devices which cannot complete a data transfer in one machine cycle.
23	TEST*	This signal is used when the 8087 is installed in the system. When control is switched to the 8087, a "wait for test" command is given. After this command, the 8087 places a high on pin 23 and the 8088 remains in an idle state until the 8087 returns pin 23 low.
24	INTA*	This pin is the interrupt acknowledge signal. The CPU brings this pin low to acknowledge a maskable interrupt and request a type number. Operation of the interrupts is discussed in the text of this chapter.
25	ALE	This signal is used to latch the address into the address latches.

Table 4.1 (continued). CPU Pin Functions

PIN NO.	SIGNAL NAME	FUNCTION
26-28	S0,S1,S2	These signals are decoded to produce the read and write pulses for the system. Table 4.2 defines the function of these signals.
29	LOCK*	This signal, when low, prevents the DMA from gaining control of the system busses.
30	RQ*/GT0	This pin is not used in the Z-100 PC, but may be used in other systems by another bus master to force the 8088 to release control of the bus.
31	RQ*/GT1	This line is used by the 8087 to force the 8088 to relinquish control of the busses. A three-pulse exchange must occur. The 8087 sends a one clock pulse-wide request to the 8088. At the end of the instruction, the 8088 sends a pulse to the 8087 indicating that it has relinquished control of the bus. One clock pulse before the end of the 8087 instruction cycle, it sends a pulse to the 8088 informing it that it will regain control of the busses on the next clock pulse. These pulses synchronize the exchange of control of the busses.
32	RD	This pin is not used in the Z-100 PC, but provides a read pulse for minimum systems. The Z-100 PC uses the S0, S1, and S2 pulses to generate this function.
33	MN/MX*	This pin, when grounded, informs the CPU that it is operating in a maximum system mode.
34	HIGH	This pin goes to a high impedance state when a request (GT1*) is granted. At all other times it is a logic high.
35-39	A15-A19	These pins form the high-order address or segment addresses.
40	VCC	This pin connects the CPU to the +5 VDC power supply.

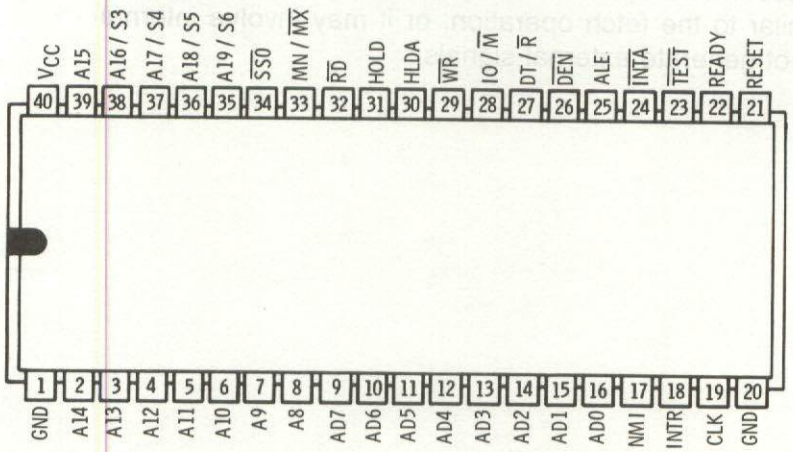


Figure 4.1. 8088/80C88 Pinout

The Instruction Cycle

The instruction cycle consists of two parts, the instruction fetch and the operation. All instruction fetches are identical regardless of the instruction, but the operation may be of variable length depending on the instruction.

The first operation in the fetch is to load the contents of the program counter (PC) internal register into the address output lines. The PC keeps track of the location of the next instruction stored in memory.

When the address is stable on the output pins, the ALE signal is brought high to latch the address into external latches. The PC then is disconnected from the outputs and incremented so that it points to the location of the next instruction.

After the address is latched, the read (RD*) signal is brought low. In maximum systems like the Z-100 PC, a combination of the S0, S1, and S2 lines also can be used to generate this function. When this signal occurs, the data from the addressed memory location is sent to the data lines and decoded by the CPU.

Some instructions are 2 bytes long. When the CPU detects that this is the case, it repeats the cycle to load the second half of the instruction.

The second half of the instruction cycle is an operation determined by decoding the instruction. The operation may involve memory reads or writes which are similar to the fetch operation, or it may involve internal functions which do not generate external signals.

System Timing

Figure 4.2 illustrates the system timing.

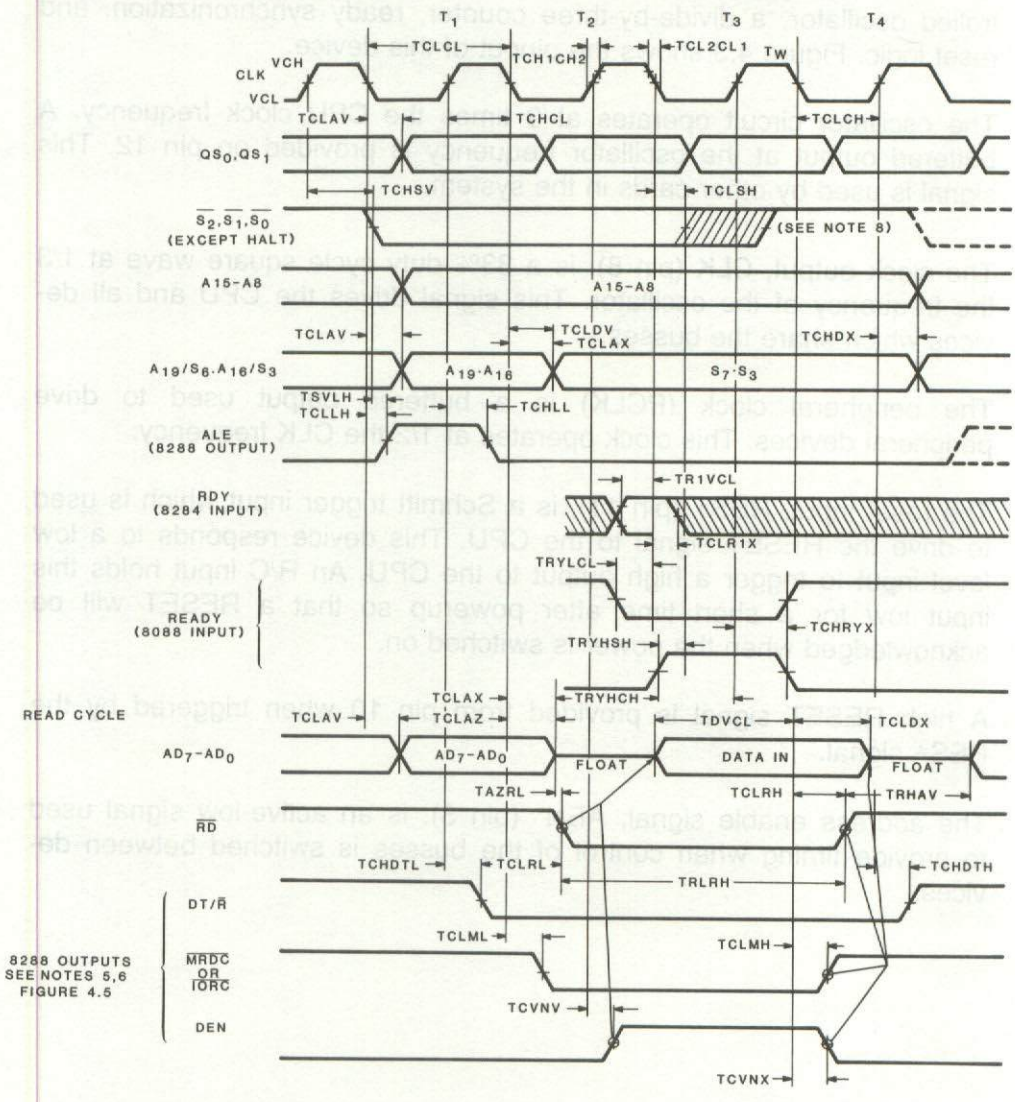


Figure 4.2. 8088/80C88 Maximum Mode Timing

Clock Generator 8284

The 8284 clock generator provides the system clock, in addition to a number of timing functions for the CPU. The chip contains a crystal controlled oscillator, a divide-by-three counter, ready synchronization, and reset logic. Figure 4.3 shows the pinout of this device.

The oscillator circuit operates at 3 times the CPU clock frequency. A buffered output at the oscillator frequency is provided on pin 12. This signal is used by other cards in the system.

The clock output, CLK (pin 8), is a 33% duty cycle square wave at 1/3 the frequency of the oscillator. This signal drives the CPU and all devices which share the busses.

The peripheral clock (PCLK) is a buffered output used to drive peripheral devices. This clock operates at 1/2 the CLK frequency.

The reset input, RES* (pin 11), is a Schmitt trigger input which is used to drive the RESET signal to the CPU. This device responds to a low level input to trigger a high output to the CPU. An R/C input holds this input low for a short time after powerup so that a RESET will be acknowledged when the power is switched on.

A high RESET signal is provided from pin 10 when triggered by the RES* signal.

The address enable signal, AEN* (pin 3), is an active-low signal used to provide timing when control of the busses is switched between devices.

The bus ready signal, RDY1 (pin 4), is used to inform the clock generator that bus control is being shifted from another bus master back to the CPU. This signal is synchronized to the clock and sent to the CPU as a high on the READY line (pin 5).

+5 VDC is supplied to the clock generator on pin 8 and ground must be supplied on pin 9.

The other pins of the clock generator are not used in the Z-100 PC.

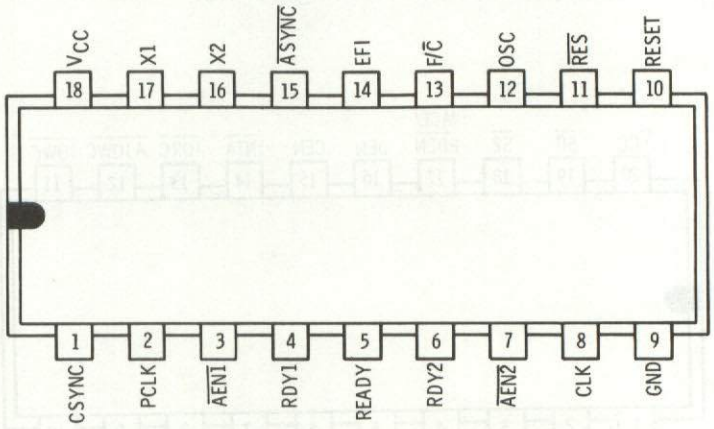


Figure 4.3. 8284 Clock Generator Pinout

8288 Bus Controller

The bus controller decodes the CPU status lines (S0, S1, and S2) to provide the address latch signals and the read and write pulses for the busses. The bus controller also disables the bus buffer/driver/latches when other devices have control of the busses.

The 8288 pinout is shown in Figure 4.4. The output functions are defined in Table 4.2. The function of each pin is described in Table 4.3. The timing of the outputs is shown in Figure 4.5.

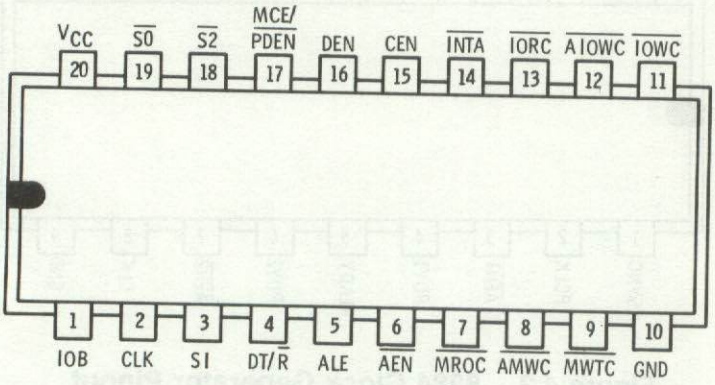
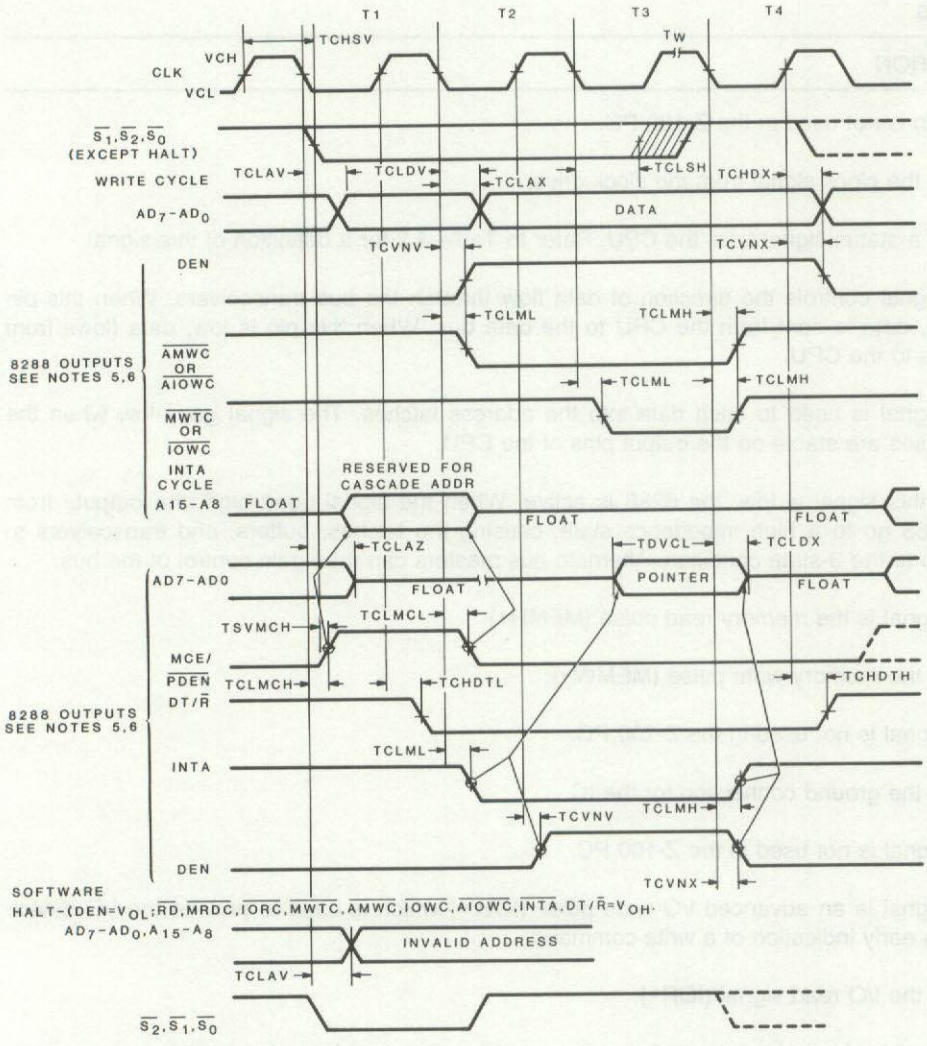


Figure 4.4. 8288 Pinout

Table 4.3. 8288 Pin Functions

PIN NO.	SIGNAL NAME	FUNCTION
1	IOB	This pin is not used in the Z-100 PC.
2	CLK	This is the clock signal from the clock driver.
3	S1*	This is a status signal from the CPU. Refer to Table 4.2 for a definition of this signal.
4	DT/R*	This signal controls the direction of data flow through the bus transceivers. When this pin is high, data is sent from the CPU to the data bus. When this pin is low, data flows from the bus to the CPU.
5	ALE	This signal is used to latch data into the address latches. The signal goes low when the addresses are stable on the output pins of the CPU.
6	AEN*	When this signal is low, the 8288 is active. When the signal goes high, the outputs from the 8288 go to a high impedance state, causing the latches, buffers, and transceivers to also go to the 3-state condition. Alternate bus masters can then gain control of the bus.
7	MRDC*	This signal is the memory read pulse (MEMR*).
8	AMWC*	This is the memory write pulse (MEMW*).
9	MWTC*	This signal is not used in the Z-100 PC.
10	GND	This is the ground connection for the IC.
11	IOWC*	This signal is not used in the Z-100 PC.
12	AIOWC*	This signal is an advanced I/O write pulse (IOW*) which is used to provide the I/O device with an early indication of a write command.
13	IORC*	This is the I/O read signal (IOR*).
14	INTA*	This signal informs an interrupting device that it must provide an interrupt type number to the CPU.
15	CEN	When this signal is low, all command outputs from this device are forced to their high impedance state. All outputs are enabled when this signal is high.
16	DEN	This signal enables the data transceivers when it is high. The data transceivers are disabled when this signal is low.
17	MCE/PDEN*	This signal is not used in the Z-100 PC.
18,19	S1,S2	These are the status inputs from the CPU. Refer to Table 4.2.
20	VCC	This is the +5 VDC power supply input.



NOTES:
1. ALL SIGNALS SWITCH BETWEEN V_{OH} AND V_{OL} UNLESS OTHERWISE SPECIFIED.
2. RDY IS SAMPLED NEAR THE END OF T_2,T_3,T_W TO DETERMINE IF T_W MACHINES STATES ARE TO BE INSERTED.
3. CASCADE ADDRESS IS VALID BETWEEN FIRST AND SECOND INTA CYCLES.
4. TWO INTA CYCLES RUN BACK-TO-BACK. THE 8088 LOCAL ADDR/DATA BUS IS FLOATING DURING BOTH INTA CYCLES. CONTROL FOR POINTER ADDRESS IS SHOWN FOR SECOND INTA CYCLE.
5. SIGNALS AT 8284 OR 8288 ARE SHOWN FOR REFERENCE ONLY.
6. THE ISSUANCE OF THE 8288 COMMAND AND CONTROL SIGNALS ($\overline{MRDC}$,$\overline{MWTC}$, $\overline{AMWC}$,$\overline{IORC}$,$\overline{IOWC}$,$\overline{AIOWC}$,$\overline{INTA}$ AND DEN) LAGS THE ACTIVE HIGH 8288 CEN.
7. ALL TIMING MEASUREMENTS ARE MADE AT 1.5V UNLESS OTHERWISE NOTED.
8. STATUS INACTIVE IN STATE JUST PRIOR TO T4.

Figure 4.5. 8288 Timing

8259 Programmable Interrupt Controller

The programmable interrupt controller is used to prioritize up to eight incoming interrupts and interface those interrupts with the CPU maskable interrupt input. The CPU can tell the 8259 to ignore (mask) all interrupts or change the priority of the interrupts.

When the system is powered up, the CPU must initialize the 8259. The CPU initializes the 8259 by writing a control word into the device. The initialization process is as follows: the IC is enabled (low on pin 1), the control word is placed on the data bus, and then the WR* pulse low is brought low (pin 2). The control word clears the internal registers and sets the priority of the interrupts. A control word can be written at any time to clear the registers or to change the priorities.

When one of the interrupt inputs goes high, the device checks and sets its interrupt request register. If no interrupt is in progress, a high pulse is sent out on the INT line. If an interrupt is in progress, the 8259 will wait until the current interrupt is completed and then begin the process. The microprocessor responds with a low on the INTA* line when it completes its current instruction. The 8259 checks all of its three cascading inputs. When the second INTA* comes from the CPU, the type number (interrupt instruction vector) of the interrupt is sent to the CPU on the data lines. When the last instruction in the interrupting routine is completed, an end of interrupt signal is sent to the 8259. The interrupt request register then is cleared.

The pinout of the 8259 is shown in Figure 4.6.

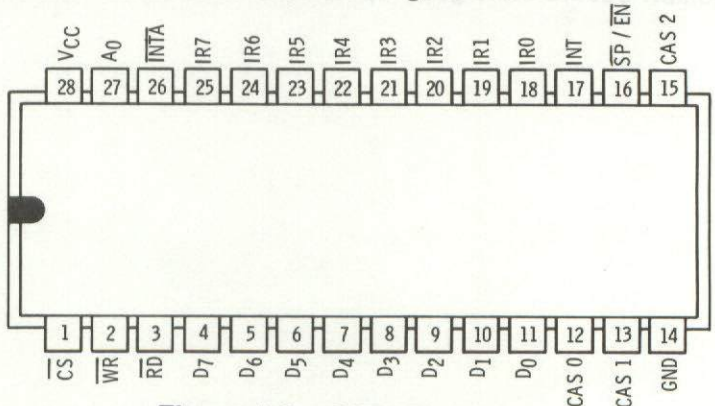


Figure 4.6. 8259 Pinout

8253 Programmable Interval Timer

The programmable interval timer contains three independent programmable clocks. The clocking signals all are connected to the PCLK signal from the clock generator (1/2 the CLK frequency). The 8253 can operate in a number of modes which are set by the control word sent from the CPU.

For mode 0, a terminal count is loaded into the selected clock and it then begins to count from 0 until the terminal count value is reached. When the clock reaches the terminal count, a high is sent out on the appropriate output and will remain there until the terminal count is loaded again. This high may be used to trigger an interrupt or drive an external device.

Mode 1 is identical to mode 0 except that the output high is sent for a fixed time and then returns low.

Mode 2 is a divide-by-N rate generator. The incoming clock will be divided by the value loaded into the start register, and an output pulse equal to the length of one incoming clock pulse will be output.

Mode 3 is the same as mode 2 except that the output pulse will remain high until the next count reaches 1/2 the starting count.

Mode 4 is similar to mode 2 except that the output starts high and goes low when the terminal count is reached.

Mode 5 is a hardware-triggered strobe. The count begins when a low to high transition occurs on a gate input.

The pinout of the 8253 is shown in Figure 4.7. The programming instructions from the CPU are shown in Table 4.4.

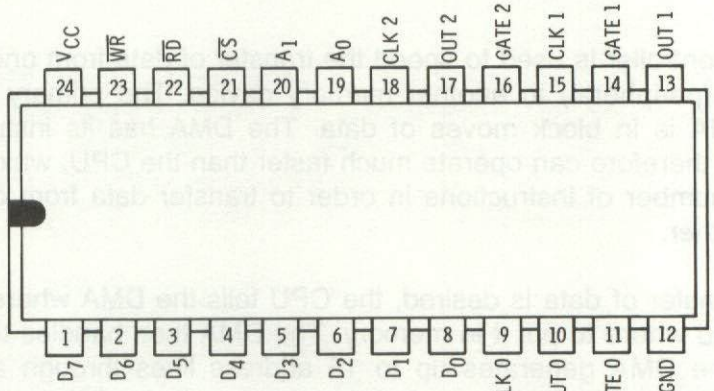


Figure 4.7. 8253 Pinout

Table 4.4. 8253 Programming Codes

CS*	RD*	WR*	A1	A2	FUNCTION
0	1	0	0	0	Load Counter 0
0	1	0	0	1	Load Counter 1
0	1	0	1	0	Load Counter 2
0	1	0	1	1	Write Mode Word
0	0	1	0	0	Read Counter 0
0	0	1	0	1	Read Counter 1
0	0	1	1	0	Read Counter 2
0	0	1	1	1	No Operation 3-State
1	X	X	X	X	Disabled 3-State
0	1	1	X	X	No Operation 3-State

8237 DMA Controller

The DMA controller is used to speed the transfer of data from one memory device (peripheral) to another memory device. The primary advantage to DMA is in block moves of data. The DMA has its instructions built in and therefore can operate much faster than the CPU, which must decode a number of instructions in order to transfer data from one device to another.

When a transfer of data is desired, the CPU tells the DMA where to get the data and where to put it in memory. The DMA then handles the data transfer. The DMA generates up to 16 address lines through address outputs A0 through A7. The high-order address is first placed on the address bus and latched by a high on the ADSTB line. The 8237 only latches the high-order address when it changes, speeding the process. The address latches and buffers are enabled by a high on the AEN line. The DMA generates all of the memory read and write signals (MEMR*, MEMW*, IOR*, and IOW*).

The DMA can operate in one of three modes. A single byte of data can be transferred, a block of data can be transferred with both the start and end of the block defined by the CPU, or, a block of data can be transferred with the end of the block defined by an external signal on the EOP line.

When the DMA is to control the bus, a hold request (HRQ) is issued to the CPU. The CPU responds with a hold acknowledge signal (HLDA) and goes into a hold state until the transfer is completed.

A peripheral can request DMA service from the 8237 on one of the DREQ lines. The 8237 responds to the input by requesting a CPU hold, and then sending a DMA acknowledge output to the peripheral when the CPU enters a hold state.

The pinout of the 8237 is shown in Figure 4.8.

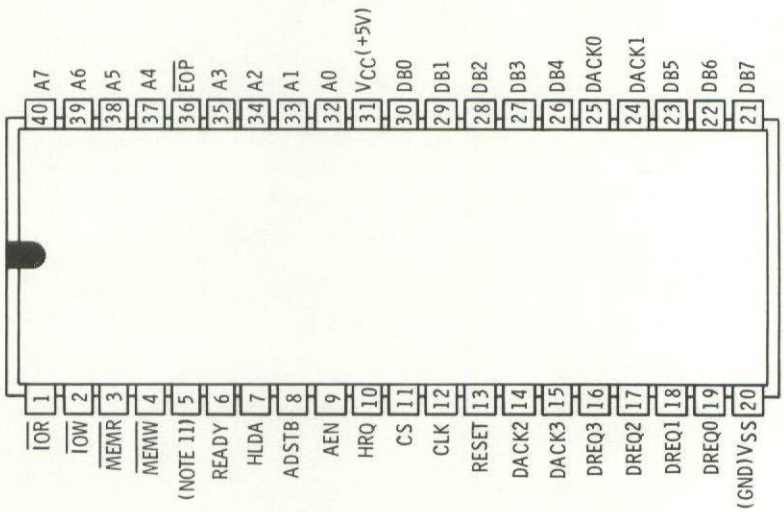


Figure 4.8. 8237 Pinout

Chapter 5

Detailed Circuit Description

Circuit Description

This chapter describes the function of each component on the CPU card. Refer to the schematic when reading the following sections.

CPU

U212 is the microprocessor, an 8088, or a Harris 80C88. This device is, internally, a 16-bit microprocessor which communicates with the rest of the system through an 8-bit data bus.

AD0 through AD7 form the data bus and the first 8 bits of the address bus. These signals come from pins 9 through 16. When a fetch cycle begins, the address is present on these lines. The ALE signal on pin 25 then goes high, causing the address to be latched into 8-bit latches U222, U241, and U242. When the address is latched, the AD pins then are free to transfer data. The DEN* signal from pin 26 then goes low. This signal is inverted by bus controller U243 and used to enable the data transceiver, U223. The direction of data flow (to or from the CPU) then is controlled by the state of pin 27 (DT/R*). If this signal is low, data is to be received and U223 allows data to flow from the bus to the CPU. If pin 27 is high, data flows through U223 from the CPU to the bus.

Address lines A8 through A19 are processed through the latches the same way as AD0 through AD7. Address lines A8 through A15 can be used only for addresses. Address lines A16 through A19 have multiplexed functions, but only the addresses are used in this system.

Pin 40 is the V_{CC} (+5 VDC power supply) input. Pin 20 is the ground connection for the power supply.

Pin 18 is the software interrupt request input (INTR) to the CPU. This is a flexible type of interrupt because the interrupting device tells the CPU how to process it. When the CPU acknowledges that this type of interrupt has occured, the interrupting device must supply the CPU with the address of the instruction which begins the programming routine for that interrupt. As many as 256 different interrupting devices can use this input so long as each device provides a different address to the CPU. Interrupt controller U237 prioritizes up to eight interrupt inputs. When a device requests an interrupt, U237 supplies the INTR signal and then the address of the routine corresponding to the interrupt input. When more than one interrupt request occurs at the same time, the highest priority interrupt will be processed first.

The programmable interrupt controller sends a high to CPU pin 18 whenever any interrupt input is received. A high on this line informs the CPU that some device has requested an interrupt. This signal is acknowledged by a low on pin 24 (INTA*) when the CPU finishes processing the current instruction. When this signal occurs, the programmable interrupt controller sends the address of the instruction to the CPU on the data lines (AD0 through AD7). Note that when the 80C88 microprocessor is used, an additional timing flip-flop is inserted in the INTR line as shown in the schematic diagram.

Pin 22 is the RDY signal used by slower memory devices to tell the CPU that they will require more than the standard amount of time to complete a data transfer. The memory device places a low on this line when it will take longer than one cycle to respond. This signal is timed through the clock generator, U211. When the device is ready to transfer data, the RDY signal is returned high.

Pin 19 is the clock input. The 4.77 MHz square wave input to this pin comes from U211, the clock generator.

Pin 21 is the RESET signal. This signal goes high when the system is powered up, and forces the CPU to begin its power-up sequence. This signal comes from clock generator U211.

Pin 17 is the non-maskable interrupt. It operates like the RESET line in that a high on this line will force the CPU to a specific location in program instructions.

Pins 23 and 34 are signals used only when the optional 8087 coprocessor is installed. Refer to Chapter 4 for a full description.

Pin 29 is the LOCK* signal. When this pin goes low (caused by specific instructions), no other device can gain control of the bus. This signal prevents the DMA from using the bus during idle times in the CPU cycle.

Pin 28 supplies the IO/M* signal. When this signal is high, I/O devices are being addressed. When this signal is low, memory is being addressed.

Clock Generator

The clock generator has a number of functions. Its primary job is to act as a crystal controlled, square wave oscillator and to provide the CPU clock. Secondarily, it provides timing synchronization for the RDY signal and provides the RESET signal at system powerup.

The oscillator in U211 is controlled by a 14.31818 MHz crystal. A buffered output at this frequency is provided and sent out on the backplane connector for use in other parts of the system. The clock generator also divides this frequency by 3 to provide a 4.77 MHz, 33.33% duty cycle square wave signal which is used to generate the CPU clock.

When the system is powered up, the input to pin 11 remains low until capacitor C7 is charged. This low is inverted and sent to the CPU as a RESET signal, causing initiation of the power-up sequence.

The 14.31818 MHz signal is used internally to provide correct timing of the RDY signal to the CPU. A DMAACTIVE* signal into the clock generator will be sent to the CPU as a high at the correct time. This may delay the RDY signal slightly.

Interrupt Controller U237

The interrupt controller generates a maskable interrupt to the CPU when any of eight input signals requests an interrupt. This device prioritizes the inputs and stores an interrupt vector (instruction address) for each input. If more than one interrupt occurs at the same time, the one with the highest priority will be processed first.

When any interrupt input goes low, a high is sent out of pin 17, INT. When the CPU finishes its current instruction, it sends back a low to pin 26 of U237. The interrupt controller then responds by sending the address of the instruction (interrupt vector) which the CPU should process in response to the interrupt.

Bus Controller U243

The bus controller is used to generate the latching and enabling signals for the buffers and address latches, as well as the read and write pulse for the system memory and I/O. These signals are generated by the S0*, S1*, and S2* signals from the CPU.

Programmable DMA Controller

Programmable DMA controller U209 can perform many memory operations involving blocks of data more rapidly or more easily than the CPU. The DMA, when permitted by the CPU, uses the address and data busses to transfer a block of data from a peripheral (such as a disk drive) directly into memory.

When a peripheral requests a DMA transfer by sending a high on one of the four DREQ lines, the DMA controller will send a hold (HLDA) signal to the CPU. The DMA then assumes control of all system busses. Data is transferred from the peripheral to a sequential block of memory locations, or from a block of memory to the peripheral.

When the DMA controller has possession of the busses, it generates its own addresses and control signals. These signals are identical to those sent from the CPU. Buffers U239 and U233, and transceivers U220, U239, and U224 allow the DMA to place its commands on the busses only when the DMA controls the busses.

ROMs U208 and U217

ROMs U208 and U217 store the basic procedures the CPU must use to begin processing software and the system diagnostics. These devices tell the CPU such things as how to initialize the system on powerup, and how to read the keyboard.

Chip Select Logic and Timing

The devices shown on sheet 3 of the schematic provide the address decoding to enable the various devices on the CPU card, and to control the timing of the DMA signals.

U201 drives the diagnostic LEDs. This hex "D" flip-flop is set or reset, depending on the results of diagnostic tests.

Programmable Peripheral Interface

The programmable peripheral interface (PPI), U230, functions as a general purpose I/O component to interface between the CPU and the keyboard, the programmable interval timer (PIT), and the configuration switches.

U230 contains three 8-bit, bidirectional, 3-state ports. The CPU communicates with the peripherals through these ports.

Port A is used for most of the data gathering. Configuration switch SW1 and the keyboard are connected to multiplexers U215 and U214, which select which device will be written into port A.

Port B is used for timing signals to the PIT.

Port C is used to read the state of configuration switch SW2.

Keyboard Communication

The keyboard sends data in a serial format. When data is received, an interrupt request (IRQ1) is sent to the programmable interrupt controller. Data is shifted into serial-in, parallel-out shift register U202. When 8 bits of data have been collected, the data is transferred to the PPI and then read by the CPU.

Programmable Interval Timer

The PIT, U232, operates as three independent 16-bit counters. All modes of operation are software programmable by the control signals and data received from the CPU. An internal 3-state buffer is used to connect the PIT to the system data bus. The counter outputs are OUT0, OUT1, and OUT2.

These clocks are loaded with a starting count and then count down until 0 is reached. When they reach 0, they send a signal to the output. This signal then is processed as a system interrupt and causes a specific function to occur.

Clock 0 causes the CPU to issue a memory refresh signal. Clock 1 causes a DMA request and is used to update the system time-of-day clock. Clock 2 is used to provide the beeper frequency to the keyboard.

Chapter 6

Troubleshooting

Introduction

Three software-based diagnostic aids are available to service personnel. These are the status LEDs, the ROM-based diagnostics, and the disk-based diagnostics (CB-5063-13). The status LEDs are located on the backplane board and on the CPU card; they are used to indicate the failure of major portions of the system. The ROM-based diagnostics include the power-up test (done automatically when the system is switched on) and several other complete tests which are selected from the menu. The operation of these tests is discussed in the *Base Unit Service Module.* The disk-based diagnostics are available as an option and are much more complete than the ROM-based diagnostics.

Servicing the CPU card with an oscilloscope is difficult because of the variable nature of the microprocessor. With experience, a technician can gather much information about the status of the card using an oscilloscope.

In order to obtain completely reliable information with the oscilloscope, it is necessary to write machine language programs to exercise the hardware so that predictable results are obtained in the desired location. No such programs are provided in this manual.

System Troubleshooting

System troubleshooting, using the ROM-based diagnostics, is covered in the appropriate *Base Unit Service Module* of the Z-100 PC Series of service modules. Refer to the applicable service module, or to the disk-based diagnostics documentation (CB-5063-13).

The LEDs on the CPU card have a diagnostic function, and are shown in Figure 6.1. All of these LEDs should light when the system is first switched on, and go out one at a time until only the RDY LED is on. (The RDY LED goes out when the operating system is loaded into RAM.) If the CPU, ROM, or INT LED is on, the CPU has failed.

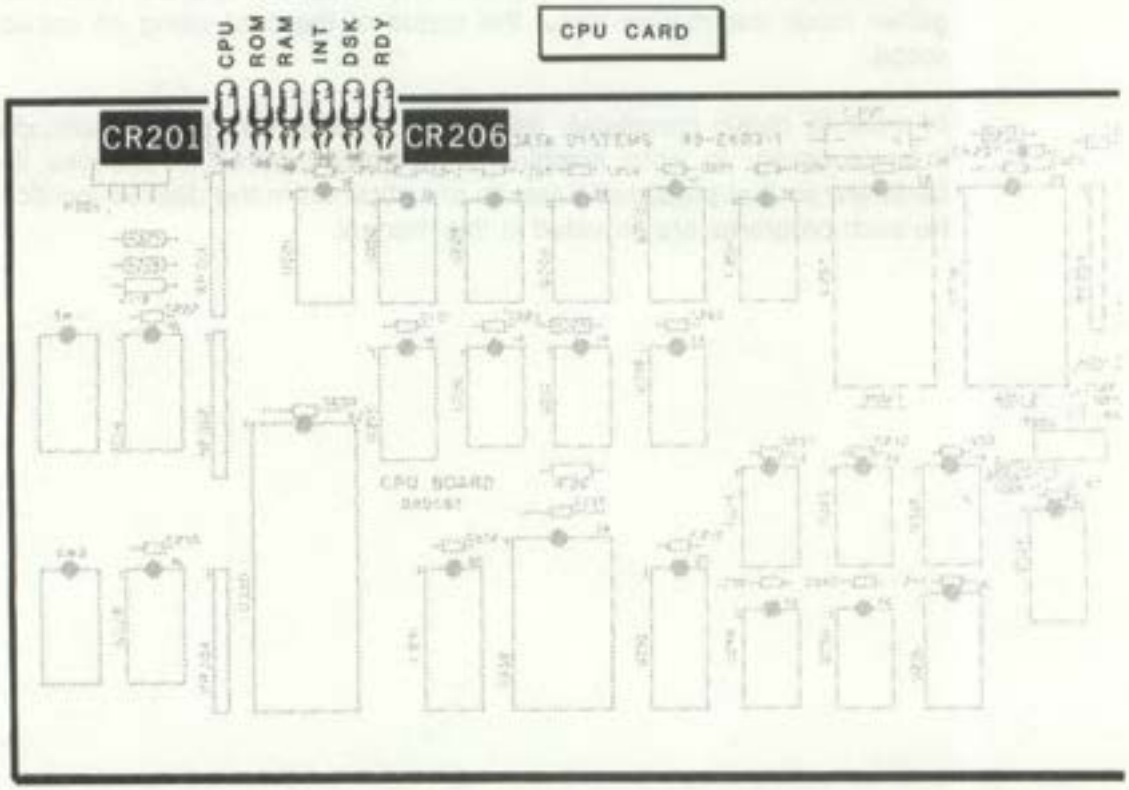


Figure 6.1. CPU LEDs

CPU Troubleshooting

Most of the circuitry on the CPU card is absolutely essential to the operation of all parts of the computer system. In most cases, a failure on the CPU card will prevent system operation. Certain failures will be indicated by either a lit status LED or a CPU failure error message.

A CPU failure error message will be displayed only if there is a partial failure of the microprocessor. If this message is displayed, replace the microprocessor.

A lit CPU LED indicates that either the microprocessor or its associated latches or buffers have failed.

Refer to the documentation supplied with the diagnostic disk (CB-5063-13) for information on the disk-based diagnostic tests.

If the software tests do not work, first check the backplane LEDs (Figure 6.2). All of these LEDs should be lit. The −5 VDC LED indicates a backplane failure. All other LEDs indicate a power supply failure.

Use an oscilloscope to check the outputs of clock generator U211. Pin 12 should have a 14.31818 MHz square wave output, and pin 8 should have a 4.77 MHz square wave output.

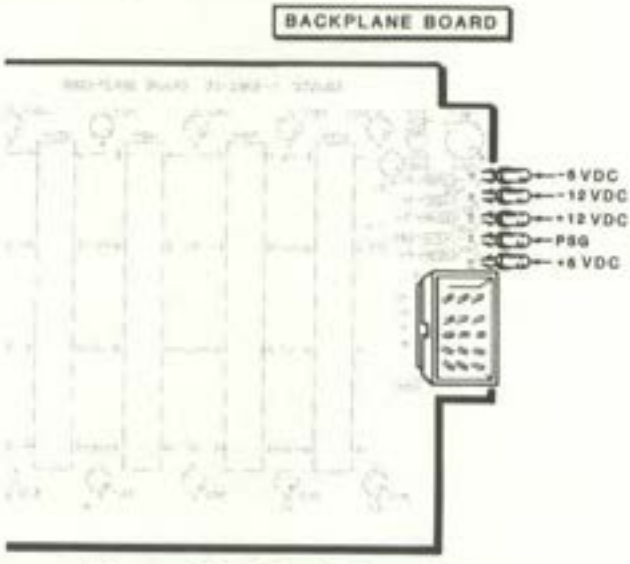


Figure 6.2. Backplane LEDs

Check the outputs from the CPU (U212) against the timing diagram shown in Figure 6.3. Note, however, that this timing diagram illustrates only the read and write functions of the CPU. Some CPU operations are internal and do not require all of the interface signals shown in the diagram. All of the pulses shown in the timing diagram should occur, and they should have the timing with respect to the other signals which is shown. Note that the actual frequency of these pulses is variable.

Pulses also should occur on pins 1 and 11 of the address latches U222, U241, and U242. Transceiver U223 should have pulses of variable frequency on pins 1 and 19.

Pulses should occur, with variable frequency, on all other ICs on the card.

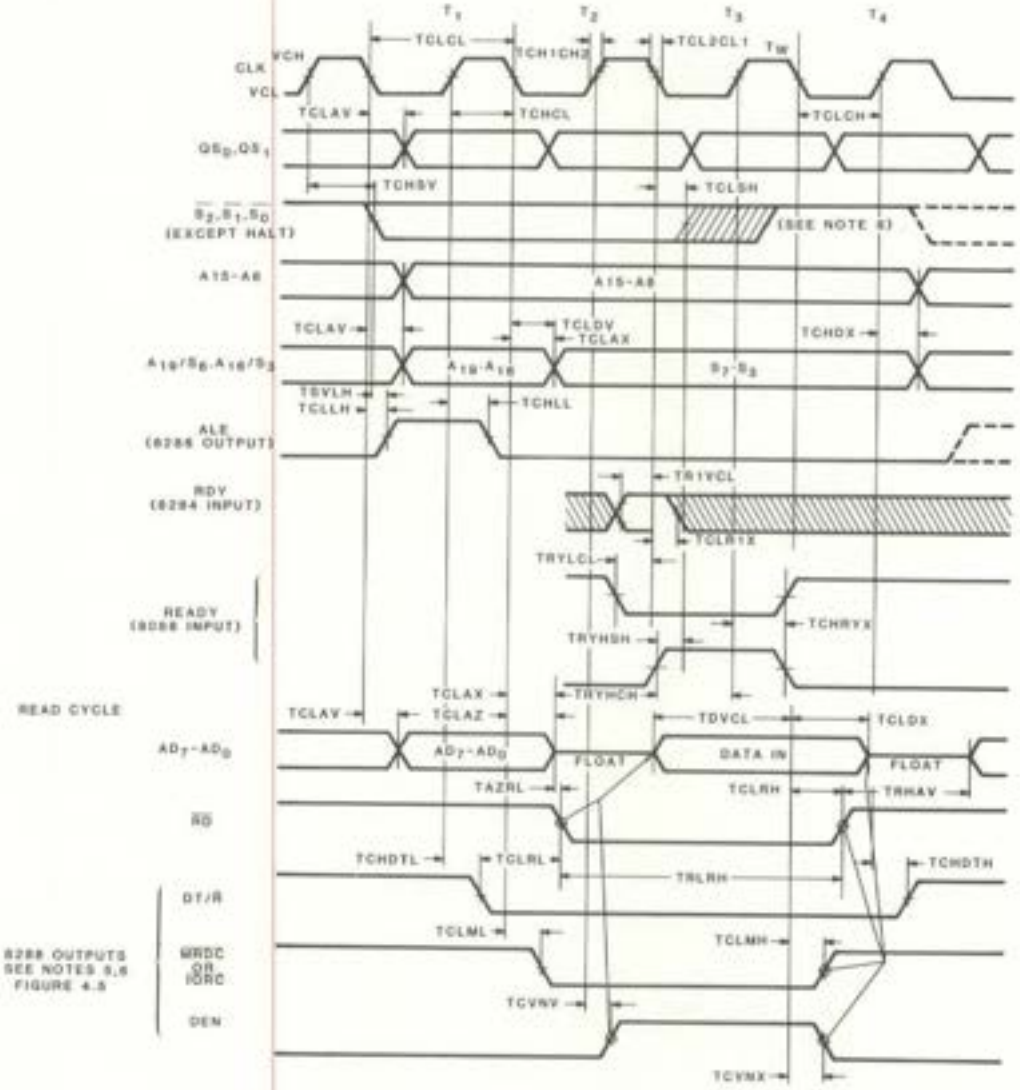
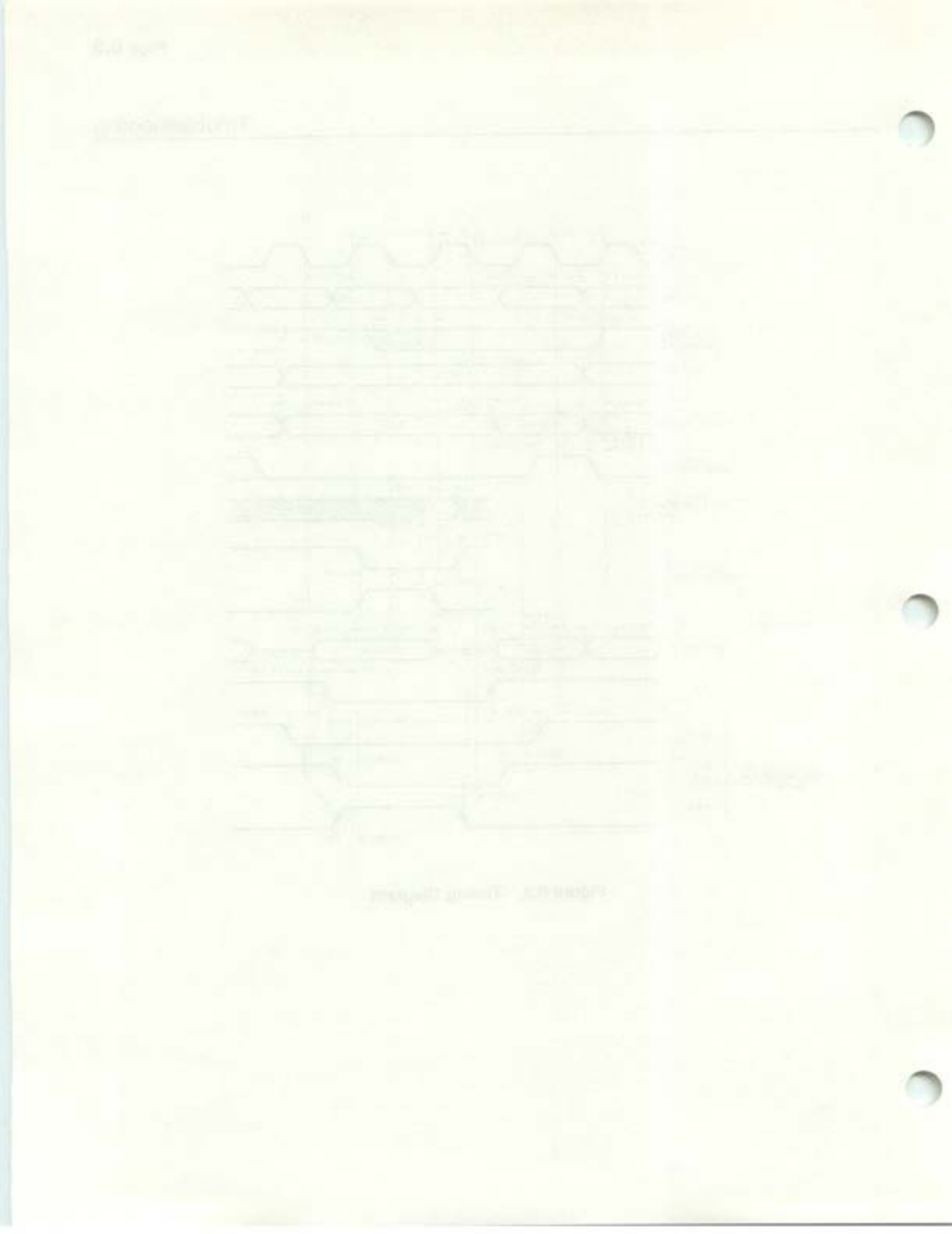


Figure 6.3. Timing Diagram



Chapter 7

CPU Card Parts List

Introduction

This portion of the service module contains a component view of the CPU card (part numbers HE 181-5574, HE 181-4646, HE 181-5442, or HE 181-5059) and the related parts lists. Refer to Figure 7.1 for the location of the parts and components described in this chapter. Refer to Chapter 8, "CPU Semiconductor Identification," for descriptions of semiconductor devices used on these cards.

NOTE: The actual part number is not printed on the card. The card can be identified by the part number of the bare (no components installed) card, which is printed on the card. Card HE 181-4646 and card HE 181-5442 have a bare card part number of 85-3000. Card HE 181-5059 (80C88) has bare card part number 85-3017-1 printed on the card, and card HE 181-5574 has bare card part number 85-2889-1.

NOTE: Cards HE 181-4646 and HE 181-5442 are identical except that all 74LS series components have been replaced by 74ALS series components. Card HE 181-5574 has a static RAM chip installed at U206. The ICs on this and card HE 181-5059 begin at U200, which corresponds with U201 on the other two cards. The component numbers are identical after U206. U231 is not used on any of these cards. Card HE 181-5059 uses the 80C88 and has a flip-flop installed at U231.

CAUTION: This card contains electrostatic-sensitive devices (ESD). Exercise extreme care when handling these devices to prevent damage.

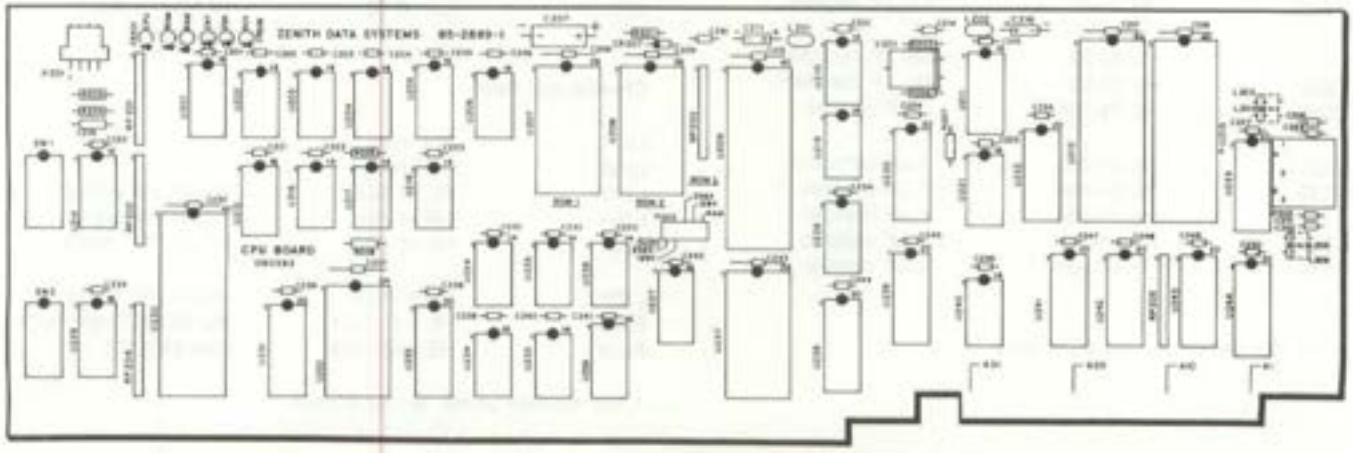


Figure 7.1. CPU Card Component Layout

Parts List

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
Capacitors		
C201	HE 21-786	.1 µF ceramic
C202	HE 21-786	.1 µF ceramic
C203	HE 21-786	.1 µF ceramic
C204	HE 21-786	.1 µF ceramic
C205	HE 21-786	.1 µF ceramic
C206	HE 21-786	.1 µF ceramic
C207	HE 25-940	22 µF electrolytic
C208	HE 21-786	.1 µF ceramic
C209	HE 21-786	.1 µF ceramic
C210	HE 21-786	.1 µF ceramic
C211	HE 25-195	2.2 µF tantalum
C212	HE 21-786	.1 µF ceramic
C213	HE 21-786	.1 µF ceramic
C214	HE 21-786	.1 µF ceramic
C215	HE 21-786	.1 µF ceramic
C216	HE 25-195	2.2 µF tantalum
C217	HE 21-786	.1 µF ceramic
C218	HE 21-786	.1 µF ceramic
C219	HE 21-761	.01 µF glass
C220	HE 21-786	.1 µF ceramic
C221	HE 21-786	.1 µF ceramic
C222	HE 21-786	.1 µF ceramic
C223	HE 21-786	.1 µF ceramic
C224	HE 21-786	.1 µF ceramic
C225	HE 21-786	.1 µF ceramic
C226	HE 21-786	.1 µF ceramic
C227	HE 21-786	.1 µF ceramic
C228	HE 21-43	100 pF ceramic
	or	
	HE 21-22	220 pF ceramic*
C229	HE 21-22	220 pF ceramic
C230	HE 21-786	.1 µF ceramic
C231	HE 21-786	.1 µF ceramic
C232	HE 21-786	.1 µF ceramic
C233	HE 21-786	.1 µF ceramic
C234	HE 21-786	.1 µF ceramic
C235	HE 21-786	.1 µF ceramic

* Not installed on HE 181-5326 card.

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
C236	HE 21-786	.1 µF ceramic
C237	HE 21-786	.1 µF ceramic
C238	HE 21-786	.1 µF ceramic
C239	HE 21-786	.1 µF ceramic
C240	HE 21-786	.1 µF ceramic
C241	HE 21-786	.1 µF ceramic
C242	HE 21-786	.1 µF ceramic
C243	HE 21-786	.1 µF ceramic
C244	HE 21-786	.1 µF ceramic
C245	HE 21-786	.1 µF ceramic
C246	HE 21-786	.1 µF ceramic
C247	HE 21-786	.1 µF ceramic
C248	HE 21-786	.1 µF ceramic
C249	HE 21-786	.1 µF ceramic
C250	HE 21-786	.1 µF ceramic
C251	HE 21-43	100 pF ceramic
	or	
	HE 21-717*	.01 µF ceramic*
C252	HE 21-43	100 pF ceramic
	or	
	HE 21-717*	.01 µF ceramic*
Diodes		
CR201	HE 412-654	LED, red
CR202	HE 412-654	LED, red
CR203	HE 412-654	LED, red
CR204	HE 412-654	LED, red
CR205	HE 412-654	LED, red
CR206	HE 412-654	LED, red
CR207	HE 56-56	10 mA, 75 V, IN4149
Chokes and Pins		
L201	Not Used	
L202	Not Used	
L203	HE 45-629	10 µH, RF choke
L204	HE 45-629	10 µH, RF choke
L205	HE 45-629	10 µH, RF choke
L206	HE 45-629	10 µH, RF choke
P201	HE 432-1231	4M MOLEX right angle
P202	HE 432-1349	10M MOLEX

* Not installed on HE 181-5236 card.

CPU Card Parts List

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
Resistors		
R201	HE 6-103-12	10 KΩ
R202	HE 6-511-12	510 Ω
R203	HE 6-151-12	150 Ω
R204	HE 6-220-12	22 Ω
R205	HE 6-472-12	4.7 KΩ
R206	HE 6-511-12	510 Ω
R207	HE 6-270-12	27 Ω
R208	HE 6-471-12	470 Ω
RP201	HE 9-132	330 Ω resistor pack
RP202	HE 9-133	4.7 KΩ resistor pack
RP203	HE 9-133	4.7 KΩ resistor pack
RP204	HE 9-133	4.7 KΩ resistor pack
RP205	HE 9-155	2.2 KΩ resistor pack
Switches		
SW201	HE 60-657	DIP, SPST
SW202	HE 60-657	DIP, SPST
Integrated Circuits		
U200 (U201)*	HE 443-879*	Flip-flop, hex D*
	HE 443-299	Socket
U201 (U202)	HE 443-769	Shift register, 8-bit*
	HE 434-298	Socket
U202 (U203)	HE 443-1084	Buffer, hex
	HE 443-298	Socket
U203 (U204)	HE 443-1072	OR gate, quad 2-input
	HE 434-298	Socket
	or	
	HE 443-875	OR gate, quad 2-input
	HE 434-298	Socket
U204 (U205)	HE 443-877	Decoder
	HE 434-299	Socket
U205 (U206)	HE 443-800	NOR gate, triple 3-input
	or	
	HE 443-1230	NOR gate, triple 3-input
	HE 434-298	Socket

* Circuit Designator in parentheses applies to the HE 181-4646 and HE 181-5442 cards.

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
Integrated Circuits (Continued)		
U206**	HE 443-1138	Static RAM, 8K × 8
	HE 434-312	Socket
U207****	HE 444-229-8	System monitor ROM 1
	HE 434-312	Socket
U208****	HE 444-260-8	System monitor ROM 2
	HE 434-312	Socket
U209	HE 443-1170	Programmable DMA controller
	HE 434-253	Socket
U210	HE 443-728	NAND gate, quad 2-input
	or	
	HE 443-1080	NAND gate, quad 2-input
	HE 434-298	Socket
U211	HE 443-1011	Clock generator driver
	HE 343-310	Socket
U212	HE 443-1009	8088 Microprocessor
	or	
	HE 443-1228***	80C88 Microprocessor***
	HE 434-253	Socket
U213	HE 443-1168	8087 Coprocessor (Optional)
	HE 434-253	Socket
U214	HE 443-799	Mux, quad 2-input
	HE 434-299	Socket
U215	HE 443-799	Mux quad 2-input
	HE 434-299	Socket
U216	HE 443-967	Inverter, hex
	HE 434-298	Socket
U217	HE 443-730	Flip-flop, dual D
	HE 443-298	Socket
U218	HE 443-730	Flip-flop, dual D
	HE 434-298	Socket

** Not used on cards HE 181-4646 or HE 181-5442.
*** Used on HE 181-5059 card only.
****Must be replaced as a set.

CPU Card Parts List

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
Integrated Circuits (Continued)		
U219	HE 443-780	AND gate, quad 2-input
	or	
	HE 443-1073	AND gate, quad 2-input
	HE 434-298	Socket
U220	HE 443-885	Transceiver
	HE 434-311	Socket
U221	HE 443-1172	Delay element
	HE 434-299	Socket
U222	HE 443-837	Latch, 8-bit 3-state
	HE 434-311	Socket
U223	HE 443-885	Transceiver
	HE 434-311	Socket
U224	HE 443-1047	NAND gate, triple 3-input
	HE 434-298	Socket
U225	HE 443-864	AND gate, triple 3-input
	or	
	HE 443-1078	AND gate, triple 3-input
	HE 434-298	Socket
U226	HE 443-1051	Flip-flop, dual D
	HE 434-298	Socket
U227	HE 443-1053	Flip-flop, hex D
	HE 434-299	Socket
U228	HE 443-1173	Register file, 4 × 4
	HE 434-299	Socket
U229	HE 443-799	Mux, quad 2-input
	HE 434-299	Socket
U230	HE 443-1021	Interface
	HE 434-253	Socket
U231	HE-443-1051****	Flip-flop, dual D****
	HE-434-298****	Socket****
U232	HE 443-1066	Timer, programmable interval
	HE 434-307	Socket
U233	HE 443-754	Buffer, octal 3-state
	HE 434-311	Socket
U234	HE 443-755	Inverter, hex
	or	
	HE 443-1082	Inverter, hex
	HE 434-298	Socket
U235	HE 443-728	NAND gate, quad 2-input
	or	
	HE 443-1080	NAND gate, quad 2-input
	HE 434-298	Socket
U236	**HE 444-228**	**ROM, select**
	HE 434-299	**Socket**
U237	HE 443-1012	Controller, interrupt
	HE 434-312	Socket
U238	HE 443-837	Latch, 8-bit 3-state
	HE 434-311	Socket
U239	HE 443-791	Buffer/driver, 3-state
	HE 434-311	Socket
U240	HE 443-839	Transceiver, quad
	HE 434-298	Socket
U241	HE 443-837	Latch, 8-bit 3-state
	HE 434-311	Socket
U242	HE 443-837	Latch, 8-bit 3-state
	HE 434-311	Socket
U243	HE 443-1169	Controller, bus
	HE 434-311	Socket
U244	HE 443-885	Transceiver
	HE 434-311	Socket

**** Used only on HE 181-5059. Not installed on other cards.

CPU Card Parts List

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
Crystal		
Y1	HE 404-673	Crystal
Jumper		
J201	HE 432-1171	Pin 2M MOLEX
Miscellaneous		
	HE 204-2718	Bracket
	HE 250-1411	Screw, pan head Phillips 4-40 × .250"
	HE 75-139	Insulator
	HE 75-792	Insulator
	HE 250-1408	Screw, pan head 4-AB × .375"

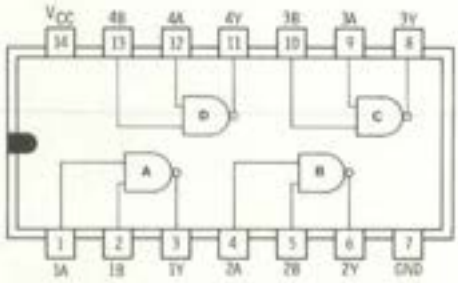
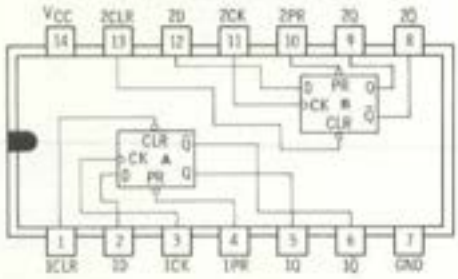
Chapter 8

Semiconductor Identification

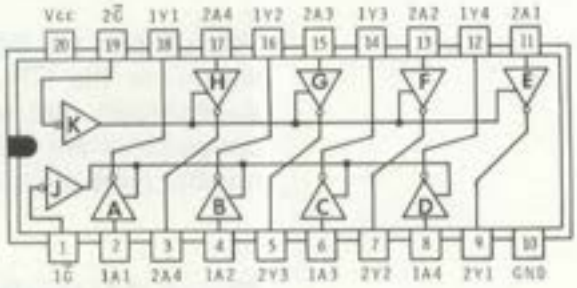
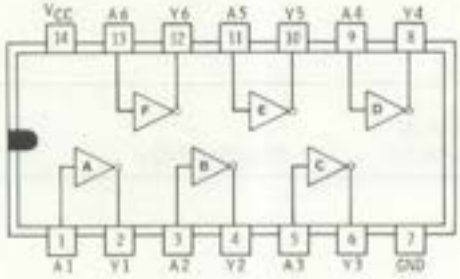
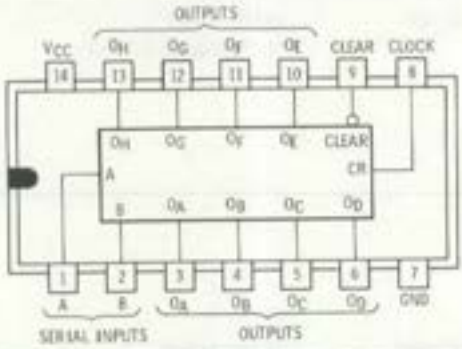
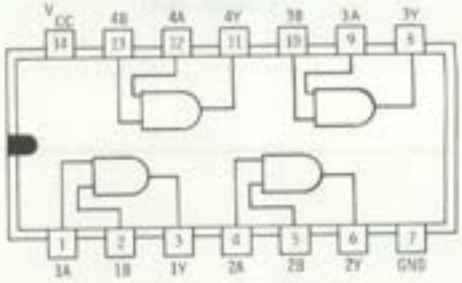
Introduction

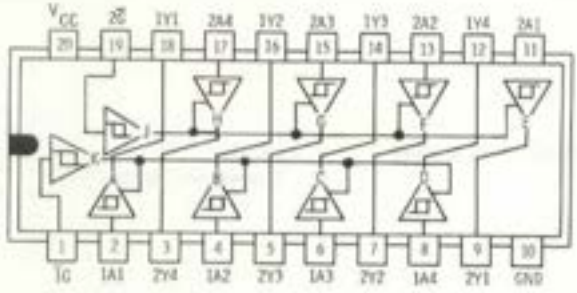
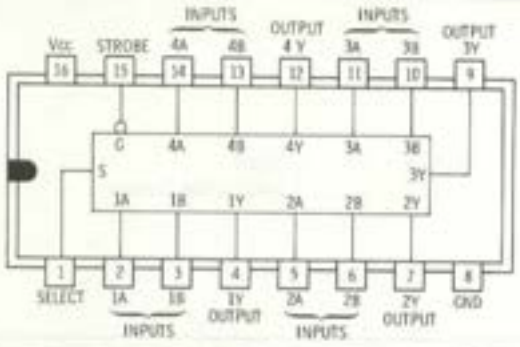
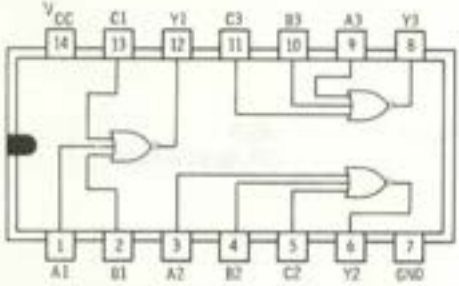
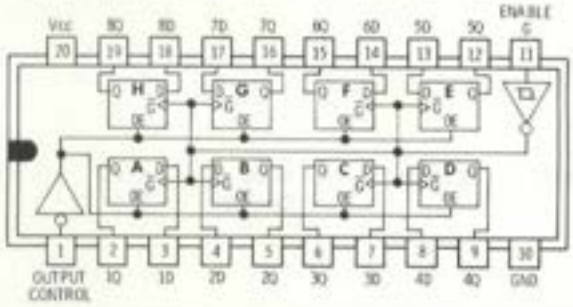
This chapter will help to identify the various semiconductor devices installed on the CPU card by cross-referencing, where applicable, the Zenith/Heath part numbers with generic/alternate device numbers. The components are listed in ascending numerical order, along with device number (where applicable), and device lead configuration.

Part Number Index

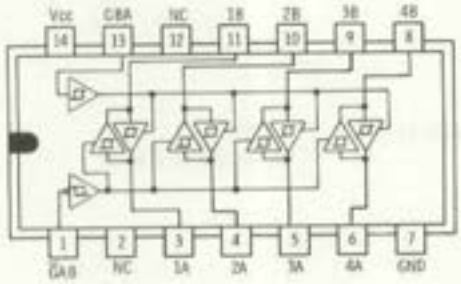
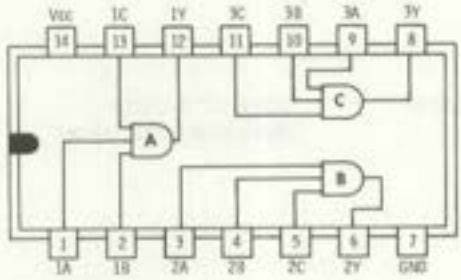
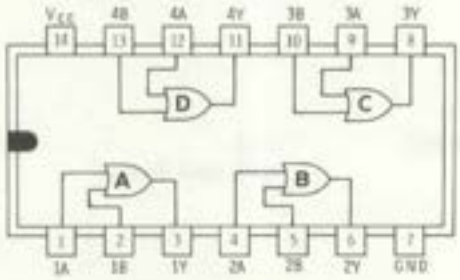
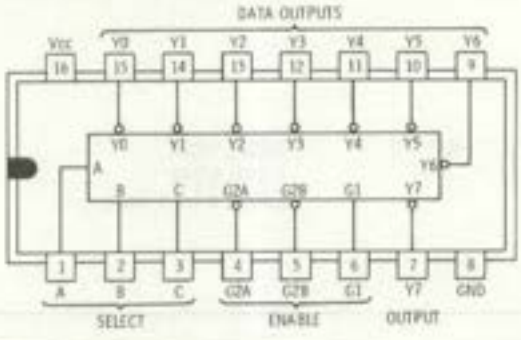
HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
HE 443-728	74LS00	U210, U235 NAND, quad 2-input	
HE 443-730	74IS290	U217, U218 Counter, BCD	

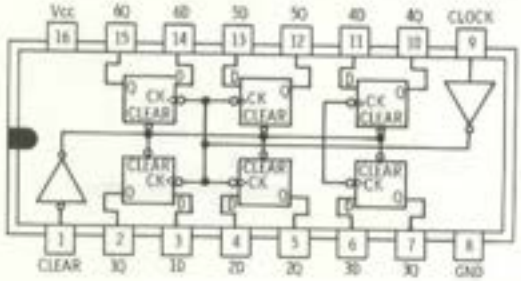
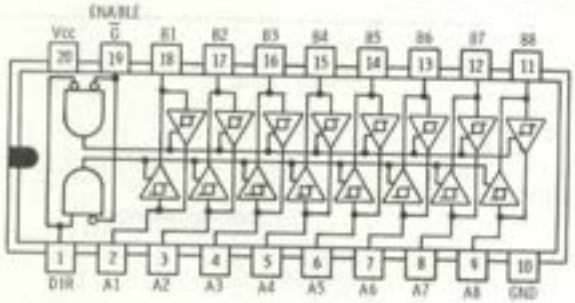
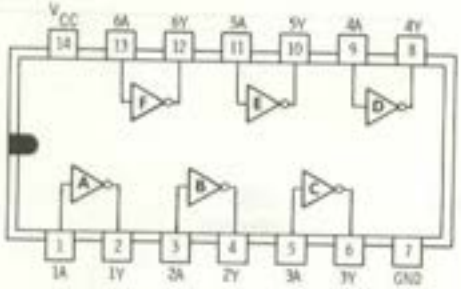
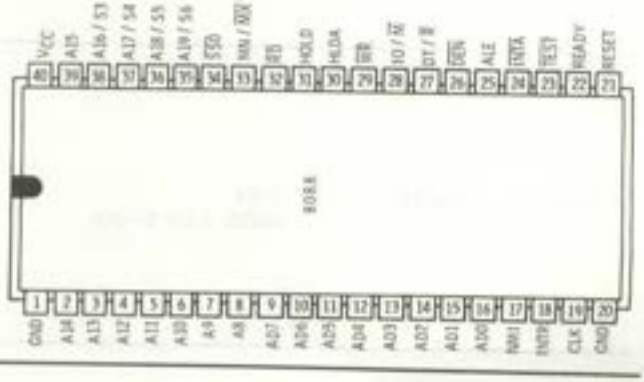
Semiconductor Identification

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
HE 443-754	74LS240	U233 Buffer, octal 3-state	
HE 443-755	74LS04	U234 Inverter, hex	
HE 443-769	74LS164	U201 Shift register, 8-bit	
HE 443-780	74LS08	U219 AND, quad 2-input	

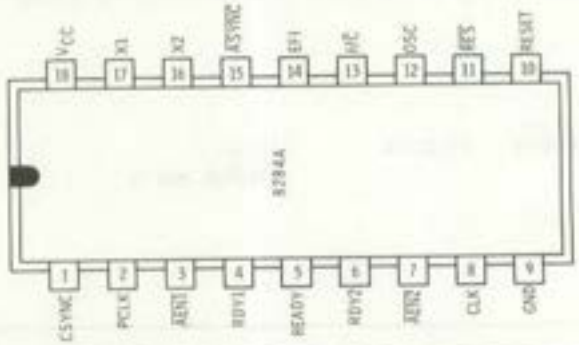
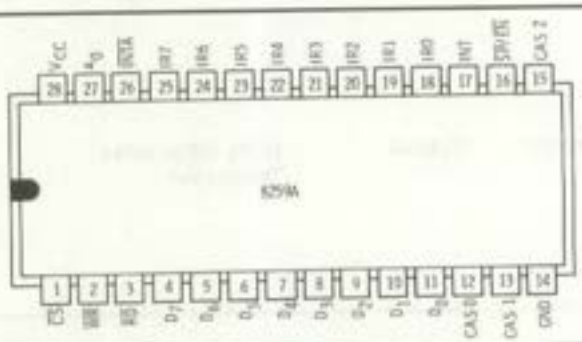
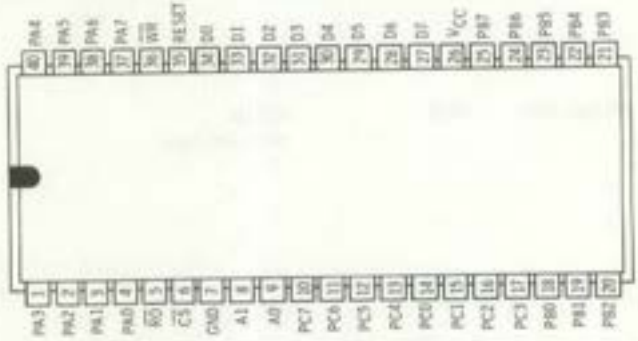
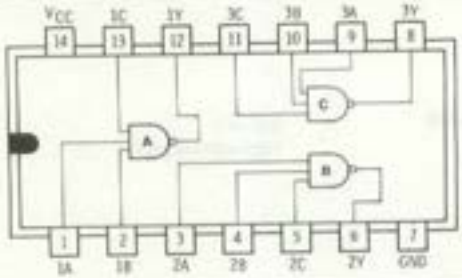
HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
HE 443-791	74LS244	U239 Buffer/driver 3-state	
HE 443-799	74LS157	U214, U215, U229 Multiplexer, quad 2-input	
HE 443-800	74LS27	U205 NOR, triple 3-input	
HE 443-837	74LS373	U222, U238, U241, U242 Latch, 8-bit 3-state	

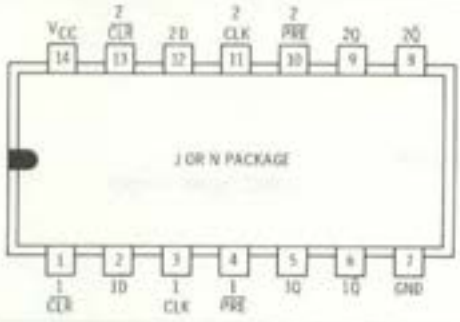
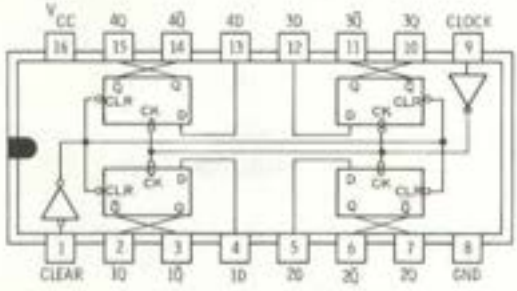
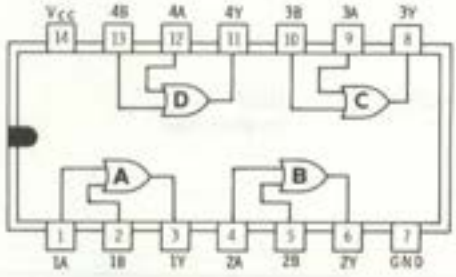
Semiconductor Identification

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
HE 443-839	74LS243	U240 Transceiver, quad	
HE 443-864	74LS11	U225 AND, triple 3-input	
HE 443-875	74LS32	U203 OR, quad 2-input	
HE 443-877	74LS138	U204 Decoder	

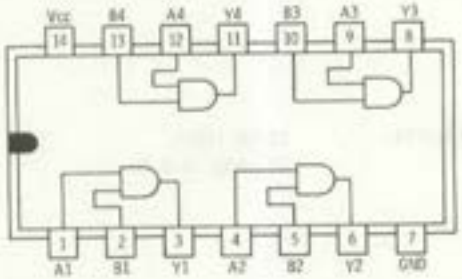
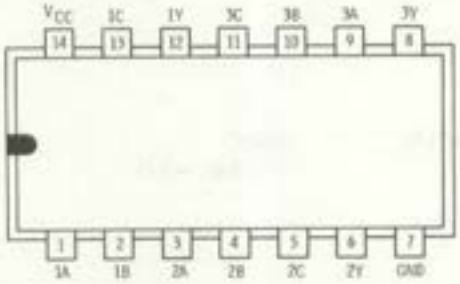
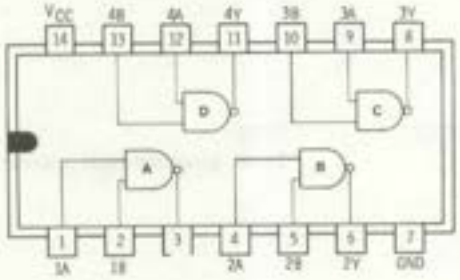
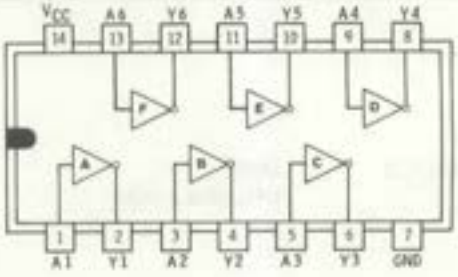
HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
HE 443-879	74LS174	U200 Flip-flop, hex D	
HE 443-885	74LS245	U220, U223, U244 Transceiver	
HE 443-967	7406	U216 Inverter, hex	
HE 443-1009	8088	U212 Microprocessor	

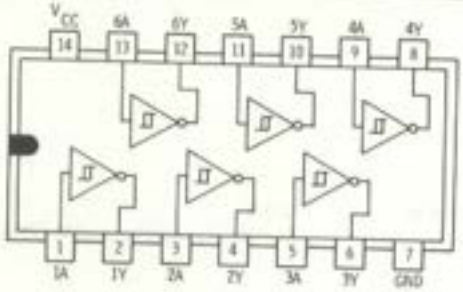
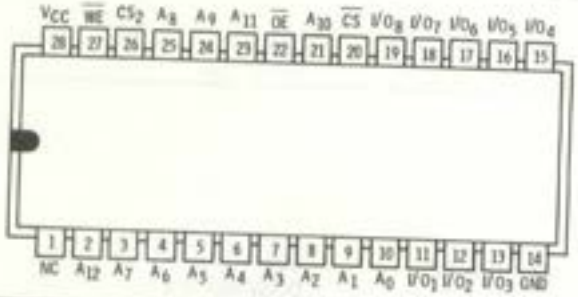
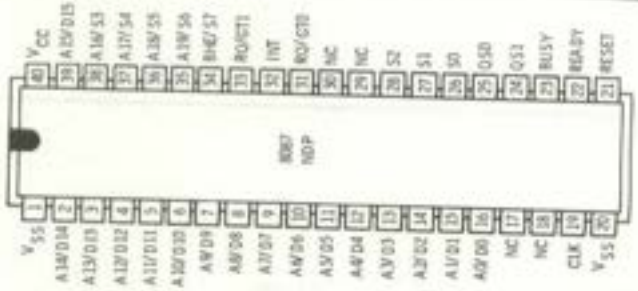
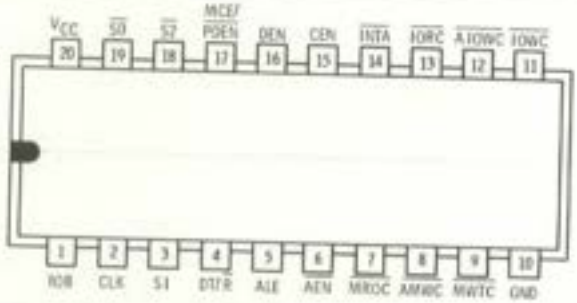
Semiconductor Identification

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
HE 443-1011	8284	U211 Clock generator/driver	
HE 443-1012	8259	U237 Controller, interrupt	
HE 443-1021	8255	U230 Interface	
HE 443-1047	74ALS10	U224 NAND, triple 3-input	

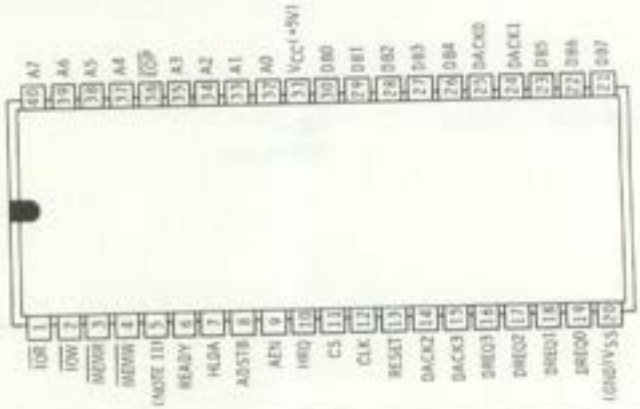
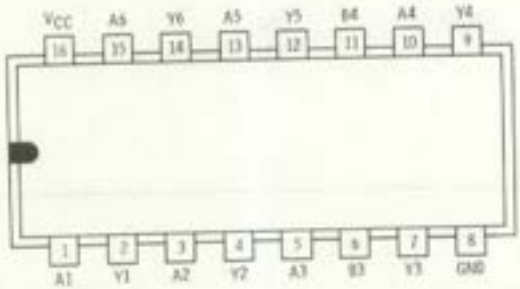
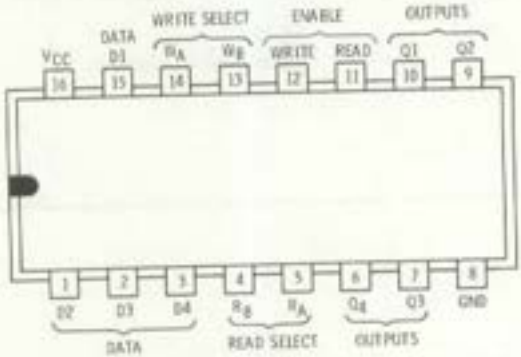
HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
HE 443-1051	74ALS74	U226, U231 Flip-flop, dual D	
HE 443-1053	74S174	U227 Flip-flop, hex D	
HE 443-1066	8253-5	U232 Timer, programmable interval	
HE 443-1072	74ALS32	U203 OR, quad 2-input	

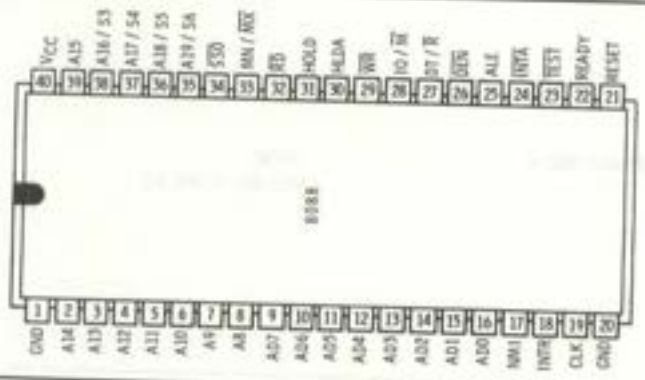
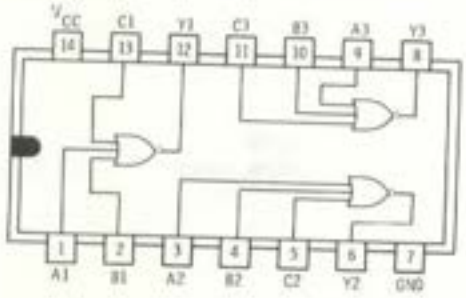
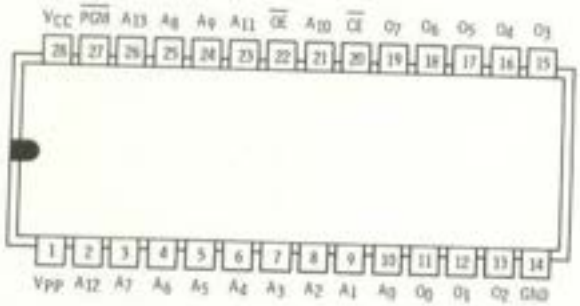
Semiconductor Identification

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
HE 443-1073	74ALS08	U219 AND, quad 2-input	
HE 443-1078	74ALS11	U225 AND, triple 3-input	
HE 443-1080	74ALS00	U235, U210 NAND, quad 2-input	
HE 443-1082	74ALS04	U234 Inverter, hex	

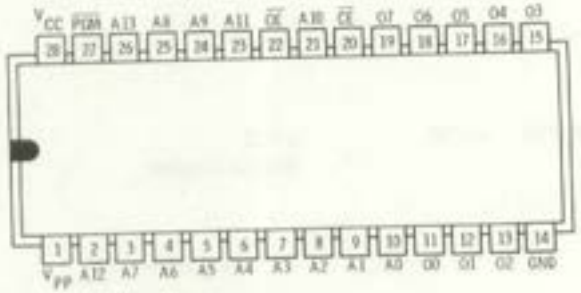
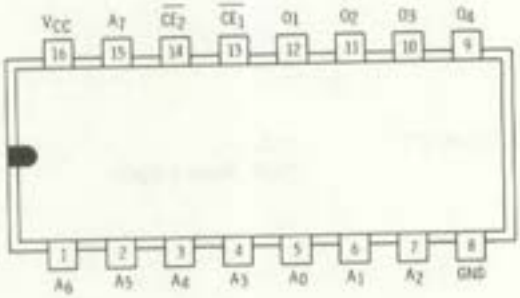
HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
HE 443-1084	74LS19	U202 Buffer, hex	
HE 443-1138	6264P15	U206 RAM, static 8K × 8	
HE 443-1168	8087	U213 Coprocessor, numeric	
HE 443-1169	8288	U243 Controller, bus	

Semiconductor Identification

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
HE 443-1170	8237A-5	U209 Controller, programmable DMA	
HE 443-1172	74LS31	U221 Delay element	
HE 443-1173	74LS670	U228 Register file, 4 × 4	

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
HE 443-1228	80C88	U212 Microprocessor	
HE 443-1230	74ALS27	U205 NOR, triple 3-input	
HE 444-229-4		U207 Monitor ROM #1	

Semiconductor Identification

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
HE 444-260-4		U206 Monitor ROM #2	
HE 444-228		U236 ROM, select	

SERVICE MODULE

Video Card

Z-309

585-67-01

860-45

ZENITH data systems

The purpose of this page is to make sure that all service bulletins are entered in this manual. When a service bulletin is received, annotate the manual and list the information in the record below.

Record of Service Bulletins

SERVICE BULLETIN NUMBER	DATE OF ISSUE	CHANGED PAGE(S)	PURPOSE OF SERVICE BULLETIN	INITIALS

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Abbreviations

ASCII	Americal Standard Code for Information Interchange
Addr	Address
B	Blue
Char	Character
CPU	Central Processing Unit
CRT	Cathode Ray Tube
CRTC	Cathode Ray Tube (monitor) Controller
Dispd	Displayed
G	Green or (buffer) Gate
Hex	Hexadecimal
Horiz	Horizontal
I	Intensity
IC	Integrated Circuit
I/O	Input/Output
K-byte	Kilobyte
LED	Light-Emitting Diode
LSB	Least-Significant Bit
Max	Maximum
MHz	Megahertz
MSB	Most-Significant Bit
PAL	Programmable Array Logic
pF	Picofarad
Pixel	Picture Element
R	Red
RGB	Red, Green, Blue
RAM	Random Access Memory
Reg	Register
RF	Radio Frequency
ROM	Read Only Memory
R/W	Read/Write
Stat	Status
Sync	Synchronization
TTL	Transistor-Transistor Logic
µF	Microfarad
µH	Microhenry
Vert	Vertical
XOR	Exclusive OR

Chapter 1

Introduction and Specifications

The Z-309 Video Card provides an interface between the computer and various display output devices including a monochrome monitor, and an RGB color monitor. An optional light pen also may be interfaced through this card. The monochrome output is connected to an RCA phono jack, and the RGB, or color output, to a 9-pin D-type connector. Both outputs are located on the video card and project through the rear of the computer cabinet. The optional light pen interfaces through a 6-pin connector strip, P302, located on the video card.

The following are features, functions, and capabilities of the video card:

- Addressing, and reading and writing to the 16K video RAM;
- Foreground, background, and border color selection;
- Mode selection (text mode or all-points-addressable graphics);
- A 256-character font ROM;
- 7 or 14 MHz video bandwidth, mode-dependent;
- Monochrome and/or color (RGB) output;
- External vertical, horizontal, and/or composite sync polarity selection;
- Light pen interface;
- Cursor-type selection (block, line, blinking, etc.).

Chapter 2
Configuration

Introduction

This chapter describes the optional functions obtainable through the positioning of the configuration jumpers located on the Z-309 Video Card.

When using the following instructions, should it become necessary to access and/or remove the video card, refer to the base unit cabinet disassembly and video card removal and replacement procedures.

CAUTION: This card contains electrostatic sensitive devices (ESD). Exercise extreme care when handling these devices to prevent damage.

Refer to Figure 9.1 for location of the hardware jumpers mentioned in the following paragraphs.

The seven configuration jumpers located on the video interface card can be used to set initial power-up parameters: to configure sync type and polarity to drive different types of monitors; configure proper input polarity from a light pen device; and to power-on select the desired character font.

Light Pen Polarity

If a light pen with a positive-going pulse output is being used, position J301, the light pen jumper, to "+". If the pen outputs a negative-going pulse, position J301 to "–".

Character Font Selection

Figure 2.1 illustrates the contents of the character font ROM, and the ASCII hexadecimal values which represent them.

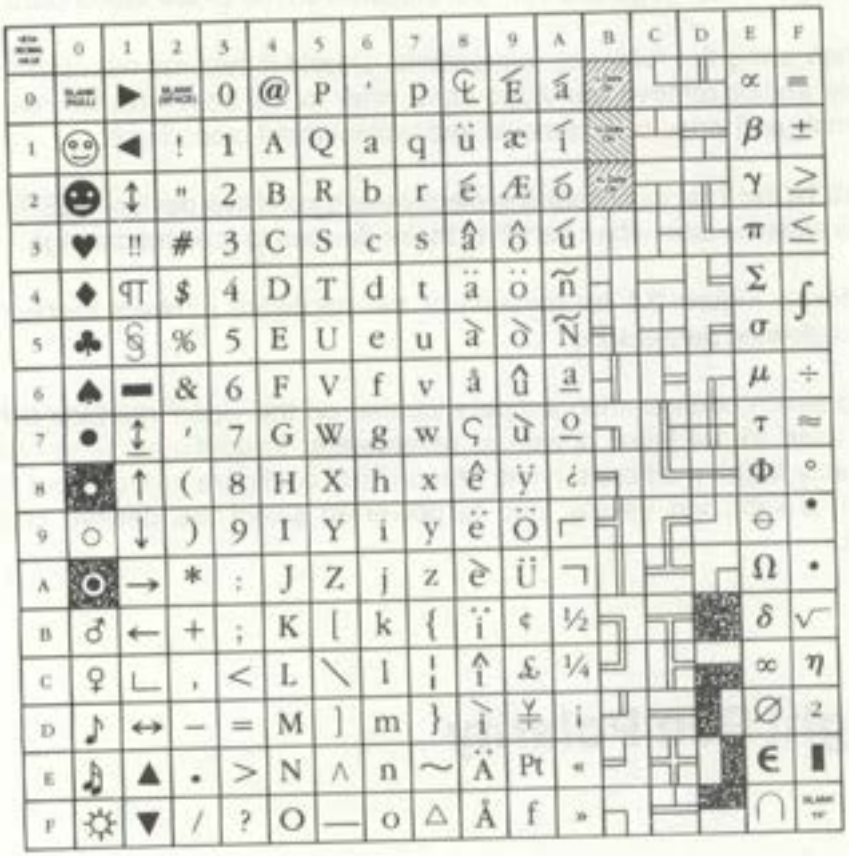


Figure 2.1. Character ROM Contents

J302 and J304 are the character-type selection jumpers. The condition of these jumpers is polled when the computer is first turned on, and will determine whether the characters from the character font ROM are single-dot or double-dot. Position the jumpers to the "0" or "1" markings on the card corresponding to the desired configuration. The following logic (Table 2.1) determines character selection.

Table 2.1. Character Font Selection

J304	J302	CHARACTER FONT
0	0	Double-dot characters
0	1	Reserved
1	0	Single-dot characters
1	1	Reserved

Selection of a "reserved" option will result in a white screen, or selection of a non-desired character type.

Monitor Synchronization

If an RGB monitor which requires composite (horizontal and vertical) sync is being used, position J303 to "C". If the monitor requires separate horizontal and vertical sync, position J303 to "V".

Position J305 to the card markings corresponding to the vertical sync polarity required by the monochrome monitor being used, positive "+" or negative "−".

Position J306 to the card markings corresponding to the horizontal sync polarity required by the RGB monitor being used, positive "+" or negative "−".

Position J307 to the card markings which correspond to the vertical/composite sync polarity required by the RGB monitor being used, positive "+" or negative "−".

Chapter 3

Theory of Operation

The following paragraphs detail the various functions and features of the Z-309 Video Card.

Major Components

Refer to Figure 9.2, the video interface block diagram, for the following descriptions.

CRT Controller

A 6845 CRT controller IC provides the proper drive signals for a raster-scan type CRT. The device is highly programmable with regard to raster and character manipulation, and allows for the implementation of many display modes.

Mode Select and Status Registers

The mode select and status registers on the video card are general purpose programmable input/output (I/O) registers which determine mode of operation, color, and levels of gray on a CRT display.

Display Buffer

The display buffer, which resides in addressable memory at location B8000, incorporates 16K-bytes of dynamic read/write memory. A dual-porting arrangement allows both the CPU and CRT controller equal access to this buffer in all modes of operation, but in case of a conflict, the CRT controller has a higher priority.

Monitor RAM

An additional 16K-bytes of RAM is contained on the video card, and located at F0000 to F3FFF. This RAM is for use by monitor-driven software only, and should not be written to by the user. Strange and unpredictable results in the monitor formatting and displays may occur if data is inadvertently sent to this buffer.

Character Generator

The ROM character generator on the video card, when in text mode, generates characters from dot patterns stored in the ROM. Two character configurations are provided: a 7 × 7 double-dot and a 5 × 7 single-dot width character set. The supplied hardware jumpers may be positioned to enable either of the character types at power up, and 8088 I/O OUT commands may be used to program-select single- or double-dot characters.

Timing Generator

The timing generator creates the timing signals for the 6845 CRT controller and the dynamic display memory. It also handles traffic control between the CPU and CRT controller for display buffer access.

Color Video Encoder

The color video encoder accepts the color and mode-select information along with appropriate timing, dots, and control signals, then generates the color video information. This is sent to the video output circuitry for further processing.

Video Output

The video output circuitry routes the video information to the proper output connector. It sends color dot information to the RGB connector, and generates levels of gray for a monochrome monitor.

Modes of Operation

The video card can be selected to operate in one of two major modes of operation: text mode or all-points-addressable graphics mode. Additional submodes are available within each mode, for either color or monochrome display.

Text Mode

In text mode, the display formats in either a 40-column by 25-line submode, or in an 80-column by 25-line submode. In either submode, characters are formed in an 8 × 8 character matrix. Also, in either submode, the characters take up a 7 × 7 portion of this matrix, with one line of descender for lowercase alphabetical characters. Both uppercase and lowercase characters are available in all modes.

On a monochrome display, reverse video, blinking, and highlighting features, and 16 levels of gray foreground and background shades, on an individual character basis, can be obtained. On an RGB monitor, 16 foreground, background, or border colors, blinking, and highlighting, are available on a per-character basis.

Using 40 × 25 resolution requires 1000 bytes for character information storage, and 1000 bytes for attribute or color information for one screen page of information. Since there are 16K-bytes of video memory, up to 8 pages of screens can be stored in video memory; additionally, since all the video memory is directly addressable by the CPU, extreme flexibility in manipulation of screen contents is obtainable.

Using 25 × 80 format, the same rules apply, but since there are twice as many characters per row at this resolution, 4000 bytes of video memory are required to store one screen. Hence, only 4 screens may be stored at one time.

Text Mode Display Architecture

A two-byte character/attribute format is used to define each character display position. These two bytes are mapped into assigned locations in video RAM (this buffer is part of the video interface, not system memory). Table 3.1 shows the codes assigned to the particular character attribute desired for a monochrome display. The starting address (character byte) must be an even-numbered location.

Table 3.1. Monochrome Character/Attribute Selection

CHARACTER BYTE (M)	ATTRIBUTE BYTE(M + 1)
7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0

	Attribute Byte							
Function	7	6	5	4	3	2	1	0
Normal video	B	0	0	0	I	1	1	1
Reverse video	B	1	1	1	I	0	0	0
Non-display (black)	B	0	0	0	I	0	0	0
Non-display (white)	B	1	1	1	I	1	1	1

If B (bit 7) is logic one, foreground blinks. If I (bit 3) is logic one, foreground is intensified.

Note that bits 0 through 2 and bits 4 through 6 are either all logic ones (white) or all logic zeroes (black), in monochrome submode. All other combinations of these bits are used to obtain the desired foreground and background colors on an RGB monitor, or levels of gray on a monchrome monitor.

Table 3.2 shows the attribute byte breakdown. As before, bits 7 and 3 determine blink and intensity, respectively, of the foreground character.

Table 3.2. Color Attribute Byte Logic

	BACKGROUND			FOREGROUND		
COLOR	6	5	4	2	1	0
Black	0	0	0	0	0	0
Blue	0	0	1	0	0	1
Green	0	1	0	0	1	0
Cyan	0	1	1	0	1	1
Red	1	0	0	1	0	0
Magenta	1	0	1	1	0	1
Brown	1	1	0	1	1	0
Light Gray	1	1	1	1	1	1

Intensified brown is yellow. Intensified light gray is white. Intensified black is dark gray.

Graphics Mode

In graphics mode, two degrees of resolution are available: 320 × 200 and 640 × 200. 640 × 200 resolution is obtainable only as a monochrome display, since the full 16 K-bytes of video memory is needed to define the ON or OFF states of a screenful of pixels (picture elements). If a color other than white is desired for the ON state of a given pixel, one of the 16 border colors may be selected. In the 320 × 200 resolution, each pixel may be one of four colors. This color may be one of the 16 background colors or one of three other colors software-selected from the red/green/brown palette or the cyan/magenta/white palette.

Color (Medium Resolution) Graphics

Pixel information is stored in video memory in two banks of 8000 bytes each, as shown in Figure 3.1, with address B8000 containing color selection data for the pixels in the upper-left corner of the display area. Addresses B8000 to B9F3F contain information for pixels in even-numbered rows 0 through 198, and addresses BA000 to BBF3F for odd-numbered rows 1 through 199.

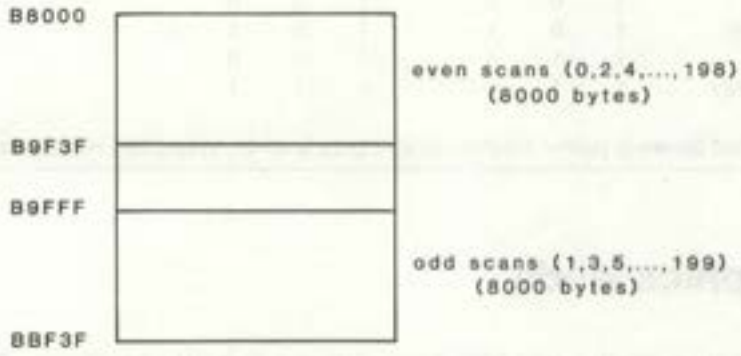


Figure 3.1. Graphics Storage Map

Each video memory byte contains color information for four pixels in two-bit pairs, as in the following format:

7	6	5	4	3	2	1	0
C1	C0	C1	C0	C1	C0	C1	C0

For a given pixel bit-pair composed of bits C0 and C1, the following logic, Table 3.3, determines which color is selected from one of four colors: the current background color or one of the colors from the current palette.

Table 3.3. Color Select Logic

C1	C0	Color select code
0	0	Pixel becomes the current background color
0	1	Pixel becomes color #1 of current palette
1	0	Pixel becomes color #2 of current palette
1	1	Pixel becomes color #3 of current palette

The palettes are structured as follows:

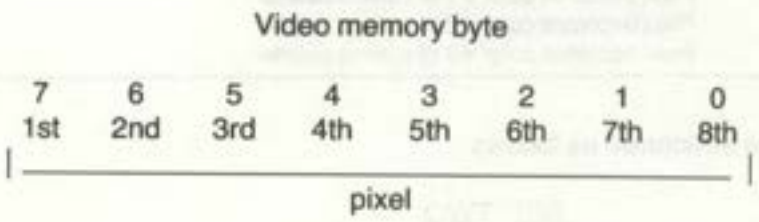
SET ONE	SET TWO
Color 1 – Cyan	Color 1 – Green
Color 2 – Magenta	Color 2 – Red
Color 3 – White	Color 3 – Brown

The possible background colors are the same basic eight colors used in low resolution graphics, plus the lighter shades of these colors which result when intensified, for a total of sixteen colors including black and white (see Table 3.2).

In order to obtain the lighter (intensified) shades, the monitor being used must be capable of recognizing the "I" bit.

High Resolution (640 × 200) Graphics

The high resolution graphics submode, as mentioned previously, may be implemented only in a monochrome format because of memory limitations. Addressing and mapping is the same as medium resolution, but formatting of the data is different. In this submode, each bit, as opposed to a bit-pair, represents a pixel on the screen as shown:



For detailed information on implementing the various modes and submodes, refer to the register descriptions in "Troubleshooting," Chapter 5.

For further details on video card operation, refer to "Detailed Circuit Description," Chapter 4.

Chapter 4

Detailed Circuit Description

General

This chapter covers detailed circuit operation of the Z-309 Video Card.

Before studying this material, read the "Theory of Operation," Chapter 3, for an overall view of video card functions and operations.

Refer to the video card schematic, and the individual schematic breakdowns, Figures 9.3 through 9.12, for each of the following circuit descriptions.

Bus Interface

Refer to Figure 9.3, which shows the manner in which system I/O interfaces with the video card. U359, U360, U361, and U340 are buffers for the I/O signals used by the video card. The backplane edge connector, an integral part of the video card, provides these signals, as well as D0 through D7, the data information, address lines A0 through 19, +12 VDC, +5 VDC, and the I/O CHRDY (ready) signal which is applied to the video timing and control circuitry.

After buffering, the 20 address lines, BA0 through BA19, and BMW*, BMR*, BIOW*, BIOR*, DACK0*, AEN, CLK, RESET*, and OSC are sent out to other portions of the video circuitry.

U358 is a bidirectional data buffer which determines whether data is routed to the video card from the system bus, or to the I/O channel data bus from the video card. Two sections of U303, configured as negative-logic AND gates, and sections of U301 and U347, configured as negative-logic OR gates, determine the direction of data flow, in accordance with the states of the BMR*, BIOR*, AEN, VMEMSEL*, SEL3DX*, and IOAXS* signals.

The G input of U358 will be enabled if either VMEMSEL* or SEL3DX* and IOAXS* are active-low. The direction of data travel is determined by the logic state on the DIR input. When BMR* is low, this DIR line is high and data flows through the buffer from video memory to the I/O bus. When BIOR* and AEN are both low, the DIR line also is low and the data flows from the video card to the bus. If the G input is high, the buffer is isolaied or tri-stated, and data does not transfer in either direction, regardless of DIR state.

+5 VDC is filtered, decoupled, and filtered again by C342, C341, C338, C337, C336, C335, C334, C333, and C301 through C332, before being used as operating power by the video card TTL devices.

Video I/O Ports

The video I/O ports, Figure 9.4, perform video mode selection and status transfer between the video card and the system in accordance with port-select signals routed from the video I/O decoder circuits.

Data lines D0 through D7 provide the values for the various register operations.

Ports 3D8 and 3D9 are output (write) only registers. 3D8 acts as a mode-select register to configure the video interface for the desired operation. This register determines low, medium, or high resolution mode, monochrome or color, and enables or disables the video interface and character blink. Port 3D9 determines color palette in use, and screen border color. It also selects intensified background colors.

The port at 3DA is either read or written to determined by the condition of BIOW* or BIOR* signal. If BIOW* (write) is active-low, U357, the mode-select register is written to. If BIOR* is active-low, the status register, U351, is read from.

Refer to Chapter 5, "Troubleshooting," for details on these register functions.

This video card has only one character font, and J302 and J304 should be positioned accordingly, as described in Chapter 2, "Configuration."

CRT Controller, Buffers, and Latches

Figure 9.5 details the main video control circuit and the character and attribute byte data latches and input buffers.

U337 is the video card CRT controller IC. It uses the signals at its input to select and control desired parameters and video memory addresses.

The input signals to the CRT controller are defined in Chapter 5, "Troubleshooting."

BA3, the buffered address bit 3 signal, in conjunction with SEL3DX, selects the CRT controller. BA0 acts as the CRT controller register select signal.

In addition to video memory addressing information, U337 supplies vertical and horizontal sync timing, character row information, and cursor and display-enable status signals to appropriate circuitry on the video card.

U356 and U354 are the character code data latch and input buffer, respectively. D0 through D7, representing the character code, are written onto the character data bus and into video RAM as CCD0 through CCD7, when U354 is enabled by the write video RAM, WVRAM*, signal.

The character code is read from video RAM as U356 receives an active-high CPU access, (CPUAXS) signal, and an active-low read video character code (RVCC*) signal.

U355 and U353 are the attribute code data latch and input buffer, respectively. Following receipt of the character code, the next D0 through D7 byte representing the attribute code are driven onto the attribute data bus as ATD0 through ATD7, when U353 is enabled by WVRAM*.

The attribute code is read from attribute memory as U355 receives the CPUAXS and read video attribute code (RVAT*) signals.

Bytes always must be written in pairs, the first byte always representing the character code, and the second the attribute code.

Video RAM Address Multiplexers

Figure 9.6 represents the address multiplexers used to access video RAM. U315, U310, U316, and U336 use ADMUX as a bit-group select signal to form the two 8-bit (RAM0 through RAM7) address bytes required to select one of the 16K video RAM locations. Q3P and Q3P* select either the bus (CPU) or the CRT controller as the addressing device.

Bits BA0 through BA13 are the buffered CPU address lines, and MA0 through MA13 the CRT controller lines. Arbitration is determined by Q3P and Q3P*, which are alternately low and high.

U336 is a programmable array logic (PAL) chip configured as a quad 4-to-1 decoder, which uses the GRPH, PSEL, SA11, and SA12, signals to support scrolling operations in the different video modes. Chapter 7 contains the equations which determine the logical functioning of this device.

Video RAM, Data Latches, and Serial Output

Refer to Figure 9.7.

U312 and U308 form the video RAM for character code storage. U309 and U314 store attribute codes. There are 8 K-bytes of RAM available for character code storage, and 8 K-bytes for attribute code storage, resulting in 16 K-bytes total for monitor screen information storage.

Eight K-bytes of each bank are used as scratchpad RAM for ROM-based functions.

To access a given memory location in the character RAM bank, the first 8-bit address byte is latched off the RAM0-RAM7 bus when row-address select signal RASCC*, from the RAM controller, goes low, and is retained as the row-address byte. A few nanoseconds later, the column-address select (CAS*) signal goes low and the next 8-bit byte is fetched, to complete the cycle. The two bytes together determine the desired physical address.

If WVRAM* is low, the D0-D7 data is written into the banks.

The attribute memory banks function in much the same fashion, except that proper timing must be preserved between character and attribute data access. This is accomplished by using RASAT* as the row-address select. The attribute data is retrieved off the ATD0-ATD7 data bus.

Data is applied to U306, the character font ROM IC, and the value represented used to select the desired character from the font. The dot pattern for this character code is then sent to U305, a text mode serializer, which takes the parallel data and translates it to a serial format. The output, a stream of coded character dots, is then sent to the dot synchronizer, part of the timing and control circuitry.

In graphics mode, even-numbered code bits are applied to U328, and odd-numbered bits to U348, to contribute to the forming of the serialized C0 and C1 graphic information.

Data on ATD0 through ATD7, the attribute bus, is applied to U352, the attribute code latch, which picks off the attribute value and sends it to U327, another latch, to U348, which forms the C1 composite serial signal, and to U328, which forms the C0 composite serial signal.

U327, the additional attribute latch, is used to provide proper timing of the attribute bits, AT0 to AT7, in text mode, before application to the color encoder circuitry.

Q0 and Q1* are applied to a negative-logic AND gate, part of U345, the output of which, along with Φ1 and CLR S/R*, becomes the S/L*, CLK, and CLR signals for the three graphic serializer ICs.

U344, a D-type flip-flop, provides the proper blink attribute timing. It uses inputs composed of ATD7, Q1*, and HI-B, on its D, CLK, and PR/CLR lines, respectively.

Video Timing and Control

Figures 9.8 and 9.9 depict the video timing and control circuits. These circuits are responsible for insuring that the video functions occur when they should.

Refer to Figure 9.8. The system OSC signal, which switches at a rate of 14.3 MHz, is the basic timing unit from which are derived the video timing signals.

U331, a divide-by-two counter, derives the 7.15 MHz signal from the system OSC signal, and applies it to U332, the RAM controller logic, and to part of U343 (Figure 9.9), the horizontal sync timing flip-flop.

U332 is the RAM controller logic IC. The logic which dictates its operation is detailed in the PAL equations in Chapter 7. The XCLK signal on pin 12 of this device is derived from either the system 14.3 MHz OSC signal or 7.15 MHz, depending on whether HRES (high resolution) is high or low. Two sections of U307, exclusive ORs, then use the XCLK signal to clock the two timing flip-flops, U335 and U334.

DCLK, the dot clock signal, is the output of an exclusive OR segment of U307, derived from the DOTS signal from U332.

RASCC*, RASAT*, and CAS* are used to select the memory row and column of the video RAM character and attribute banks. ADMUX enables the RAM address multiplexers.

U335 and U334 are two quad D-type flip-flops wired as a multiple counter to provide the video clock timing pulses, Q0, Q1*, Q2*, Q3P*, Q0P*, and Q3P.

Part of U302, U331, U330, and parts of U313 and U323, form the decision circuitry for CPU/CRT controller video memory access. VMEMSEL*, the video memory select signal, after inversion by U302, is applied to the D input of U331, the CLR input of U330, and one input of NAND gate U323. As long as CPUAXS is active-high, U330 Q* is low, and RDY is high. When BMW* goes active-low, and if U331, pin 6, Q* is low, WVRAM* goes active-low, to enable data to enter video RAM.

VMEMSEL*, BMR*, and BA0 together arbitrate between a character or attribute memory read operation, with BA0 used to determine which bank to access. If BA0 is high, the attribute code is read; if low, the character code is fetched.

Refer to Figure 9.9, which shows the horizontal and vertical sync and timing, cursor and display enable, and the dot synchronization and blink control circuits.

U326 is a PAL chip programmed as a video synchronizer. The logic equations which dictate its operation are detailed in Chapter 7. Upon receipt of the proper input signals, U326 generates text dots (A/N DOTS), display enable (delayed), DISPENDLY*, C1 DLY, and C0 DLY for use by the B/I dots color encoder, U325, and the R/G dots color encoder, U324, on Figure 9.11.

U343 is the horizontal sync and timing circuit. It is a binary counter configured to divide the 7.15 MHz signal by 32 to create a 4.76 μsec horizontal sync pulse width. U321 acts as the horizontal start/stop control. Horizontal retrace starts when U321 is clocked active and stops when HSYNC goes low to clear the flip-flop. The resulting output is applied to the D4 input of U333, and the Q4 output eventually becomes the delayed horizontal sync signal for the RGB monitor output.

VSYNC is applied to the D5 input of U333, to emerge from Q5 as the vertical (V) timing signal for the color encoders, and as one of the clock signals for the character and cursor blink generator U322.

CURSOR is inverted and applied to the D0 input of U333. Q0 is fed back to the D1 input and the resultant cursor output from Q1, delayed by two character clocks, is applied to pin 2 of U326 as the cursor delayed, CDLY*, signal.

Display enable (DISPEN) is inverted by U302 and applied to pin 6, the D2 input of U333, and also goes to U351, the status register, as the DISPLAY* signal. The Q2 output of U333 is used as one possible signal source for the CLR S/R* signal, and also is fed back to U333, D3. The Q3 output emerges as the display enable delayed (DDLY*) signal, and supplied to the dot synchronizer and blink controller, from which it emerges as DISPENDLY* for use by the color encoders.

If neither VIDEO EN, nor VIDEO ON is active, the CLR S/R* signal also is issued.

VIDEO ON, VIDEO EN, and COMP SYNC are NORred together to create the BLANK* signal for the color encoding circuitry.

U322 uses the V output of U333 to create the cursor BLINK* and the character CBLINK* signals, and is configured to blink the cursor approximately twice as fast as the characters.

Other inputs to the sync decoder are GATE*, derived from the HI-A signal, DCLK, CDOTS, EBLINK, ATBLINK, Φ1, 640X200, C0, and C1.

Memory and I/O Decoders

Figure 9.10 shows the circuitry for the video RAM and I/O port address decoders.

U362 is a PROM device programmed to act as a memory address decoder. It uses BA15, BA16, BA17, BA18, BA19, and BA14 buffered address lines, and the negative-ORed BMR* and BMW* signal lines, to make its selections. When signal conditions are correct, O3 emerges as the video memory select (VMEMSEL*) signal, and O4 becomes XRAM, scratchpad RAM select.

The read or write decision is made by U321, using system CLK, HI-B, and BIOW* as inputs. The R/W* signal produced is the CRT controller read/write timing signal.

The CRT controller enabling clock (ECLK) signal is produced by U344 based on the input states of CLK, HI-B, BIOW*, and BIOR*. BIOW* and BIOR* are negative-ORed and inverted before application to the CLR and D inputs of the flip-flop. The ORed output, before inversion, becomes the data buffer enable signal, IOAXS* (I/O access), for U303 on Figure 9.3, and also is used as a gate-enable input signal by I/O decoder U329.

Part of U301, U317, and U329 comprise the video I/O port address decoders. BA9 and BA8 are ANDed to become the gate 1, G1, signal for U317. BA5 is G2B and AEN is G2A. BA4, BA6, and BA7 are the actual address selection lines, A, B, and C, for U317. When the status of these signals indicates a valid video I/O port address, the Y7 output becomes the G2B enable for U329. U329 then uses BA0, BA1, BA2, and BA3 to determine the actual video port address. Y7 of U317 also is the SEL3DX* signal used by the CRT controller and bidirectional data bus for I/O read/write decisions.

U330 and two U304 inverters form the interface for an optional light pen. P302, a 6-pin terminal strip, supplies +5 VDC, +12 VDC, and ground to the device. The light pen switch connects to pin 3 to become the LPSW* signal.

The light pen output connects to pin 9 of the strip, is inverted, and applied to pin 3 of J302, the light pen polarity select jumper, and is again inverted and routed to pin 1. In this manner, when a female jumper connector is placed between pin 2 and 3, or between pin 2 and 1, either a negative- or a positive-going light pen pulse is seen by the CLK line of flip-flop U330.

A decoupled +5 VDC signal (HI-B) always is present on the D input, so that as long as valid video addresses cause U329 to prevent lows on the CLR and PR inputs, a pulse from a light pen will clock the flip-flop and generate the LPEN signal for use by the status register and the CRT controller.

Color Video Encoder and Synchronization

Figure 9.11 details the color encoder and video sync generator.

U324 and U325, two PAL devices, generate the encoded color signal, before application to the video timing and output circuits. The functional equations for these devices are detailed in Chapter 7. U324 encodes the red and green signals, and U325, the blue and intensity bits.

C0 DLY, C1 DLY, DISPEN DLY*, GRPH, A/N DOTS, BLANK*, and 640X200 are common inputs to both devices.

Attribute bits AT1, AT2, AT5, and AT6, and the OVERSCAN R and OVERSCAN G signals, determine whether the R (red) or G (green) signals, or both, are output to U338 from the R/G encoder.

Attribute bits AT0, AT3, AT4, and AT7, and the OVERSCAN B and OVERSCAN I signals, determine whether the B (blue) and I (intensity) signals from the B/I encoder are used. The I bit is also dependent on the ON or OFF states of the BGNDI and ENABLINK signals, and the B bit also is dependent on the SELBLUE signal derived from COLORSEL and BW signals.

U338 is responsible for the proper timing of the dot stream to be sent to the video output circuit. The horizontal and vertical sync (H and V) from the video sync circuit, and the dots clock (DCLK) signal are here mixed with the color information and sent out to the video output circuitry.

Video Output

Refer to Figure 9.12 for the description of the video output circuits.

The RDOTS, GDOTS, BDOTS, IDOTS, HSDLY, and VSDLY signals come from U338. From there, the dots signals are buffered, filtered and placed on the 9-pin D-type connector, which is the RGB output interface. The dots signals also are routed to the A, B, and C inputs of U318, an 8-bit demultiplexer.

HSDLY and VSDLY are ORed by U313 and applied to the C terminal of J303, the vertical/composite sync selection jumper, and also to inverter U341, for integration into the composite monochrome signal.

VSDLY also is connected to the V terminal of J303 and exclusive ORed with the internal vertical sync selection jumper, J305. The XORed output of U339 is buffered by part of U363 and connected to pin 5 of P303 for use by an internal display monitor.

HSDLY also is buffered and connects to pin 4 of P303. HSDLY and the HSYNC polarity select jumper, J306, are exclusive ORed and, after inversion and filtering, applied to pin 8 of the RGB video output connector, P304.

J303, the composite/vertical sync selector jumper, and J307, the vertical sync polarity select jumper, are exclusive ORed, inverted, filtered, and connected to pin 9 of P304.

When the dots signals leave U340, they are filtered and placed on pins 3 through 6 of the RGB output connector, P304, for use by the attached RGB monitor.

U318 latches the B, R, and G dots at A, B, and C into an 8-bit format and applies the resultant parallel dot pattern to an octal D flip-flop device, U319. The dot patterns at the Q outputs are inverted by sections of U320 and U341, and injected into the integrating resistor network composed of R303 through R308, which in effect performs a digital-to-analog translation of the signal levels. The IDOTS signal also is buffered and the resultant state integrated into the dot string at U320, pin 2.

The composite video signal comprised of the red, green, blue, and intensity dots, and the composite sync information, is applied to the base of the first video output transistor, Q301. Q301 and Q302 together form a modified Darlington pair for high gain and isolation from the monochrome video output connector. R310 provides a means of setting the black screen level for different monitors. R311 sets the dark-to-light screen area ratio.

C338, C341, and C342, in conjunction with L303, provide further filtering and decoupling of the +5 VDC before use by the video output transistors. R316, R317, L302, C339, and C340 impedance-match the video output and monitor.

Chapter 5

Troubleshooting

General

Use of the information in this chapter assumes that one or more malfunctions have been traced to the Z-309 Video Card, and the power-on, menu-selected, or disk-based diagnostics, or LEDs have not isolated the problem. The information provided here will supplement the procedures provided by the built-in, debugging routines of system ROM. Refer to the "ROM Diagnostics" chapter in the base unit service module for details on the use of these routines.

An abundance of useful information is included in this chapter, which will aid the service technician in troubleshooting problems at nearly any level of difficulty. If problems are encountered that do not appear to warrant the degree of detail presented here, proceed to the general troubleshooting chart at the end of this chapter.

In the following descriptions, all address and register values are given in hexadecimal notation. The term "set" in a given bit position indicates a logic one (1) state. The term "reset" indicates a logic zero (0).

Video Memory

The memory used by the video interface is a self-contained 16K-byte bank with no parity bit. It is used in text mode for storage and retrieval of character and attribute information. In graphics mode, it contains data to define color attributes of the graphics pixels. The buffer address starts at B8000.

CRT Controller

The following paragraphs define the functions and interrelationships of the signals appearing on the pins of the 6845. For more detailed information, refer to the 6845 CRT Controller data sheets in Chapter 8.

The signals fall into three categories: signals which interface the controller with the microprocessor and system busses; signals which interface the controller with the video memory bank and character generator logic; and signals which directly relate to controller/monitor interfacing.

Microprocessor Interface Signals

Table 5.1 defines the signals used to provide communication and data transfer between the video card and the rest of the system.

Table 5.1. Video Card-to-System Interface Signals

SIGNAL	FUNCTION
A0 to A19	The 20 system address lines used to access memory locations.
D0 to D7	Bidirectional data lines which transfer information between the CPU and the internal registers of the 6845.
CS*	Chip Select signal typically generated by system address decoding logic. CS* must be low to read information from, or write information to, one of the 6845 internal registers.
RS	6845 register select signal. Rather than sacrifice five of the 40 available pins to 6845 register-addressing, one of the registers is used as an address register to access the other 18 registers. When the RS signal is low, the address register is accessed and then can be loaded with the address of the internal register to be accessed next. When RS is high, the addressed register may be accessed.
R/W*	The read/write signal. It determines whether data is to be written into or read from an internal register. R/W* is low for a write operation, high for a read operation.
E	The enabling (synchronizing clock) signal required by the 6845 which enables the internal I/O buffers and clocks data into and out of the internal registers via the data buffers. In this computer, the E input connects to the system ECLK signal.
CLK	Synchronizes the 6845's control signals. It is derived from the system clock to become the character rate clock in text mode. Although this signal is more closely related to the character generator and video interface, it is included here because it is the primary timing unit to the 6845.
RESET*	Initializes the 6845. When this pin goes low, the internal counters are cleared and the 6845 outputs go low, effectively stopping the video display operation. As the RESET* signal does not affect the program-accessible counters within the 6845, display may continue when RESET* goes high.
Vcc (+5 V) and Vss (Ground)	Standard TTL power levels which enable proper operation of the video card ICs.

Screen Memory and Character Generator Signals

There are two sets of signals provided by the 6845 to implement screen memory and character generator logic interface. MA0 through MA13 are screen memory address outputs, and RA0 through RA4 are the raster address signals to character generator logic. The 14 screen memory address lines allow the 6845 to address the 16 K-bytes of video memory. The raster address lines are outputs from the 6845's scan line counter required by the character generator logic to determine which scan line of a character row is in progress.

CRT Monitor Signals

HSYNC and VSYNC are standard horizontal and vertical synchronization signals required by the CRT monitor for display stabilization. DISPEN is the display enable signal which goes high whenever the video signal to the CRT is to be active. DISPEN is low during horizontal and vertical retrace, and also could be called the video blanking signal. CURSOR is the cursor enable signal which allows a steady stream of dots to be produced on the CRT screen as a cursor symbol.

LPEN is the light pen strobe input signal which may be used to interface a light pen. A high on the LPEN line signals the 6845 to save the contents of the screen memory address in one of the internal register sets so the microprocessor can subsequently determine the position on the monitor screen at which the light pen was detected.

CRT Controller Registers

The 19 internal registers of the 6845 CRT controller can be software-programmed to define display and control parameters of a raster-scanned monitor. One of these registers, the address register, is used only as a pointer to the addresses of the other 18 registers. The address register is write-only and is loaded from the CPU, using an I/O OUT instruction to the I/O port at 3D4. This register is loaded with the five least-significant bits of the I/O argument.

The other 18 registers are selected by the pointer information in the address register, then the CPU directs the information at address 3D5 to be loaded into the selected register. Transfers of address and parameter information to and from the registers is via data lines D0 through D7.

Programming the Registers

Table 1 in the data sheets illustrates the logic involved in accessing the 6845 internal registers. Table 5.2 defines the individual registers in terms of values contained in them and the results obtained with these values. All values are expressed in hexadecimal.

Table 5.2. CRT Controller Register Functions

					VALUES		
REG. ADDR.	REG. NO.	REG. TYPE	UNITS	REG. STAT.	40 × 25 TEXT	80 × 25 TEXT	GRAPHICS MODE
0	R0	Horiz. Total	Char.	Write	38	71	38
1	R1	Horiz. Dispd.	Char.	Write	28	50	28
2	R2	Horiz. Sync. Position	Char.	Write	2D	5A	2D
3	R3	Horiz. Sync.	Char.	Write	0A	0A	0A
4	R4	Vert. Total	Row	Write	1F	1F	7F
5	R5	Vert. Total Adjust	Scan Line	Write	06	06	06
6	R6	Vert. Dispd.	Row	Write	19	19	64
7	R7	Vert. Sync. Position	Row	Write	1C	1C	70
8	R8	Interlace Mode	—	Write	02	02	02
9	R9	Max. Scan Line Addr.	Scan Line	Write	07	07	01
A	R10	Cursor Start	Scan Line	Write	06	06	06
B	R11	Cursor End	Scan Line	Write	07	07	07
C	R12	Start Addr.	High	Write	00	00	00
D	R13	Start Addr.	Low	Write	00	00	00
E	R14	Cursor Addr.	High	Read/ Write	XX	XX	XX
F	R15	Cursor Addr.	Low	Read/ Write	XX	XX	XX
10	R16	Light Pen	High	Read	XX	XX	XX
11	R17	Light Pen	Low	Read	XX	XX	XX

xx is a hex number from 00 to FF.

The first group of registers, R0 through R3, establishes the horizontal format and timing parameters. Registers R4 through R9 determine vertical format and timing parameters. The remaining registers, R10 through R17, deal with cursor characteristics, screen memory addressing, and the light pen interface. Typically, registers R0 through R11 are loaded when the system is turned on and should not need to be accessed thereafter. The other six registers, R12 through R17, need to be accessed on an ongoing basis during display operations. R12 and R13 establish the 14-bit starting (top-of-page) address of screen memory. The contents of these registers may be manipulated to perform scrolling of the screen contents. R14 and R15 establish the 14-bit cursor address which establishes the cursor symbol position on the screen. R16 and R17 are used only if a light pen is interfaced.

Horizontal Timing and Format Registers

The contents of register R0 determines the total time allotted for one scan line in terms of character clock (CLK) cycles (total of displayed and undisplayed characters minus 1) per horizontal line, thus determining the horizontal sync (HSYNC) frequency.

R1 is the character row register. It is loaded with the total number of characters minus 1 in character clock (CLK) units.

The horizontal sync register, R2, establishes the point at which the HSYNC signal makes its negative-to-positive transition, specified in terms of CLKs. The reference point for the beginning of the HSYNC pulse is the left-most character position displayed on the scan line.

R3, the HSYNC width register, uses only the four least-significant bits of data to establish the duration of the HSYNC pulse in the range of 1 to 16 character clocks. This allows the HSYNC pulse duration to be adjusted to the requirements of the CRT monitor in use.

Figure 5.1 shows the interrelationship between the four horizontal timing and format registers (R0 through R3) in terms of CLK.

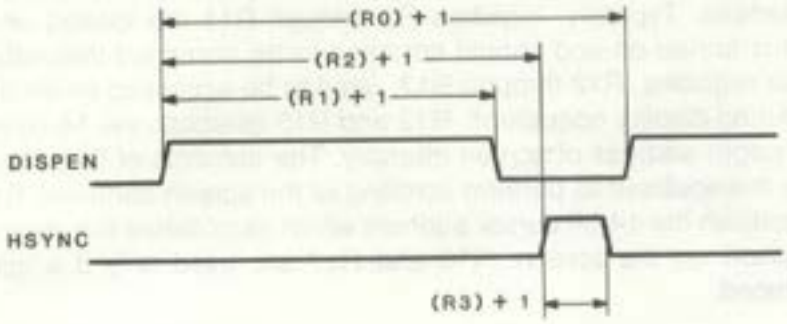


Figure 5.1. Horizontal Timing and Format

Vertical Timing and Format Registers

Registers R4 through R9 are normally loaded at system startup and normally are not changed thereafter. The point of reference for these registers is the top-most character position displayed on the monitor screen.

The vertical total register, R4, and the vertical sync adjust register determine the total number of scan line times in a frame, including vertical retrace, establishing the overall frame rate or VSYNC frequency.

R4 is a 7-bit register loaded with the total number of character rows. Since a character row can consist of up to 32 scan lines, it may be difficult to establish a refresh frequency close to the line frequency. Register R5, a 5-bit VSYNC adjust register, then may be used to fine-tune the VSYNC frequency. R5 is loaded with a value representing scan line times.

The character-rows-displayed register, R6, is a 7-bit register which allows the selection of the number of rows of characters to be displayed, up to 128. What is specified for this register does not determine the positions of the VSYNC pulse, but the point at which display enable (DISPEN) will be reset for vertical retrace.

R7, the vertical sync (VSYNC) position register, determines the point at which the VSYNC signal makes its negative-to-positive transition to initiate vertical retrace. VSYNC position is determined by the character row times, measured from the first character row on the monitor screen. The VSYNC pulse always has a duration of 16 scan lines. Since the scan line frequency will vary from one application to another, and since the VSYNC pulse duration cannot be changed, external circuitry may be needed to achieve a pulse that is compatible with the CRT monitor being used.

The interlace mode register, R8, determines whether interlaced or non-interlaced scan is used.

The value in register R9 determines the number of scan lines per character row. This 5-bit register may be programmed for a character row of up to 32 scan lines. The value used will dictate the maximum count output by the raster address signals (RA0 through RA4) to the character generator logic. Load R9 with the desired scan line count minus 1.

The cursor formatting registers are comprised of the cursor start and cursor stop registers, R10 and R11, respectively. The five least-significant bits of each register determine the scan lines within a character row where the cursor symbol is to be activated. The scan line specified in R10 is the first scan in which the CURSOR signal is to be set and it will remain set until the scan line specified in R11 has been completed. Accordingly, if the cursor symbol is to occupy a single scan line, the same value must be loaded into both registers. If different values are loaded, a block-type cursor will be formed. In interlaced sync and video mode, both registers must be loaded with either odd or even values. Bits 5 and 6 determine whether or not the cursor is to blink, and if so, at either $1/16^{th}$ or $1/32^{th}$ of the field rate. See the data sheets in Chapter 8 for clarification of cursor format programming.

Primary Operating Registers

The remaining six registers, R12 through R17, are considered the primary operating registers since, in the course of display programming, the contents will be changed on an ongoing basis rather than being loaded one-shot at system startup. The six registers are arranged as three 14-bit register pairs (bits 6 and 7 of the most-significant byte are not used).

R12 and R13 comprise the top-of-page register which specifies the screen memory address containing the first character from the top-left corner to be displayed. At the end of each vertical retrace, the first screen memory address generated will be the one contained in these registers. Since the 6845 addresses memory linearly, rather than on a row/column basis, scrolling can be performed on either a character-by-character or row-by-row basis.

The cursor position registers, R14 and R15, generate a cursor signal when the 6845 generates a screen memory address on MA0 through MA13 that matches the contents of this register pair, and when the scan line counter (RA0 through RA4) outputs fall within the limits established by registers R10 and R11. It may be necessary to delay the cursor signal with external logic circuitry to achieve display at the desired position. Cursor movement on the screen is accomplished by loading new values into R14 and R15. These registers are the 6845's only read/write registers so they also can be used to keep track of the cursor position, rather than copying this information from another memory location.

R16 and R17 are the light pen register pair, which will be loaded with the screen memory address corresponding to the screen position at which the LPEN signal was detected. Since there are several critical timing parameters involved with this signal, be sure to carefully study the documentation supplied with this option.

The 6845 CRT controller occupies two I/O port addresses. The RS (register select) line is connected to the least-significant bit, A0. When A0 is reset, the address register is accessed to load it with the register address of the desired parameter, which would then be accessed by setting A0 (RS). A typical register access operation then would consist of two consecutive device write cycles, or a write cycle followed by a read cycle, and these cycles would be directed to consecutive memory or I/O locations.

Color Select Register

The color select register, located at address 3D9, is a 6-bit output-only device (it cannot be read) which can be written to using the I/O OUT command. Only the six least-significant bits of the instruction are used, as shown in Table 5.5.

Table 5.5. Color Select Register Logic

Bit 0	B (blue) border color select (text mode) or 640 X 200 graphics dot color
Bit 1	G (green) border color select (text mode) or 640 X 200 graphics dot color
Bit 2	R (red) border color select (text mode) or 640 X 200 graphics dot color
Bit 3	I (intensity) intensifies border color (text mode) or 640 X 200 graphics dot color
Bit 4	Selects alternate background color palette for medium resolution graphics mode color
Bit 5	320 × 200, graphics color palette selection

Bits 6 and 7 are not used.

Raster Scan Signals

The raster scan outputs, RA0 through RA4, provide the interface between the 6845 and the character generator logic. These outputs may represent scan line counts of from 0 to 31, or up to 32 scan lines per character row. Register R9, the scan lines/row register, determines the maximum count from the scan output registers before reset occurs. Scan line counts are incremented at the HSYNC rate, but also are dependent on the interlace format selected.

Video Card I/O Devices

Table 5.3 defines the I/O devices contained on the video interface.

Table 5.3. Video Card I/O Port Assignments

PORT ADDRESS	REGISTER
3D0	6845
3D1	6845
3D8	Mode Control
3D9	Color Select
3DA	Status/Mode I/O
3DB	Light Pen Latch CLEAR
3DC	Light Pen Latch PRESET

To address a given port, the address lines are programmed as defined in Table 5.4.

Table 5.4. Video I/O Port Selection

PORT	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
3D0	1	1	1	1	0	1	0	X	X	0
3D1	1	1	1	1	0	1	0	X	X	1
3D8	1	1	1	1	0	1	1	0	0	0
3D9	1	1	1	1	0	1	1	0	0	1
3DA	1	1	1	1	0	1	1	0	1	0
3DB	1	1	1	1	0	1	1	0	1	1
3DC	1	1	1	1	0	1	1	1	0	0

X = Don't care

In text mode, bits 0, 1, 2, and 3 determine the screen border color. In 320 × 200 graphics submode, these bits select the screen background color (C0 and C1).

Bit 4, when set, selects an alternate, intensified palette of background colors in text mode, if bit 5 in the mode select register, I/O port 3D8, is reset.

Bit 5 only is used in the 320 × 200 graphics submode to select the active palette of screen display colors. If bit 5 is a logical 1, color is determined by the logic of Table 5.6.

Table 5.6. Palette Number 1 Selection

C1	C0	BACKGROUND COLOR
0	0	Defined by bits 0-3 of I/O port 3D9
0	1	Cyan
1	0	Magenta
1	1	White

If bit 5 is a logical 0, color is determined by the logic of Table 5.7.

Table 5.7. Palette Number 2 Selection

C1	C0	BACKGROUND COLOR
0	0	Defined by bits 0-3 of I/O port 3D9
0	1	Green
1	0	Red
1	1	Brown

Mode Select Registers

The mode select registers are also write-only registers. One is a 6-bit register at port address 3D8; the other is an 8-bit register at 3DA. Both can be written to using I/O OUT commands. The output register at 3D8 functions according to the logic of Table 5.8.

Table 5.8. Mode Select Port 3D8 Logic.

Bit 0	A logical 1 selects 80 × 25 text submode. A logical 0 selects 40 × 25 submode.
Bit 1	A logical 1 selects 320 × 200 graphics submode. A logical 0 selects text mode.
Bit 2	A logical 1 selects monochrome submode. A logical 0 selects color submode.
Bit 3	Disables the video signal during mode changes. The video signal should be re-enabled following a mode change. A logical 1 enables the video.
Bit 4	A logical 1 selects 640 × 200 monochrome graphics submode. Use I/O port 3D9 to select one of eight colors when using a direct drive monitor in this submode.
Bit 5	A logical 1 selects blinking feature in alpha numeric mode (normal setting). A logical 0 intensifies whichever of the 16 background colors is selected to yield a lighter shade of that color.

Bits 6 and 7 are not used.

The register at 3DA functions according to the logic of Table 5. 9.

Table 5.9. Mode-Select Port 3DA Logic.

Bit 0	A logical 1 overrides the VIDEO ENABLE signal from 3D8; will eliminate monitor display flicker when in text mode.
Bit 1	Character font selection. Least-significant bit (LSB).
Bit 2	Character font selection. Most-significant bit (MSB).
Bit 3	Reserved for video diagnostics; used to light the LED located on the video card.
Bit 4	Not defined.
Bit 5	A logical 1 enables fast hardware scrolling in the 80 × 25 submode only.
Bits 6 and 7	Used to select one of four pages of display text from the 16K video RAM according to the following logic:

BIT 7	BIT 6	SCREEN PAGE SELECT
0	0	First page
0	1	Second page
1	0	Third page
1	1	Fourth page

Status Register

The status register, an 8-bit read-only buffer, resides at input port address 3DA. Table 5.10 summarizes the logical operation of this register.

Table 5.10. Status Select Logic

Bit 0	A logical 1 indicates that a horizontal or vertical retrace is in progress. This bit can be used to update the video memory during screen refresh intervals.
Bit 1	A logical 1 in this bit position indicates that a positive-going light pen signal has set the light pen trigger. This trigger is reset at powerup and also may be cleared by issuing an I/O OUT command to port address 3DB. The reset is address-activated; no specific data need be output.
Bit 2	A logical 0 indicates that the light pen switch is on. The switch signal is not latched or debounced.
Bit 3	A logical 1 indicates that a vertical retrace is in progress.
Bit 4	LSB of the character font number.
Bit 5	MSB of the character font number.

Bits 6 and 7 are not used.

Programming Sequence

In general, observe the following sequence when selecting operating parameters for the video interface:

1. Determine desired mode of operation, text mode, or all-points-addressable graphics.
2. Reset video enable bit. Also reset video override bit 0 in port address 3DA if not already reset.
3. Program the CRT controller to desired mode.
4. Determine desired submode(s), then program mode and color select registers.
5. Set video enable bit. Also set the video override bit, if desired.

Video Output Adjustments

The following paragraphs detail the procedure for setting the video output black level and contrast.

Connect the oscilloscope vertical input to the monochrome video output connector, J308. Connect oscilloscope external sync input to pin 5 of P301, HSDLY. Obtain a stable waveform resembling Figure 5.2. Be sure black and white (not intensified white) characters are displayed.

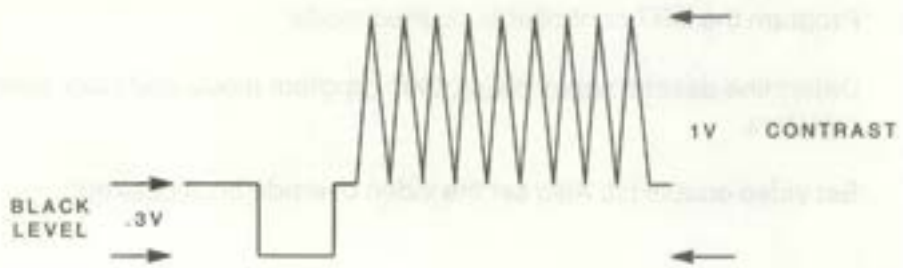


Figure 5.2. Video Output Adjustment Waveform

Adjust black level control, R310, for a pulse height of .3 volt. Then adjust the contrast control, R311, for a peak waveform height of 1 volt. The adjustments may be slightly interactive, so repeat these two operations as necessary to obtain the specified results.

Troubleshooting Table

NOTE: Use of the Disk-Based Diagnostics package, if available, is recommended for troubleshooting.

Table 5.11 lists some problems that may be encountered and some possible causes.

Table 5.11. Troubleshooting Chart

PROBLEM	POSSIBLE CAUSE
System dies when card inserted.	U330, U331, U351, U359-U361, U340, U358
No video dots.	Q301, Q302, U319, U338, U324, U325, U326, U305, U306, U311, U312, U308
Horizontal sync problems. (Starting characters off the left of screen, or first line does not start on the left side of the screen.)	U318, U339, U363, J306
Vertical sync problems. (Rolling or starting point off the top of the screen.)	J305, J307, U318, U339, U341
No monochrome vertical or horizontal sync.	U313, U341, U337
No horizontal or vertical sync.	U338, U333, U341, U336, U337, U339
No horizontal sync.	U301, U321, U343, U302, U337
Mismatched colors and intensity of colors missing.	U309, U314, U318, U319, U324, U325, U338, U340
Background colors bad.	U324, U325, U327, U352, U309, U314, U350
No RAM data output.	U332, U334, U335, U307, U362, U359, U360, U361, U308, U309, U312, U314
Cursor not blinking.	U332
Wrong font or white screen.	J304, U317, U329, U357, U358
No dots in the graphics mode or wrong dot data.	U348, U328, U332, U307
Duplicate data.	U310, U359, U315, U360, U315, U316, U336
Random characters and attributes.	U353, U354, U355, U356, U308, U309, U312, U314

Video Timing

Figure 9.13 shows the timing relationships between the various video signals. Use of this chart will be of great help when isolating time-related video card malfunctions.

Chapter 6

309 Video Card Component Parts List

Introduction

This portion of the service module contains a component view of the Z-309 Video Card and related parts list. Refer to Figure 9.14 for location of parts and components.

CAUTION: This card contains electrostatic-sensitive devices (ESD). Exercise extreme care when handling these devices to prevent damage.

Refer to Chapter 7, "Semiconductor Identification," or to the data sheets in Chapter 8 for descriptions of semiconductor devices.

Parts List

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
Capacitors		
C301	HE 21-786	.1 µF ceramic
C302	HE 21-786	.1 µF ceramic
C303	HE 21-786	.1 µF ceramic
C304	HE 21-786	.1 µF ceramic
C305	HE 21-786	.1 µF ceramic
C306	HE 21-786	.1 µF ceramic
C307	HE 21-786	.1 µF ceramic
C308	HE 21-786	.1 µF ceramic
C309	HE 21-786	.1 µF ceramic
C310	HE 21-786	.1 µF ceramic
Capacitors (Continued)		
C311	HE 21-786	.1 µF ceramic
C312	HE 21-786	.1 µF ceramic
C313	HE 21-786	.1 µF ceramic
C314	HE 21-786	.1 µF ceramic
C315	HE 21-786	.1 µF ceramic
C316	HE 21-786	.1 µF ceramic
C317	HE 21-786	.1 µF ceramic
C318	HE 21-786	.1 µF ceramic
C319	HE 21-786	.1 µF ceramic
C320	HE 21-786	.1 µF ceramic

309 Video Card Component Parts List

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
Capacitors (Continued)		
C321	HE 21-786	.1 µF ceramic
C322	HE 21-786	.1 µF ceramic
C323	HE 21-786	.1 µF ceramic
C324	HE 21-786	.1 µF ceramic
C325	HE 21-786	.1 µF ceramic
C326	HE 21-786	.1 µF ceramic
C327	HE 21-786	.1 µF ceramic
C328	HE 21-786	.1 µF ceramic
C329	HE 21-786	.1 µF ceramic
C330	HE 21-786	.1 µF ceramic
C331	HE 21-786	.1 µF ceramic
C332	HE 21-786	.1 µF ceramic
C333	HE 25-820	10 µF electrolytic
C334	HE 21-197	1 µF tantalum
C335	HE 21-786	.1 µF ceramic
C336	HE 25-820	10 µF electrolytic
C337	HE 25-820	10 µF electrolytic
C338	HE 21-786	.1 µF ceramic
C339	HE 21-804	56 pF ceramic
C340	HE 21-804	56 pF ceramic
C341	HE 25-197	1 µF tantalum
C342	HE 25-820	10 µF electrolytic
C343	HE 21-804	56 pF ceramic
C344	HE 21-804	56 pF ceramic
C345	HE 21-804	56 pF ceramic
C346	HE 21-804	56 pF ceramic
C347	HE 21-804	56 pF ceramic
C348	HE 21-804	56 pF ceramic
C349	HE 21-804	56 pF ceramic
C350	HE 21-804	56 pF ceramic
C351	HE 21-804	56 pF ceramic
C352	HE 21-804	56 pF ceramic
C353	HE 21-804	56 pF ceramic
C354	HE 21-804	56 pF ceramic
Diodes		
CR301	HE 412-654	LED, red

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
Chokes and Pins		
L301	HE 235-229	Choke, RF, 35 µH
L302	HE 45-73	Choke, RF, 2.2 µH
L303	HE 235-229	Choke, RF, 35 µH
L304	HE 45-73	Choke, RF, 2.2 µH
L305	HE 45-73	Choke, RF, 2.2 µH
L306	HE 45-73	Choke, RF, 2.2 µH
L307	HE 45-73	Choke, RF, 2.2 µH
L308	HE 45-73	Choke, RF, 2.2 µH
L309	HE 45-73	Choke, RF, 2.2 µH
P301	HE 432-1268	Pin, 8M Molex
P302	HE 432-1368	Pin, 6M Molex
P303	HE 432-1082	Pin, 5M Molex
P304	HE 432-1358	9-pin "D"
Integrated Circuits		
U301	HE 443-816	AND, quad
	HE 434-298	Socket
U302	HE 443-755	Inverter, hex
	HE 434-298	Socket
U303	HE 443-875	OR, quad
	or	
	HE-443-1072	
	HE 434-298	Socket
U304	HE 443-755	Inverter, hex
	HE 434-298	Socket
U305	HE 443-892	Shift register
	HE 434-299	Socket
U306	HE 444-230	Character ROM
	or	
	HE 444-230-1	
	HE 434-307	Socket
U307	HE 443-915	XOR, quad
	HE 434-298	Socket
U308	HE 443-1165	RAM, dynamic, 16 K × 4
	HE 434-310	Socket
U309	HE 443-1165	RAM, dynamic, 16 K × 4
	HE 434-310	Socket
U310	HE 443-1037	Selector, quad, 2 to 1
	HE 434-299	Socket

309 Video Card Component Parts List

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
Integraged Circuits (Continued)		
U311	HE 443-1031	Flip-flop, octal, D
	HE 434-311	Socket
U312	HE 443-1165	RAM, dynamic, 16 K × 4
	HE 434-310	Socket
U313	HE 443-875 or HE 443-1072	OR, quad
	HE 434-298	Socket
U314	HE 443-1165	RAM, dynamic, 16 K × 4
	HE 434-310	Socket
U315	HE 443-1037	Selector, quad, 2 to 1
	HE 434-299	Socket
U316	HE 443-1037	Selector, quad, 2 to 1
	HE 434-299	Socket
U317	HE 443-877	Decoder
	HE 434-299	Socket
U318	HE 443-804	Latch, 8-bit
	HE 434-299	Socket
U319	HE 443-805	Flip-flop, octal, D
	HE 434-311	Socket
U320	HE 443-967	Inverter, hex
	HE 434-298	Socket
U321	HE 443-1051	Flip-flop, octal, D
	HE 434-298	Socket
U322	HE 443-973	Counter, binary
	HE 434-298	Socket
U323	HE 443-1034	Buffer, quad, NAND
	HE 434-298	Socket
U324	HE 444-233	Generator, dots, R/G
	HE 434-311	Socket
U325	HE 444-234	Generator, dots, B/I
	HE 434-311	Socket
U326	HE 444-232	Video sync
	HE 434-311	Socket
U327	HE 443-1031	Flip-flop, octal, D
	HE 434-311	Socket
U328	HE 443-892	Register
	HE 434-299	Socket
U329	HE 443-877	Decoder
	HE 434-299	Socket
U330	HE 443-1051	Flip-flop, octal, D
	HE 434-298	Socket
U331	HE 443-1051	Flip-flop, octal, D
	HE 434-298	Socket
U332	HE 444-235	PAL, RAM control
	HE 434-311	Socket
U333	HE 443-879	Flip-flop, hex, D
	HE 434-299	Socket
U334	HE 443-983	Flip-flop, quad, D
	HE 434-299	Socket
U335	HE 443-983	Flip-flop, quad, D
	HE 434-299	Socket
U336	HE 444-231	Multiplexer, scroll
	HE 434-311	Socket
U337	HE 443-906	Controller, CRT
	HE 434-253	Socket
U338	HE 443-1053	Flip-flop, hex, D
	HE 434-299	Socket
U339	HE 443-891	XOR, quad, 2-input, 8-bit
	HE 434-298	Socket
U340	HE 443-1058	Buffer, octal
	HE 434-311	Socket
U341	HE 443-967	Inverter, hex
	HE 434-298	Socket
U342	Not used	
U343	HE 443-973	Counter, binary
	HE 434-298	Socket
U344	HE 443-1051	Flip-flop, dual, D
	HE 434-298	Socket
U345	HE 443-875	OR, quad
	HE 434-298	Socket
U346	HE 443-779	NOR, quad, 2-input
	HE 434-298	Socket
U347	HE 443-780	AND, quad, 2-input
	HE 434-298	Socket
U348	HE 443-892	Register
	HE 434-299	Socket
U349	HE 443-1166	Flip-flop, hex, D
	HE 434-299	Socket
U350	HE 443-1166	Flip-flop, hex, D
	HE 434-299	Socket
U351	HE 443-1058	Buffer, octal
	HE 434-311	Socket

309 Video Card Component Parts List

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
Integrated Circuits (Continued)		
U352	HE 443-1031	Flip-flop, octal, D
	HE 434-311	Socket
U353	HE 443-1058	Buffer, octal
	HE 434-311	Socket
U354	HE 443-1058	Buffer, octal
	HE 434-311	Socket
U355	HE 443-1070	Transport latch, octal, D
	HE 434-311	Socket
U356	HE 443-1070	Transport latch, octal, D
	HE 434-311	Socket
U357	HE 443-1098	Flip-flop, octal, tri-state
	HE 434-311	Socket
U358	HE 443-1097	Transceiver, octal, tri-state
	HE 434-311	Socket
U359	HE 443-1058	Buffer, octal
	HE 434-311	Socket
U360	HE 443-1058	Buffer, octal
	HE 434-311	Socket
U361	HE 443-1058	Buffer, octal
	HE 434-311	Socket
U362	HE 444-287	PROM, decoder, video address
	HE 434-299	Socket
U363	HE 443-1020	Buffer, hex
	HE 434-298	Socket
Interfaces and Jumpers		
J301	HE 432-1102	Pin, 3M MOLEX
	HE 432-1041	Pin, 2F BERG
J302	HE 432-1102	Pin, 3M MOLEX
	HE 432-1041	Pin, 2F BERG
J303	HE 432-1102	Pin, 3M MOLEX
	HE 432-1041	Pin, 2F BERG
J304	HE 432-1102	Pin, 3M MOLEX
	HE 432-1041	Pin, 2F BERG
J305	HE 432-1102	Pin, 3M MOLEX
	HE 432-1041	Pin, 2F BERG
J306	HE 432-1102	Pin, 3M MOLEX
	HE 432-1041	Pin, 2F BERG

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
Interfaces and Jumpers (Continued)		
J307	HE 432-1102	Pin, 3M MOLEX
	HE 432-1041	Pin, 2F BERG
J308	HE 434-107	Plug, phono
Resistors		
R301	HE 6-102-12	1 KΩ, film
R302	HE 6-181-12	180 Ω, film
R303	HE 6-621-12	620 Ω, film
R304	HE 6-221-12	220 Ω, film
R305	HE 6-390-12	39 Ω, film
R306	HE 6-330-12	33 Ω, film
R307	HE 6-111-12	110 Ω, film
R308	HE 6-470-12	47 Ω, film
R309	HE 6-6499-12	64.9 Ω, film
R310	HE 10-1191	100 Ω, control, linear
R311	HE 10-1204	1 KΩ, control, linear
R312	HE 6-270-12	27 Ω, film
R313	HE 6-270-12	27 Ω, film
R314	HE 6-151-12	150 Ω, film
R315	HE 6-270-12	27 Ω, film
R316	HE 6-102-12	1 KΩ, film
R317	HE 6-470-12	47 Ω, film
R318	HE 6-102-12	1 KΩ, film
R319	HE 6-102-12	1 KΩ, film
R320	HE 6-102-12	1 KΩ, film
R321	HE 6-102-12	1 KΩ, film
R322	HE 6-102-12	1 KΩ, film
R323	HE 6-102-12	1 KΩ, film
RP301	HE 9-124	4.7 KΩ × 5
RP302	HE 9-131	390 Ω × 5
Transistors		
Q301	HE 417-118	Transistor, silicon, NPN
Q302	HE 417-118	Transistor, silicon, NPN
Miscellaneous		
	HE 204-2719	Bracket
	HE 250-1411	Screw, Phillips, pan head
	HE 255-0757	Spacer, hex, threaded

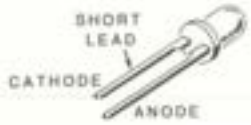
Chapter 7

Semiconductor Identification

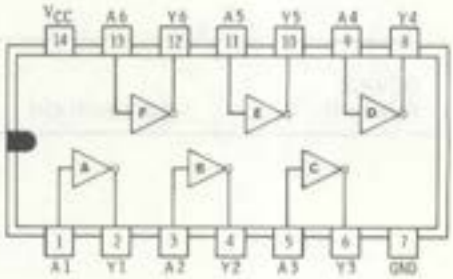
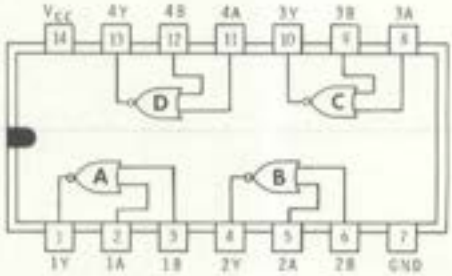
Introduction

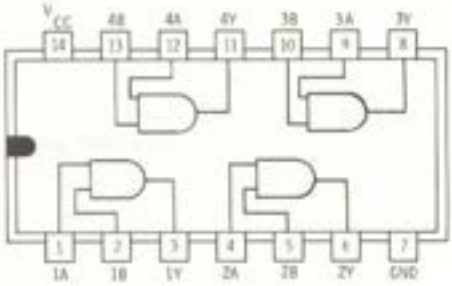
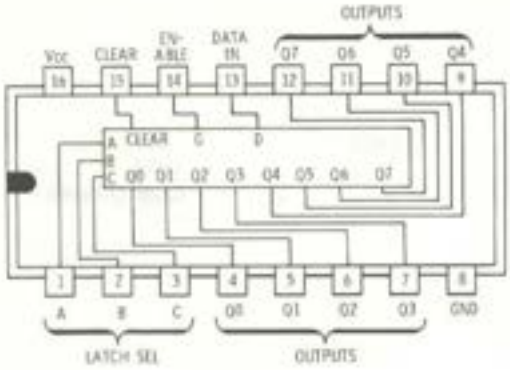
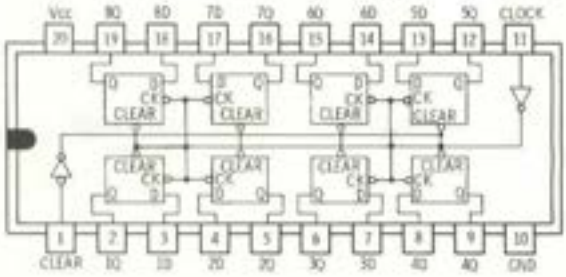
This chapter will help to identify the various semiconductor devices installed on the Z-309 Video Card by cross-referencing, where applicable, the Zenith/Heath part numbers with generic/alternate device numbers. The components are listed in ascending numerical order, along with device number (where applicable), and device lead configuration. This chapter also includes the programmable array logic (PAL) equations for the decoder devices on this card.

Part Number Index

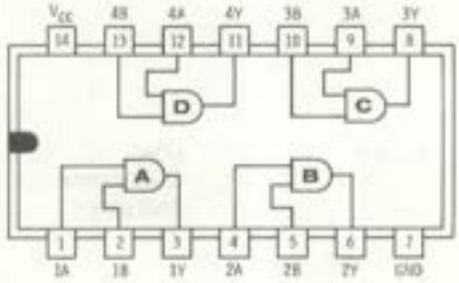
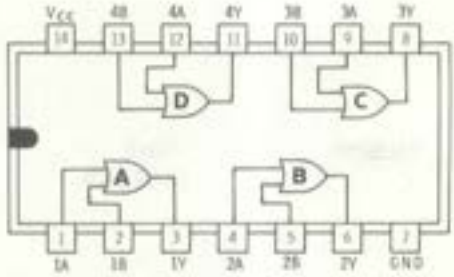
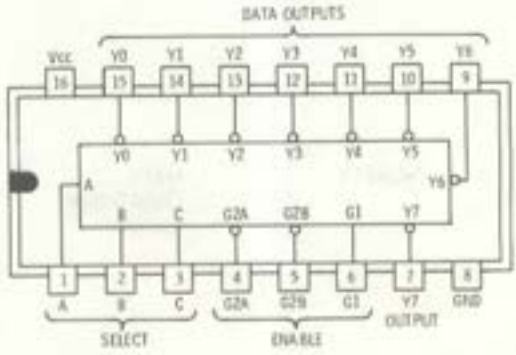
HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
412-654	HLMP-1002	CR301 Red test LED	

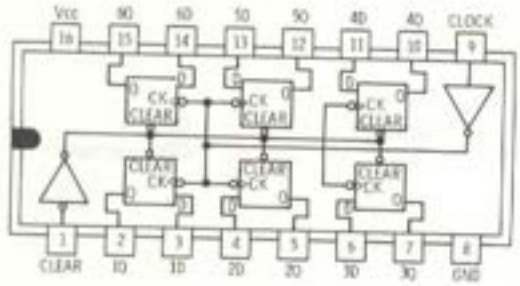
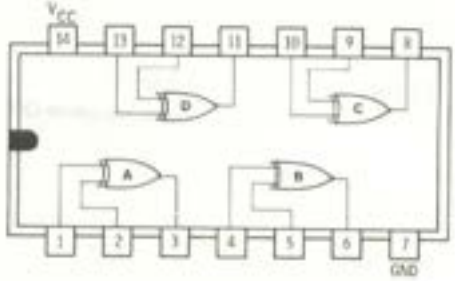
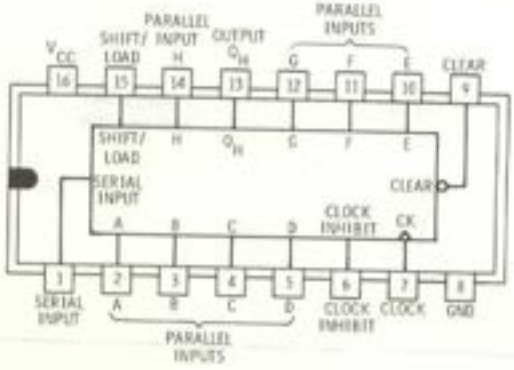
Semiconductor Identification

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
417-118	2N3393	Q301, Q302 Video output	
443-755	74LS04	U302, U304 Hex inverter	
443-779	74LS02	U346 Quad 2-input NOR gate	

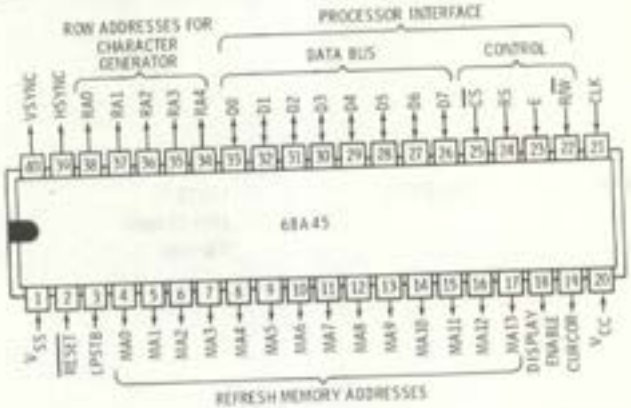
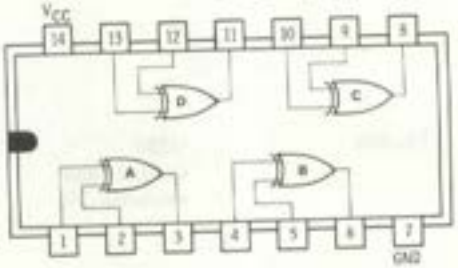
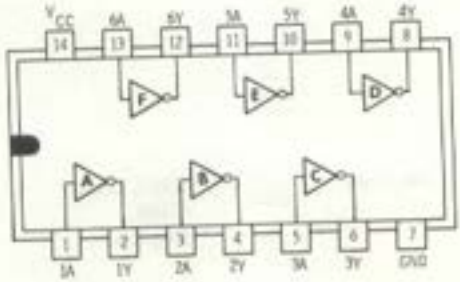
HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
443-780	74LS08	U347 Quad 2-input AND gate	
443-804	74LS259	U318 8-bit latch	
443-805	74LS273	U319 Octal D-type flip-flop	

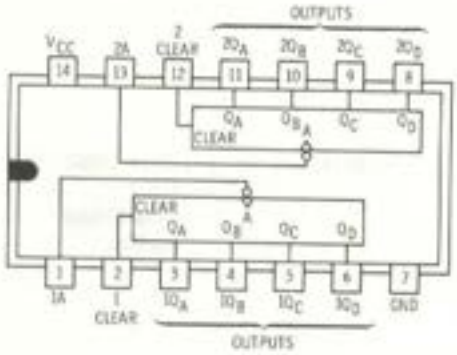
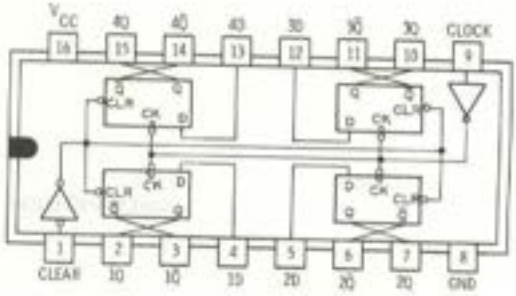
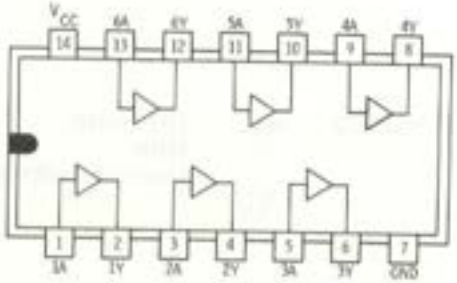
Semiconductor Identification

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
443-816	74LS09	U301 Quad AND gate	
443-875	74LS32	U303, U313, U345 Quad OR gate	
443-877	74LS138	U317, U329 Decoder	

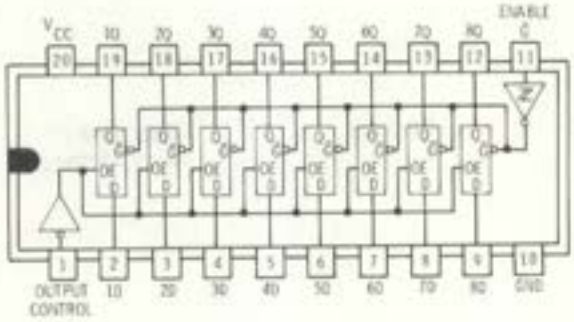
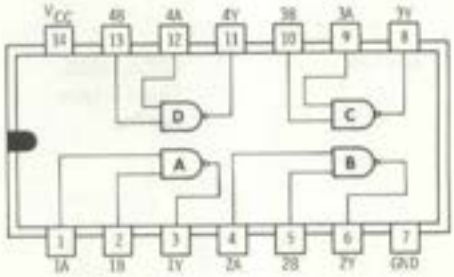
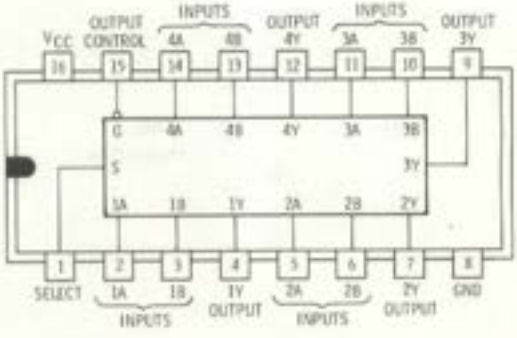
HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
443-879	74LS174	U333 Hex D-type flip-flop	
443-891	74LS86	U339 Quad 2-input exclusive OR	
443-892	74LS166	U305, U328, U348 Register	

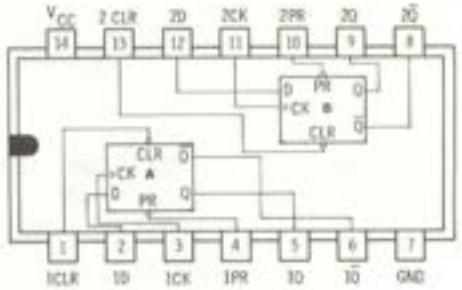
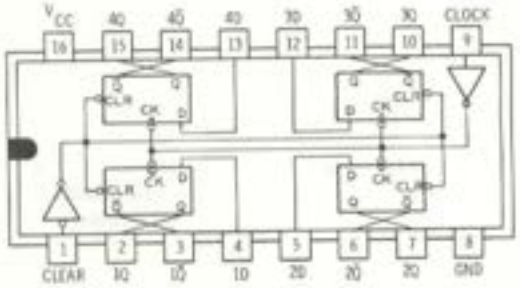
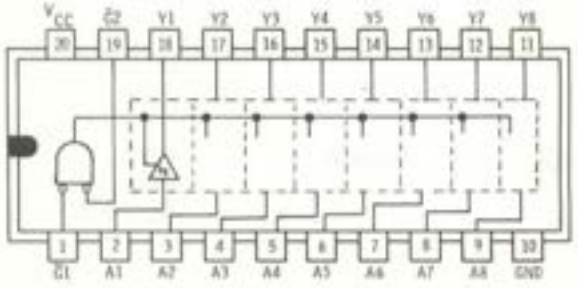
Semiconductor Identification

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
443-906	MC6845	U337 CRT controller	
443-915	74S86	U307 Quad exclusive OR	
443-967	7406	U320, U341 Hex inverter	

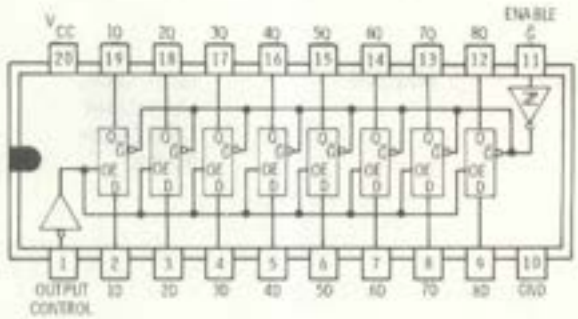
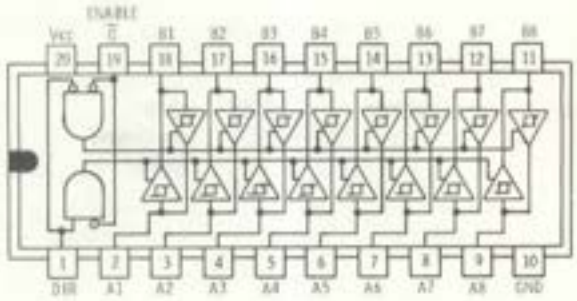
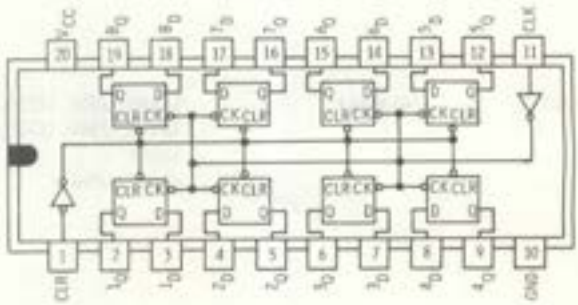
HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
443-973	74LS393	U322, U343 Binary counter	
443-983	74S175	U334, U335 Quad D-type flip-flop	
443-1020	7407	U363 Hex buffer	

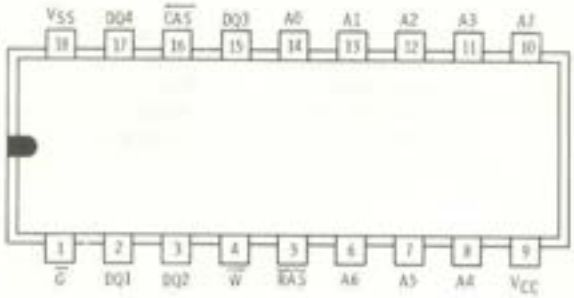
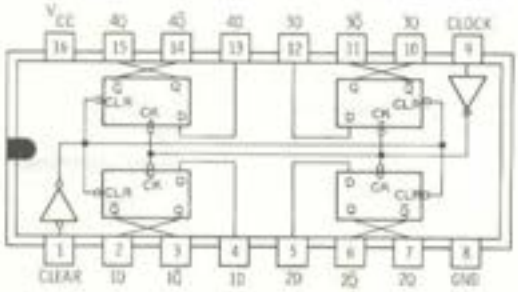
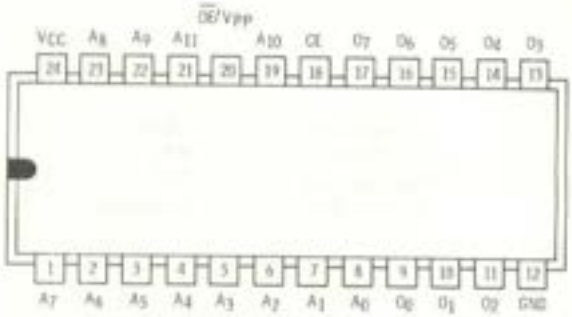
Semiconductor Identification

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
443-1031	74ALS574	U311, U352, U327 Octal D-type flip-flop	
443-1034	74LS38	U323 Quad NAND buffer	
443-1037	74LS257A	U310, U315, U316 Quad 2-to-1 selector	

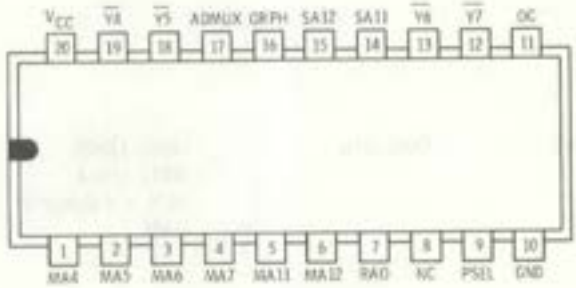
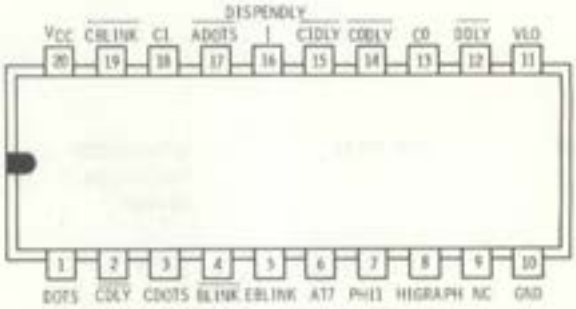
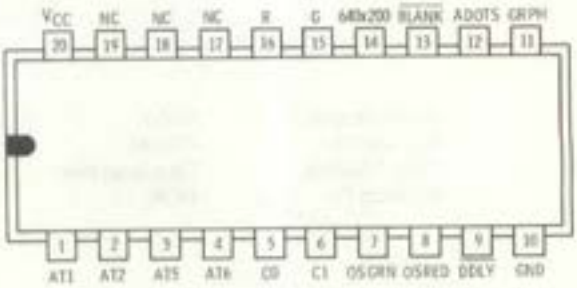
HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
443-1051	74ALS74	U321, U330, U331, U344 Octal D-type flip-flop	
443-1053	74S174	U338 Hex D-type flip-flop	
443-1058	74LS541	U340, U351, U353, U354, U359, U360, U361 Octal buffer	

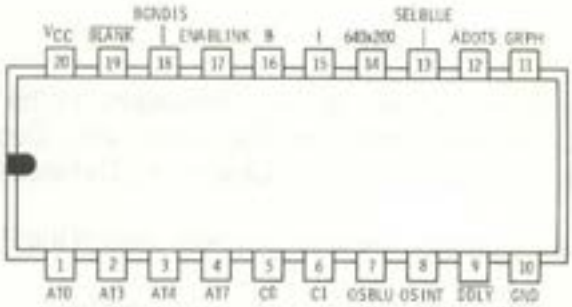
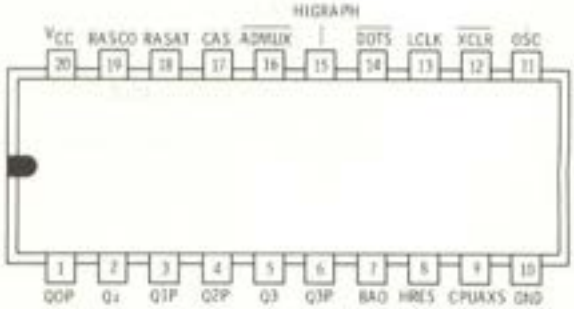
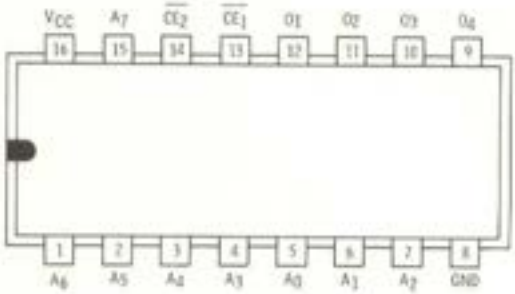
Semiconductor Identification

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
443-1070	74ALS573	U355, U356 Octal D-type latch	
443-1097	74ALS245	U358 Octal tri-state transceiver	
443-1096	74ALS273	U357 Octal tri-state flip-flop	

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
443-1165	TMS4416	U308, U309, U312, U314 16 K × 4 dynamic RAM	
443-1166	74ALS174	U349, U350 Hex D-type flip-flop	
444-230 or 444-230-1	Available only from Zenith Data Systems or Heath Co.	U306 PROM Character font ROM	

Semiconductor Identification

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
444-231	Available only from Zenith Data Systems or Heath Co.	U336 PAL Scroll multiplexer	
444-232	Available only from Zenith Data Systems or Heath Co.	U326 PAL Video synchronizer	
444-233	Available only from Zenith Data Systems or Heath Co.	U324 PAL R/G dots generator	

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
444-234	Available only from Zenith Data Systems or Heath Co.	U325 PAL B/I dots generator	
444-235	Available only from Zenith Data Systems or Heath Co.	U332 PAL RAM control	
444-287	Available only from Zenith Data Systems or Heath Co.	U362 PROM Video address decoder	

PAL Equations

This section contains the logic equations for the programmable array logic (PAL) devices located on the video card. Detailed circuit operation for these devices is covered in Chapter 4, "Detailed Circuit Description."

Table 7.1 defines the logic symbols used in the PAL equations.

Table 7.1. PAL Equation Logic Symbols

PAL SYMBOL	LOGIC FUNCTION
/	Complement
*	AND
=	EQUAL
:=	Replaced by
+	OR
( )	Three state output

U336, the scroll multiplexer, functions according to the following logic:

IF (/OC) Y4 = ADMUX */MA4 +/ADMUX */PSEL */MA11 +/ADMUX *PSEL */SA11

IF (/OC) Y5 = ADMUX */MA5 +/ADMUX */PSEL */GRPH */MA12 + /ADMUX */PSEL *GRPH */RA0 +/ADMUX *PSEL */SA12

IF (/OC) Y6 = ADMUX */MA6 +/ADMUX

IF (/OC) Y7 = ADMUX */MA7

U326, the video sync decoder, functions as follows:

A/N DOTS := /CDLY */CDOTS +/CBLINK */CDOTS +/CDLY *BLINK *EBLINK *ATBLINK

/DISPENDLY := DDLY

C1DLY := /C1 */640×200 +/C1 * Φ1 *640×200 +/C0 */ Φ1 *640×200

C0DLY := /C0 */640×200

U324, the red/green dot selector, functions as follows:

R = AT2 *DISPEN DLY */GRPH *A/N DOTS */BLANK
+AT6 *DISPEN DLY */GRPH */A/N DOTS */BLANK
+C1 *DISPEN DLY *GRPH */640×200 */BLANK
+OVERSCAN R */DISPEN DLY */BLANK */GRPH
+OVERSCAN R *DISPEN DLY *GRPH */C0 DLY */C1 DLY */640×200 */BLANK
+OVERSCAN R *DISPEN DLY *GRPH *640×200 *C1 DLY */BLANK

G = AT1 *DISPEN DLY */GRPH *A/N DOTS */BLANK
+AT5 *DISPEN DLY */GRPH */A/N DOTS */BLANK
+C0 DLY *DISPEN DLY *GRPH */640×200 */BLANK
+OVERSCAN G */DISPEN DLY */BLANK */GRPH
+OVERSCAN G *DISPEN DLY *GRPH */C0 DLY */C1 DLY */640×200 */BLANK
+OVERSCAN G *DISPEN DLY *GRPH *640×200 *C1 DLY */BLANK

Semiconductor Identification

U325, the blue/intensity dot selector, functions as follows:

B = AT0 *DISPEN DLY */GRPH *A/N DOTS */BLANK
+AT4 *DISPEN DLY */GRPH */A/N DOTS */BLANK
+SELBLUE *DISPEN DLY *GRPH */640×200 *C1 DLY */BLANK
+SELBLUE *DISPEN DLY *GRPH */640×200 *C0 DLY*/BLANK
+OVERSCAN B */DISPEN DLY */BLANK */GRPH
+OVERSCAN B *DISPEN DLY *GRPH */C0 DLY */C1 DLY */640×200 */BLANK
+OVERSCAN B *DISPEN DLY *GRPH *640×200 *C1 DLY */BLANK

I = AT3 *DISPEN DLY */GRPH *A/N DOTS */BLANK
+AT7 */ENABLE BLINK *DISPEN DLY */GRPH */A/N DOTS */BLANK
+BGNDI *DISPEN DLY *GRPH */640×200 *C0 DLY */BLANK
+BGNDI *DISPEN DLY *GRPH */640×200 *C1 DLY */BLANK
+OVERSCAN I */DISPEN DLY */BLANK */GRPH
+OVERSCAN I *DISPEN DLY *GRPH */C0 DLY */C1 DLY */640×200 */BLANK
+OVERSCAN I *DISPEN DLY *GRPH *640×200 *C1 DLY */BLANK

U332, the RAM controller, functions as follows:

IF (Vcc) /RASCC = Q0P */Q3 *CPUAXS */BA0 +/Q0P *Q3

IF (Vcc) /RASAT = Q0P */Q3 *CPUAXS *BA0 +/Q0P *Q3

IF (Vcc) /CAS = Q1P */Q3P +/Q1P *Q3P

IF (Vcc) /ADMUX = Q1 */Q3 +/Q1 *Q3

IF (Vcc) /DOTS = HRES */OSC */640×200 +/HRES */7.15 MHZ */640×200 +640×200 */OSC

IF (Vcc) /XCLK = HRES */OSC +/HRES */7.15 MHZ

Chapter 8

Data Sheets

General

This chapter provides reprints of the 6845 CRT controller (CRTC) data sheets. The following pages are reprinted with the permission of Hitachi.

HD6845S, HD68A45S, HD68B45S

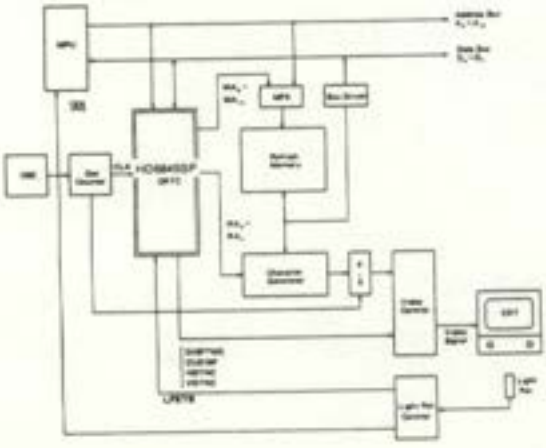
CRTC (CRT Controller)

The CRTC is a LSI controller which is designed to provide an interface for microcomputers to raster scan type CRT displays. The CRTC belongs to the HMCS6800 LSI Family and has full compatibility with MPU in both data lines and control lines. Its primary function is to generate timing signal which is necessary for raster scan type CRT display according to the specification programmed by MPU. The CRTC is also designed as a programmable controller, so applicable to wide-range CRT display from small low-functioning character display up to raster type full graphic display as well as large high-functioning limited graphic display.

■ FEATURES

- Number of Displayed Characters on the Screen, Vertical Dot Format of One Character, Horizontal and Vertical Sync Signal, Display Timing Signal are Programmable
- 3.7 MHz High Speed Display Operation
- Line Buffer-less Refreshing
- 14-bit Refresh Memory Address Output (16k Words max. Access)
- Programmable Interlace/Non-interlace Scan Mode
- Built-in Cursor Control Function
- Programmable Cursor Height and its Blink
- Built-in Light Pen Detection Function
- Paging and Scrolling Capability
- TTL Compatible
- Single +5V Power Supply
- Upward compatible with MC6845

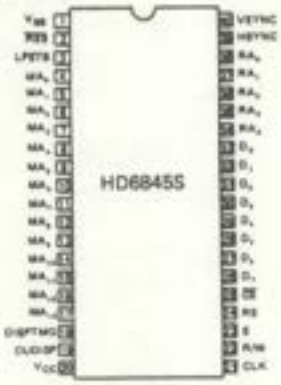
■ SYSTEM BLOCK DIAGRAM



HD6845SP, HD68A45SP, HD68B45SP

(DP-40)

■ PIN ARRANGEMENT



(Top View)

■ ORDERING INFORMATION

CRTC	Bus Timing	CRT Display Timing
HD6845SP	1.0 MHz	3.7 MHz max.
HD68A45SP	1.5 MHz	
HD68B45SP	2.0 MHz	

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage	V_{CC} *	−0.3 ~ +7.0	V
Input Voltage	V_{in} *	−0.3 ~ +7.0	V
Operating Temperature	T_{opr}	− 20 ~ + 75	°C
Storage Temperature	T_{stg}	− 55 ~ +150	°C

* With respect to V_{SS} (SYSTEM GND)

[NOTE] Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability of LSI.

■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC} *	4.75	5	5.25	V
Input Voltage	V_{IL} *	−0.3	–	0.8	V
	V_{IH} *	2.0	–	V_{CC}	V
Operating Temperature	T_{opr}	− 20	25	75	°C

* With respect to V_{SS} (SYSTEM GND)

■ ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS (V_{CC} = 5V ± 5%, V_{SS} = 0V, Ta = −20~+75°C, unless otherwise noted.)

Item	Symbol	Test Condition		min	typ	max	Unit
Input "High" Voltage	V_{IH}			2.0	–	V_{CC}	V
Input "Low" Voltage	V_{IL}			−0.3	–	0.8	V
Input Leakage Current	I_{in}	V_{in} = 0 ~ 5.25V (Except D_0~D_7)		−2.5	–	2.5	μA
Three-State Input Current (off-state)	I_{TSI}	V_{in} = 0.4 ~ 2.4V V_{CC} = 5.25V (D_0~ D_7)		− 10	–	10	μA
Output "High" Voltage	V_{OH}	I_{LOAD} = −205 μA (D_0~ D_7)		2.4	–	–	V
		I_{LOAD} = −100 μA (Other Outputs)					
Output "Low" Voltage	V_{OL}	I_{LOAD} = 1.6 mA		–	–	0.4	V
Input Capacitance	C_{in}	V_{in} = 0 Ta = 25°C f = 1.0 MHz	D_0 ~ D_7	–	–	12.5	pF
			Other Inputs	–	–	10.0	pF
Output Capacitance	C_{out}	V_{in} = 0V, Ta = 25°C, f = 1.0 MHz		–	–	10.0	pF
Power Dissipation	P_D			–	600	1000	mW

• AC CHARACTERISTICS (V_{CC} = 5V ±5%, V_{SS} = 0V, Ta = -20~+75°C, unless otherwise noted.)

1. TIMING OF CRTC SIGNAL

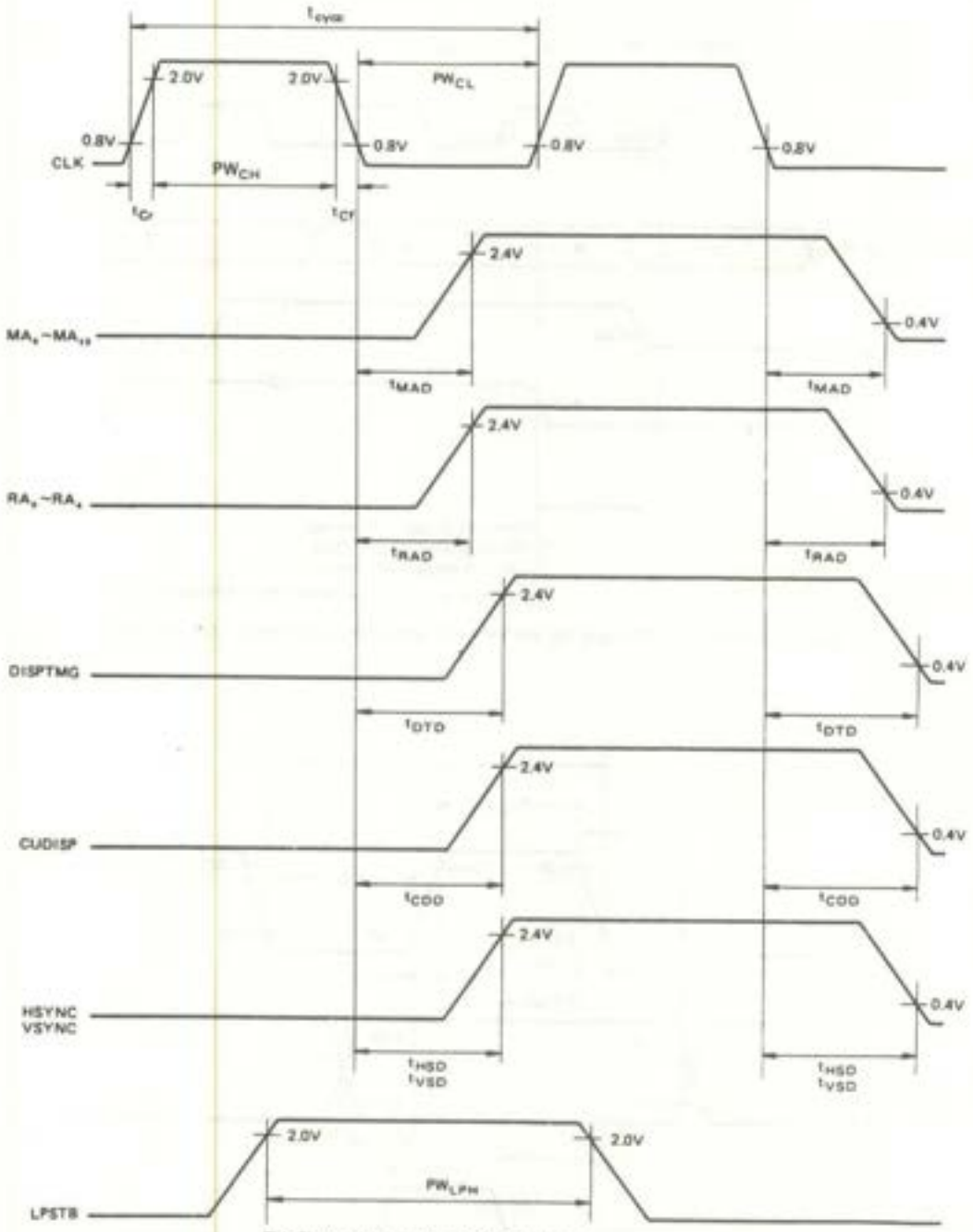
Item	Symbol	Test Condition	min	typ	max	Unit
Clock Cycle Time	t_{CYC}	Fig. 1	270	–	–	ns
Clock "High" Pulse Width	PW_{CH}		130	–	–	ns
Clock "Low" Pulse Width	PW_{CL}		130	–	–	ns
Rise and Fall Time for Clock Input	t_{Cr}, t_{Cf}		–	–	20	ns
Memory Address Delay Time	t_{MAD}		–	–	160	ns
Raster Address Delay Time	t_{RAD}		–	–	160	ns
DISPTMG Delay Time	t_{DTD}		–	–	250	ns
CUDISP Delay Time	t_{CDD}		–	–	250	ns
Horizontal Sync Delay Time	t_{HSD}		–	–	200	ns
Vertical Sync Delay Time	t_{VSD}		–	–	250	ns
Light Pen Strobe Pulse Width	PW_{LPH}		60	–	–	ns
Light Pen Strobe	t_{LPD1}	Fig. 2	–	–	70	ns
Uncertain Time of Acceptance	t_{LPD2}		–	–	0	ns

2. MPU READ TIMING

Item	Symbol	Test Condition	HD6845SP			HD68A45SP			HD68B45SP			Unit
			min	typ	max	min	typ	max	min	typ	max	
Enable Cycle Time	t_{CYCE}	Fig. 3	1.0	–	–	0.666	–	–	0.5	–	–	µs
Enable "High" Pulse Width	PW_{EH}		0.45	–	–	0.280	–	–	0.22	–	–	µs
Enable "Low" Pulse Width	PW_{EL}		0.40	–	–	0.280	–	–	0.21	–	–	µs
Enable Rise and Fall Time	t_{Er}, t_{Ef}		–	–	25	–	–	25	–	–	25	ns
Address Set Up Time	t_{AS}		140	–	–	140	–	–	70	–	–	ns
Data Delay Time	t_{DDR}		–	–	320	–	–	220	–	–	180	ns
Data Hold Time	t_H		10	–	–	10	–	–	10	–	–	ns
Address Hold Time	t_{AH}		10	–	–	10	–	–	10	–	–	ns
Data Access Time	t_{ACC}		–	–	460	–	–	360	–	–	250	ns

3. MPU WRITE TIMING

Item	Symbol	Test Condition	HD6845SP			HD68A45SP			HD68B45SP			Unit
			min	typ	max	min	typ	max	min	typ	max	
Enable Cycle Time	t_{CYCE}	Fig. 4	1.0	–	–	0.666	–	–	0.5	–	–	µs
Enable "High" Pulse Width	PW_{EH}		0.45	–	–	0.280	–	–	0.22	–	–	µs
Enable "Low" Pulse Width	PW_{EL}		0.40	–	–	0.280	–	–	0.21	–	–	µs
Enable Rise and Fall Time	t_{Er}, t_{Ef}		–	–	25	–	–	25	–	–	25	ns
Address Set Up Time	t_{AS}		140	–	–	140	–	–	70	–	–	ns
Data Set Up Time	t_{DSW}		195	–	–	80	–	–	60	–	–	ns
Data Hold Time	t_H		10	–	–	10	–	–	10	–	–	ns
Address Hold Time	t_{AH}		10	–	–	10	–	–	10	–	–	ns



This Figure shows the relation in time between CLK signal and each output signals. Output sequence is shown in Figs. 9 ~ 15.

Figure 1 Time Chart of the CRTC

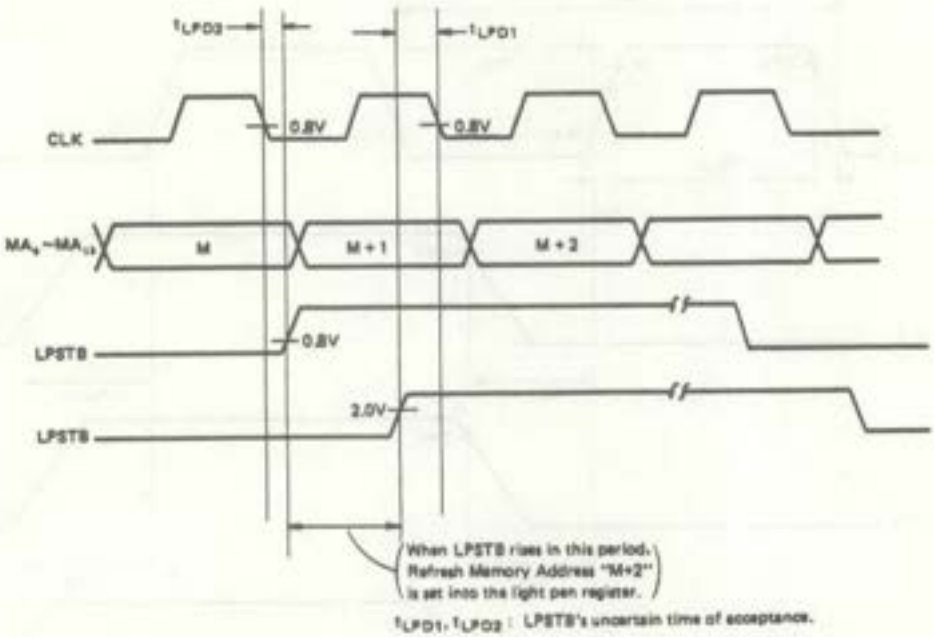


Figure 2 LPSTB Input Timing & Refresh Memory Address that is set into the light pen register.

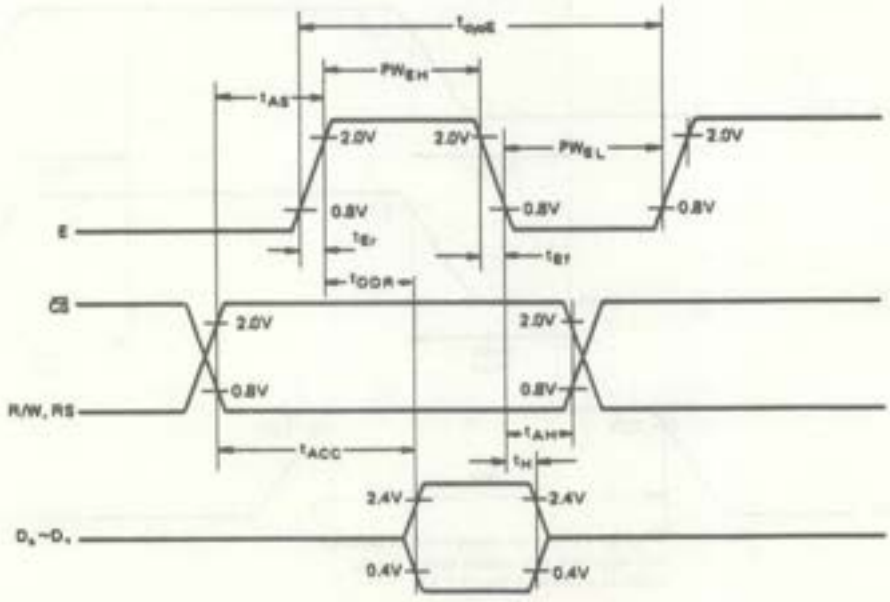


Figure 3 Read Sequence

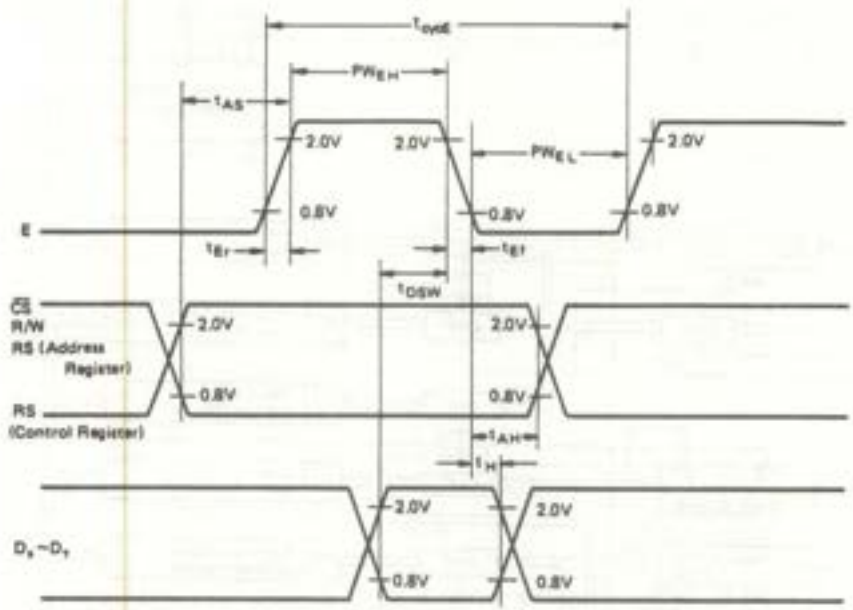


Figure 4 Write Sequence

■ SYSTEM DESCRIPTION

The CRTC is a LSI which is connected with MPU and CRT display device to control CRT display. The CRTC consists of internal register group, horizontal and vertical timing circuits, linear address generator, cursor control circuit, and light pen detection circuit. Horizontal and vertical timing circuit generate RA_0~RA_4, DISPTMG, HSYNC, and VSYNC. RA_0~RA_4 are raster address signals and used as input signals for Character Generator. DISPTMG, HSYNC, and VSYNC signals are received by video control circuit. This horizontal and vertical timing circuit consists of internal counter and comparator circuit. Linear address generator generates refresh memory address MA_0 ~MA_{13} to be used for refreshing the screen. By these address signals, refresh memory is accessed periodically. As 14 refresh memory address signals are prepared, 16k words max are accessible. Moreover, the use of start address register enables paging and scrolling. Light pen detection circuit detects light pen position on the screen. When light pen strobe signal is received, light pen register memorizes linear address generated by linear address generator in order to memorize where light pen is on the screen. Cursor control circuit controls the position of cursor, its height, and its blink.

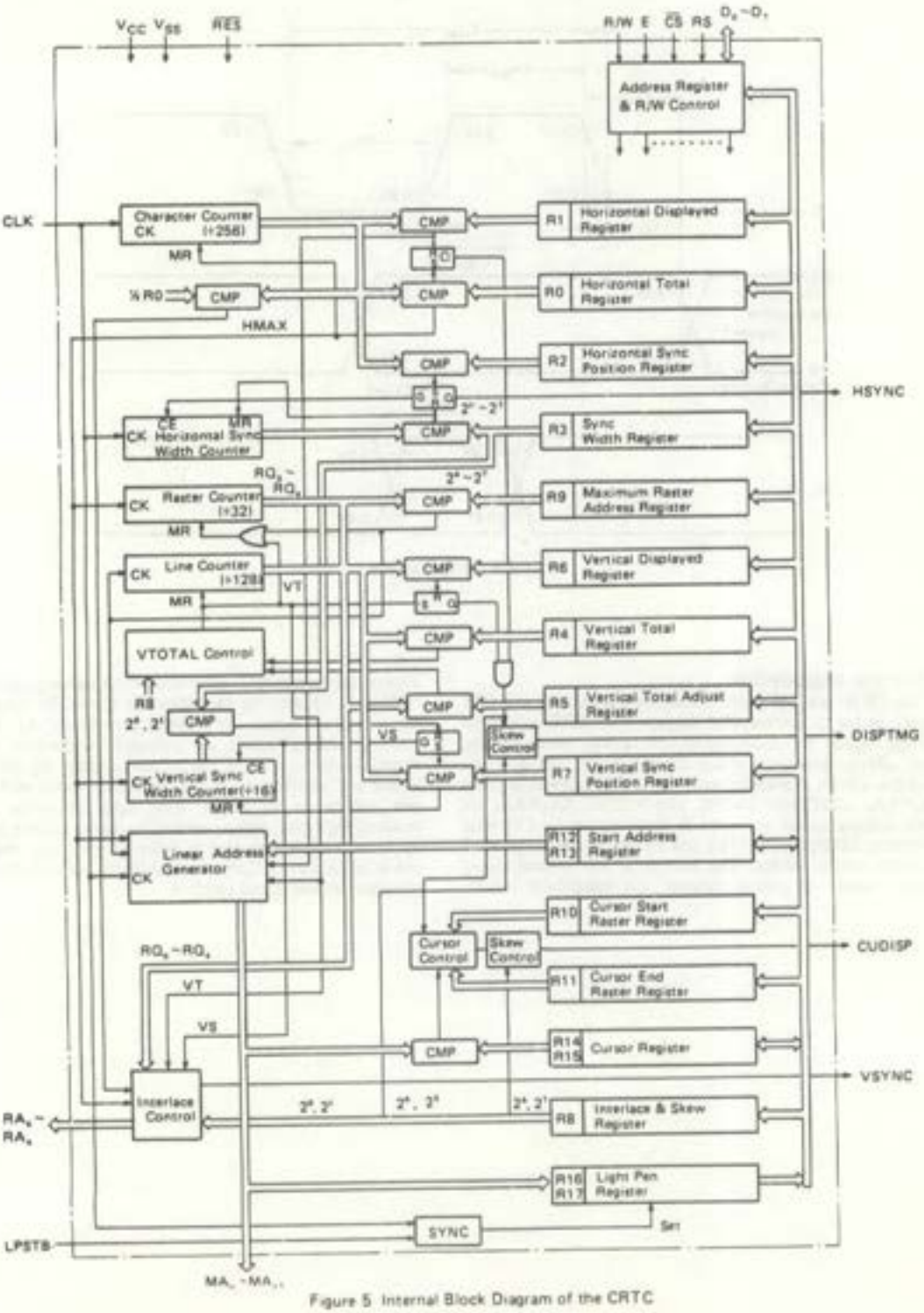


Figure 5 Internal Block Diagram of the CRTC

• FUNCTION OF SIGNAL LINE

The CRTC provides 13 interface signals to MPU and 25 interface signals to CRT display.

• Interface Signals to MPU

Bi-directional Data Bus (D_0~D_7)

Bi-directional data bus(D_0~D_7) are used for data transfer between the CRTC and MPU. The data bus outputs are 3-state buffers and remain in the high-impedance state except when MPU performs a CRTC read operation.

Read/Write (R/W)

R/W signal controls the direction of data transfer between the CRTC and MPU. When R/W is at "High" level, data of CRTC is transfered to MPU. When R/W is at "Low" level, data of MPU is transfered to CRTC.

Chip Select ($\overline{CS}$)

Chip Select signal ($\overline{CS}$) is used to address the CRTC. When $\overline{CS}$ is at "Low" level, it enables R/W operation to CRTC internal registers. Normally this signal is derived from decoded address signal of MPU under the condition that VMA signal of MPU is at "High" level.

Register Select (RS)

Register Select signal (RS) is used to select the address register and 18 control registers of the CRTC. When RS is at "Low" level, the address register is selected and when RS is at "High" level, control registers are selected. This signal is normally a derivative of the lowest bit (A0) of MPU address bus.

Enable(E)

Enable signal (E) is used as strobe signal in MPU R/W operation with the CRTC internal registers. This signal is normally a derivative of the HMCS6800 System ϕ_2 clock.

Reset ($\overline{RES}$)

Reset signal ($\overline{RES}$) is an input signal used to reset the CRTC. When $\overline{RES}$ is at "Low" level, it forces the CRTC into the following status.

1) All the counters in the CRTC are cleared and the device stops the display operation.
2) All the outputs go down to "Low" level.
3) Control registers in the CRTC are not affected and remain unchanged.

This signal is different from other HMCS6800 family LSIs in the following functions and has restrictions for usage.

1) $\overline{RES}$ signal has capability of reset function only when LPSTB is at "Low" level.
2) The CRTC starts the display operation immediately after $\overline{RES}$ signal goes "High".

• Interface Signals to CRT Display Device

Character Clock (CLK)

CLK is a standard clock input signal which defines character timing for the CRTC display operation. This signal is normally derived from the external high-speed dot timing logic.

Horizontal Sync (HSYNC)

HSYNC is an active "High" level signal which provides horizontal synchronization for display device.

Vertical Sync (VSYNC)

VSYNC is an active "High" level signal which provides vertical synchronization for display device.

Display Timing (DISPTMG)

DISPTMG is an active "High" level signal which defines the display period in horizontal and vertical raster scanning. It is necessary to enable video signal only when DISPTMG is at "High" level.

Refresh Memory Address (MA_0~MA_{13})

MA_0~MA_{13} are refresh memory address signals which are used to access to refresh memory in order to refresh the CRT screen periodically. These outputs enables 16k words max. refresh memory access. So, for instance, these are applicable up to 2000 characters/screen and 8-page system.

Raster Address (RA_0~RA_4)

RA_0~RA_4 are raster address signals which are used to select the raster of the character generator or graphic pattern generator etc.

Cursor Display (CUDISP)

CUDISP is an active "High" level video signal which is used to display the cursor on the CRT screen. This output is inhibited while DISPTMG is at "Low" level. Normally this output is mixed with video signal and provided to the CRT display device.

Light Pen Strobe (LPSTB)

LPSTB is an active "High" level input signal which accepts strobe pulse detected by the light pen and control circuit. When this signal is activated, the refresh memory address (MA_0~MA_{13}) which are shown in Fig. 2 are stored in the 14-bit light pen register. The stored refresh memory address need to be corrected in software, taking the delay time of the display device, light pen, and light pen control circuits into account.

■ REGISTER DESCRIPTION

Table 1 Internal Registers Assignment

$\overline{CS}$	RS	Address Register 4 3 2 1 0	Register #	Register Name	Program Unit	READ	WRITE	Data Bit 7	6	5	4	3	2	1	0
1	×	× × × × ×			–	–	–								
0	0	× × × × ×	AR	Address Register	–	×	O								
0	1	0 0 0 0 0	R0	Horizontal Total *	Character	×	O								
0	1	0 0 0 0 1	R1	Horizontal Displayed	Character	×	O								
0	1	0 0 0 1 0	R2	Horizontal Sync* Position	Character	×	O								
0	1	0 0 0 1 1	R3	Sync Width	Vertical-Raster, Horizontal-Character	×	O	wv3	wv2	wv1	wv0	wh3	wh2	wh1	wh0
0	1	0 0 1 0 0	R4	Vertical Total *	Line	×	O								
0	1	0 0 1 0 1	R5	Vertical Total Adjust	Raster	×	O								
0	1	0 0 1 1 0	R6	Vertical Displayed	Line	×	O								
0	1	0 0 1 1 1	R7	Vertical Sync * Position	Line	×	O								
0	1	0 1 0 0 0	R8	Interlace & Skew	–	×	O	C1	C0	D1	D0			V	S
0	1	0 1 0 0 1	R9	Maximum Raster Address	Raster	×	O								
0	1	0 1 0 1 0	R10	Cursor Start Raster	Raster	×	O		B	P					
0	1	0 1 0 1 1	R11	Cursor End Raster	Raster	×	O								
0	1	0 1 1 0 0	R12	Start Address(H)	–	O	O								
0	1	0 1 1 0 1	R13	Start Address(L)	–	O	O								
0	1	0 1 1 1 0	R14	Cursor(H)	–	O	O								
0	1	0 1 1 1 1	R15	Cursor (L)	–	O	O								
0	1	1 0 0 0 0	R16	Light Pen(H)	–	O	×								
0	1	1 0 0 0 1	R17	Light Pen(L)	–	O	×								

[NOTE] 1. The Registers marked *: (Written Value) = (Specified Value) – 1
2. Written Value of R9 is mentioned below.
1) Non-interlace Mode / Interlace Sync Mode: (Written Value Nr) = (Specified Value) – 1
2) Interlace Sync & Video Mode: (Written Value Nr) = (Specified Value) – 2
3. C0 and C1 specify skew of CUDISP output signal.
D0 and D1 specify skew of DISPTMG output signal.
When S is "1", V specifies video mode. S specifies the Interlace Sync Mode.
4. B specifies the cursor blink. P specifies the cursor blink period.
5. wv0~wv3 specify the pulse width of Vertical Sync Signal.
wh0~wh3 specify the pulse width of Horizontal Sync Signal.
6. R0 is ordinally programmed to be odd number in interlace mode.
7. O; Yes, ×; No

- **Address Register (AR)**

This is a 5-bit register used to select 18 internal control registers (R0~R17). Its contents are the address of one of 18 internal control registers. Programming the data from 18 to 31 produces no results. Access to R0~R17 requires, first of all, to write the address of corresponding control register into this register. When RS and $\overline{CS}$ are at "Low" level, this register is selected.

- **Horizontal Total Register (R0)**

This is a register used to program total number of horizontal characters per line including the retrace period. The data is 8-bit and its value should be programmed according to the specification of the CRT. When M is total number of characters, (M-1) shall be programmed to this register. When programming for interlace mode, M must be even.

- **Horizontal Displayed Register (R1)**

This is a register used to program the number of horizontal displayed characters per line. Data is 8-bit and any number that is smaller than that of horizontal total characters can be programmed.

- **Horizontal Sync Position Register (R2)**

This is a register used to program horizontal sync position as multiples of the character clock period. Data is 8-bit and any number that is lower than the horizontal total number can be programmed. When H is character number of horizontal Sync Position, (H-1) shall be programmed to this register. When programmed value of this register is increased, the display position on the CRT screen is shifted to the left. When programmed value is decreased, the position is shifted to the right. Therefore, the optimum horizontal position can be determined by this value.

- **Sync Width Register (R3)**

This is a register used to program the horizontal sync pulse width and the vertical sync pulse width. The horizontal sync pulse width is programmed in the lower 4-bit as multiples of the character clock period. "0" cannot be programmed. The vertical sync pulse width is programmed in higher 4-bit as multiples of the raster period. When "0" is programmed in higher 4-bit, 16 raster period (16H) is specified.

- **Vertical Total Register (R4)**

This is a register used to program total number of lines per frame including vertical retrace period. The data is within 7-bit and its value should be programmed according to the specification of the CRTC. When N is total number of lines, (N-1) shall be programmed to this register.

- **Vertical Total Adjust Register (R5)**

This is a register used to program the optimum number to adjust total number of rasters per field. This register enables to decide the number of vertical deflection frequency more strictly.

- **Vertical Displayed Register (R6)**

This is a register used to program the number of displayed character rows on the CRT screen. Data is 7-bit and any number that is smaller than that of vertical total characters can be programmed.

Table 2 Pulse Width of Vertical Sync Signal

VSW				Pulse Width
2^3	2^2	2^1	2^0	
0	0	0	0	16H
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

H: Raster period

Table 3 Pulse Width of Horizontal Sync Signal

HSW				Pulse Width
2^3	2^2	2^1	2^0	
0	0	0	0	– (Note)
0	0	0	1	1 CH
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

CH: Character clock period
(Note) HSW = "0" cannot be used.

• **Vertical Sync Position Register (R7)**

This is a register used to program the vertical sync position on the screen as multiples of the horizontal character line period. Data is 7-bit and any number that is equal to or less than vertical total characters can be programmed. When V is character number of vertical sync position, (V-1) shall be programmed to this register. When programmed value of this register is increased, the display position is shifted up. When programmed value is decreased, the position is shifted down. Therefore, the optimum vertical position may be determined by this value.

• **Interlace and Skew Register (R8)**

This is a register used to program raster scan mode and skew (delay) of CUDISP signal and DISPTMG signal.

Interlace Mode Program Bit (V, S)

Raster scan mode is programmed in the V, S bit.

Table 4 Interlace Mode (2^1, 2^0)

V	S	Raster Scan Mode
0	0	Non-interlace Mode
1	0	
0	1	Interlace Sync Mode
1	1	Interlace Sync & Video Mode

In the non-interlace mode, the rasters of even number field and odd number field are scanned duplicatedly. In the interlace sync mode, the rasters of odd number field are scanned in the middle of even number field. Then it is controlled to display the same character pattern in two fields. In the interlace sync and video mode, the raster scan method is the same as the interlace sync mode, but it is controlled to display different character pattern in two field.

Skew Program Bit (C1, C0, D1, D0)

These are used to program the skew (delay) of CUDISP signal and DISPTMG signal.

Skew of these two kinds of signals are programmed separately.

Table 5 DISPTMG Skew Bit (2^7, 2^6)

D1	D0	DISPTMG Signal
0	0	Non-skew
0	1	One-character skew
1	0	Two-character skew
1	1	Non-output

Table 6 Cursor Skew Bit (2^5, 2^4)

C1	C0	Non-skew
0	0	Non-skew
0	1	One-character skew
1	0	Two-character skew
1	1	Non-output

Skew function is used to delay the output timing of CUDISP and DISPTMG signals in LSI for the time to access refresh memory, character generator or pattern generator, and to make the same phase with serial video signal.

• **Maximum Raster Address Register (R9)**

This is a register used to program maximum raster address within 5-bit. This register defines total number of rasters per character including space. This register is programmed as follows.

Non-interlace Mode, Interlace Sync Mode

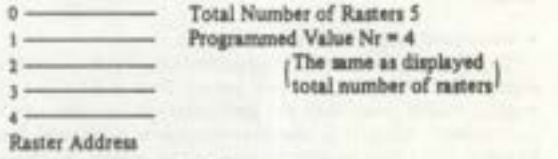
When total number of rasters is RN, (RN-1) shall be programmed.

Interlace Sync & Video Mode

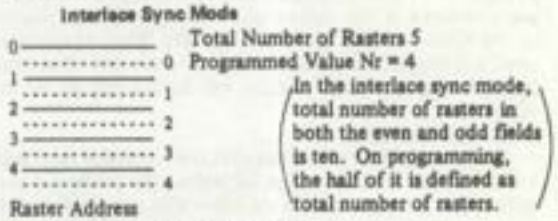
When total number of rasters is RN, (RN-2) shall be programmed.

This manual defines total number of rasters in non-interlace mode, interlace sync mode and interlace sync & video mode as follows:

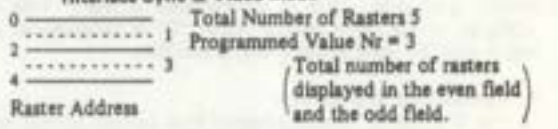
Non-interlace Mode



Interlace Sync Mode



Interlace Sync & Video Mode

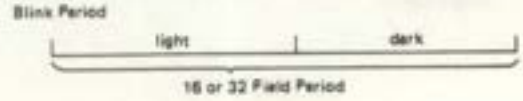


• **Cursor Start Raster Register (R10)**

This is a register used to program the cursor start raster address by lower 5-bit (2^0~2^4) and the cursor display mode by higher 2-bit (2^5, 2^6).

Table 7 Cursor Display Mode (2^6, 2^5)

B	P	Cursor Display Mode
0	0	Non-blink
0	1	Cursor Non-display
1	0	Blink, 16 Field Period
1	1	Blink, 32 Field Period



- **Cursor End Raster Register (R11)**
  This is register used to program the cursor end raster address.

- **Start Address Register (R12, R13)**
  These are used to program the first address of refresh memory to read out.
  Paging and scrolling is easily performed using this register. This register can be read but the higher 2-bit (2^6, 2^7) of R12 are always "0".

- **Cursor Register (R14, R15)**
  These two read/write registers stores the cursor location. The higher 2-bit (2^6, 2^7) of R14 are always "0".

- **Light Pen Register (R16, R17)**
  These read only registers are used to catch the detection address of the light pen. The higher 2-bit (2^6, 2^7) of R16 are always "0". Its value needs to be corrected by software because there is time delay from address output of the CRTC to signal input LPSTB pin of the CRTC in the process that raster is lit after address output and light pen detects it. Moreover, delay time shown in Fig. 2 needs to be taken into account.

Restriction on Programming Internal Register

1) $0 < Nhd < Nht + 1 \leqq 256$
2) $0 < Nvd < Nvt + 1 \leqq 128$
3) $0 \leqq Nhsp \leqq Nht$
4) $0 \leqq Nvsp \leqq Nvt$*
5) $0 \leqq N_{CSTART} \leqq N_{CEND} \leqq Nr$ (Non-interlace, Interlace sync mode)
   $0 \leqq N_{CSTART} \leqq N_{CEND} \leqq Nr + 1$ (Interlace sync & video mode)
6) $2 \leqq Nr \leqq 30$
7) $3 \leqq Nht$ (Except non-interlace mode)
   $5 \leqq Nht$ (Non-interlace mode only)

* In the interlace mode, pulse width is changed ±½ raster time when vertical sync signal extends over two fields.

Notes for Use

The method of directly using the value programmed in the internal register of LSI for controlling the CRT is adopted. Consequently, the display may flicker on the screen when the contents of the registers are changed from bus side asyncronously with the display operation.

Cursor Register

Writing into this register at frequent intervals for moving the cursor should be performed during horizontal and vertical retrace period.

Start Address Register

Writing into the start address register at frequent intervals for scrolling and paging should be performed during horizontal and vertical display period.

It is desirable to avoid programming other registers during display operation.

• OPERATION OF THE CRTC

- **Time Chart of CRT Interface Signals**
  The following example shows the display operation in which values of Table 8 are programmed to the CRTC internal registers. Fig. 6 shows the CRT screen format. Fig. 9 shows the time chart of signals output from the CRTC.

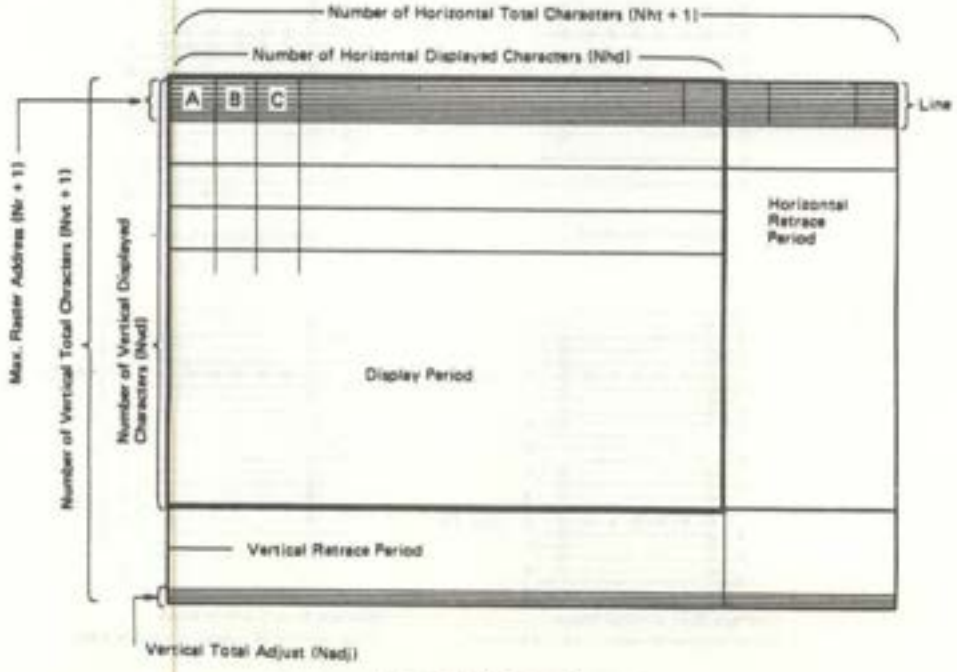


Figure 6 CRT screen Format

Table 8 Programmed Values into the Registers

Register	Register Name	Value	Register	Register Name	Value
R0	Horizontal Total	Nht	R9	Max. Raster Address	Nr
R1	Horizontal Displayed	Nhd	R10	Cursor Start Raster	
R2	Horizontal Sync Position	Nhsp	R11	Cursor End Raster	
R3	Sync Width	Nvsw, Nhsw	R12	Start Address (H)	0
R4	Vertical Total	Nvt	R13	Start Address (L)	0
R5	Vertical Total Adjust	Nadj	R14	Cursor (H)	
R6	Vertical Displayed	Nvd	R15	Cursor (L)	
R7	Vertical Sync Position	Nvsp	R16	Light Pen (H)	
R8	Interlace & Skew		R17	Light Pen (L)	

[NOTE] Nhd<Nht, Nvd<Nvt

The relation between values of Refresh Memory Address ($MA_0 \sim MA_{13}$) and Raster Address ($RA_0 \sim RA_4$) and the display position on the screen is shown in Fig. 15. Fig. 15 shows the case where the value of Start Address is 0.

- **Interlace Control**

Fig. 7 shows an example where the same character is displayed in the non-interlace mode, interlace sync mode, and video mode.

Non-interlace Mode Display

In non-interlace mode, each field is scanned duplicatedly. The values of raster addresses ($RA_0 \sim RA_4$) are counted up one from 0.

Interlace Sync Mode Display

In the interlace sync mode, raster addressed in the even field and the odd field are the same as addressed in the noninterlace mode. One character pattern is displayed mutually and its displayed position in the odd field is set at 1/2 raster space down from that in the even field.

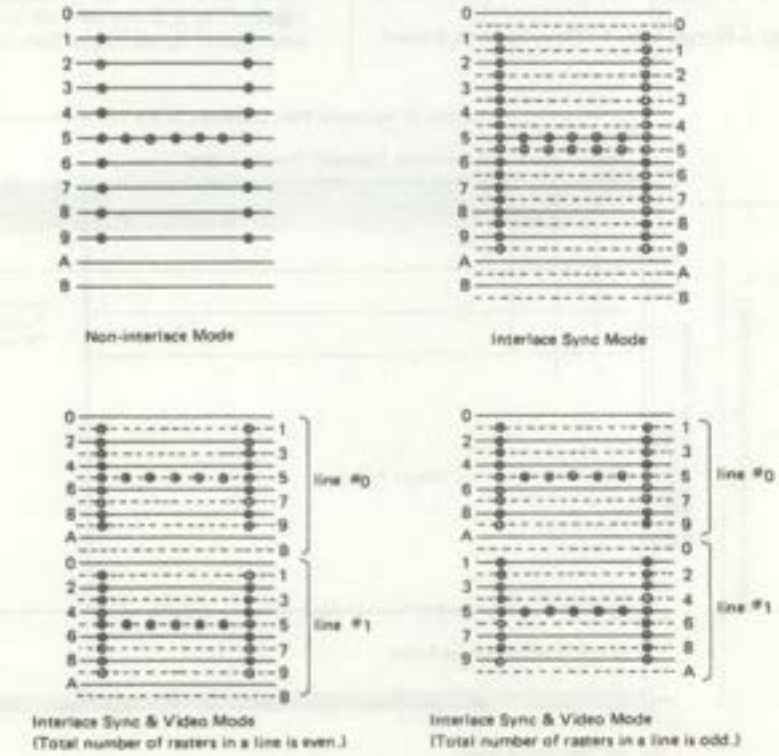


Figure 7 Example of Raster Scan Display

Interlace Sync & Video Mode Display

In interlace sync & video mode, the output raster address when the number of rasters is even is different from that when the number of rasters is odd.

Table 9 The Output of Raster Address in Interlace Sync & Video Mode

Total Number of Rasters in a Line \ Field		Even Field	Odd Field
Even		Even Address	Odd Address
Odd	Even Line*	Even Address	Odd Address
	Odd Line*	Odd Address	Even Address

* Internal line address begins from 0.

1) Total number of rasters in a line is even;

When number of rasters is programmed to be even, even raster address is output in the even field and odd raster address is output in the odd field.

2) Total number of rasters in a line is odd;

When total number of rasters is programmed to be odd, odd and even addresses are reversed according to the odd and even lines in each field. In this case, the difference in numbers of dots displayed between even field and odd field is usually smaller the case of 1). Then interlace can be displayed more stably.

[NOTE] The wide disparity of dots between number of dots between even field and odd field influences beam current of CRT. CRT, which has a stable high-voltage part, can make interlace display normal. On the contrary, CRT, which has unstable high-voltage part, moves deflection angle of beam current and also dots displayed in the even and odd fields may be shifted. Characters appears distroting on a border of the screen. So 2) programming has an effect to decrease such evil influences as mentioned above. Fig. 12 shows fine chart in each mode when interlace is performed.

• Cursor Control

Fig. 8 shows the display patterns where each value is programmed to the cursor start raster register and the cursor end raster register. Programmed values to the cursor start raster register and the cursor end raster register need to be under the following condition.

Cursor Start Raster Register ≦ Cursor End Raster Register ≦ Maximum Raster Address Register.

Time chart of CUDISP output signal is shown in Fig. 13 and Fig. 14.

■ INTERFACE TO DISPLAY CONTROL UNIT

Fig. 16 shows the interface between the CRTC and display control unit. Display control unit is mainly composed of Refresh Memory, Character Generator, and Video Control circuit. For refresh memory, 14 Memory Address line (0~16383) max are provided and for character generator, 5 Raster Address line (0~31) max are provided. For video control circuit, DISPTMG, CUDISP, HSYNC, and VSYNC signals are sent out. DISPTMG signal is used to control the blank period of video signal. CUDISP signal is used as video signal to display the cursor on the CRT screen. Moreover, HSYNC and VSYNC signals are used as drive signals respectively for CRT horizontal and vertical deflection circuits.

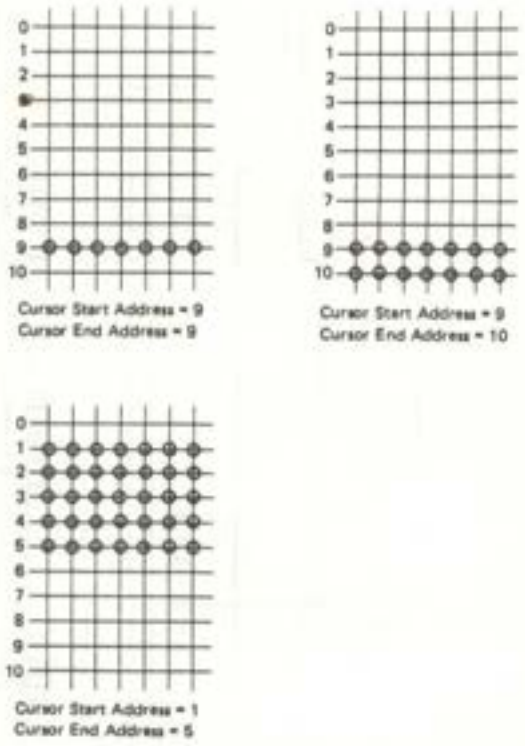


Figure 8 Cursor Control

Outputs from video control circuit, (video signals and sync signals) are provided to CRT display unit to control the deflection and brightness of CRT, thus characters are displayed on the screen.

Fig. 17 shows detailed block diagram of display control unit. This shows how to use CUDISP and DISPTMG signals. CUDISP and DISPTMG signals should be used being latched at least one time at external flip-flop F1 and F2. Flip-flop F1 and F2 function to make one-character delay time so as to synchronize them with video signal from parallel-serial converter. High-speed D type flip-flop as TTL is used for this purpose. After being delayed at F1 and F2 DISPTMG signal is AND-ed with character video signal, and CUDISP signal is OR-ed with output from AND gate. By using this circuitry, blanking of horizontal and vertical retrace time is controlled. And cursor video is mixed with character video signal.

Fig. 17 shows the example in the case that both refresh memory and CG can be accessed for horizontal one character time. Time chart for this case is shown in Fig. 20. This method is used when a few character needed to be displayed in horizontal direction on the screen.

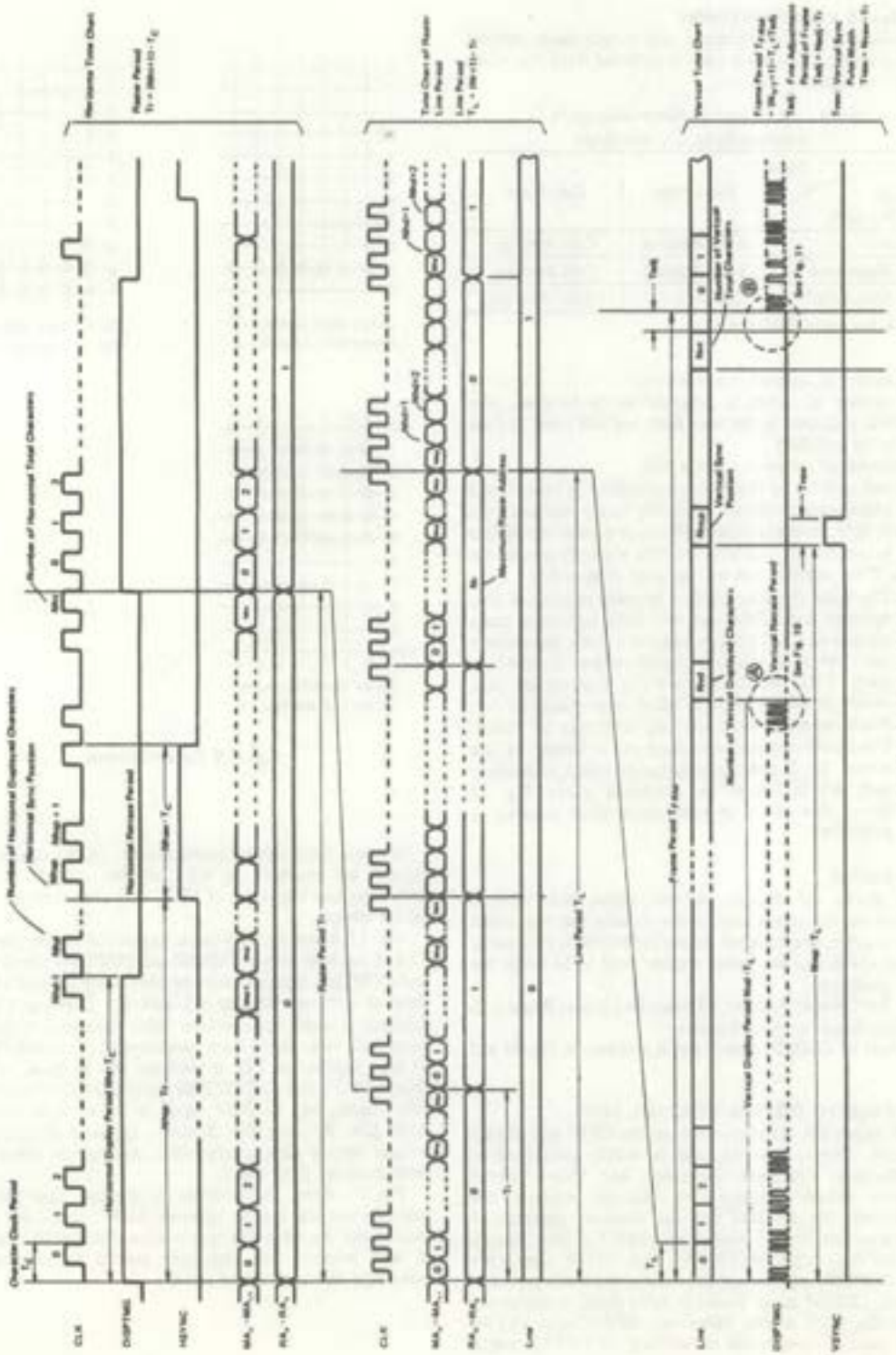


Figure 9 CRTC Time Chart
(Output waveform of horizontal & vertical display in the case where values shown in Table 8 are Programmed to each register.)

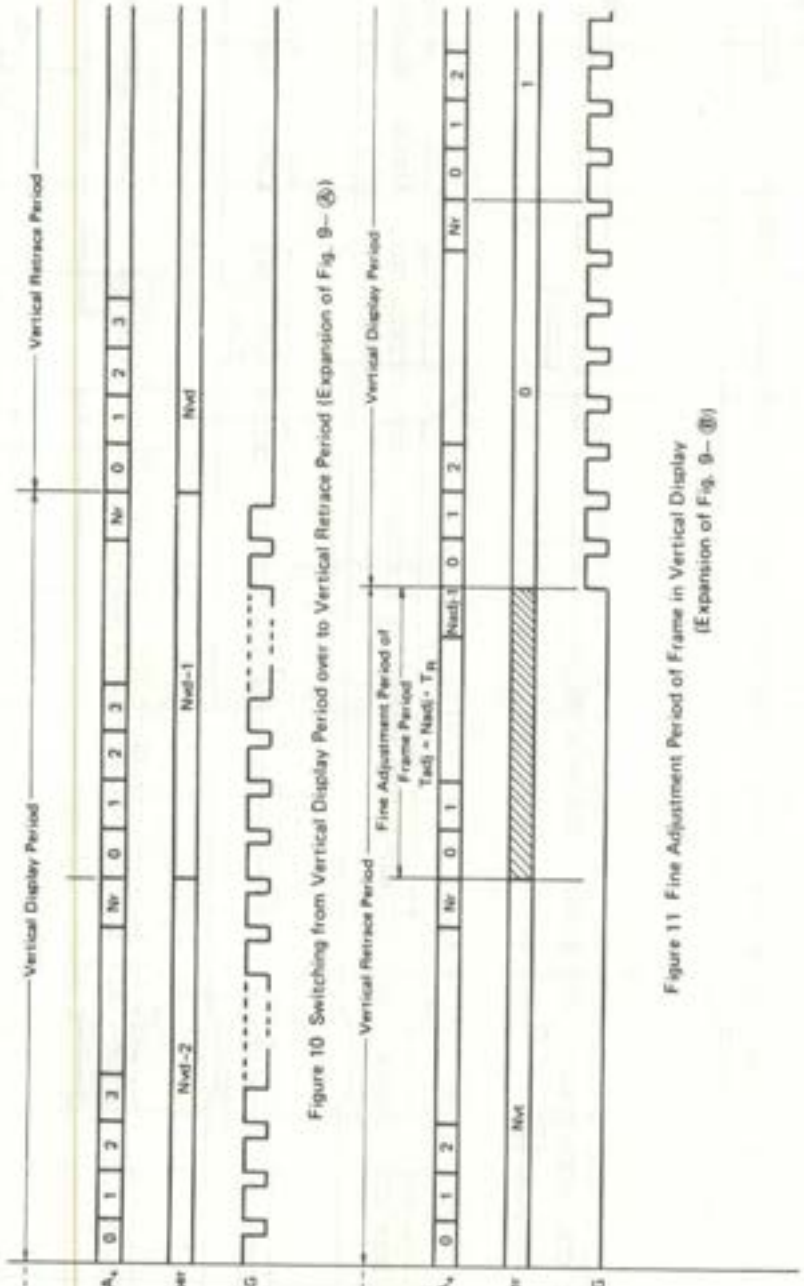


Figure 10 Switching from Vertical Display Period over to Vertical Retrace Period (Expansion of Fig. 9– ⑧)

Figure 11 Fine Adjustment Period of Frame in Vertical Display (Expansion of Fig. 9– ⑧)

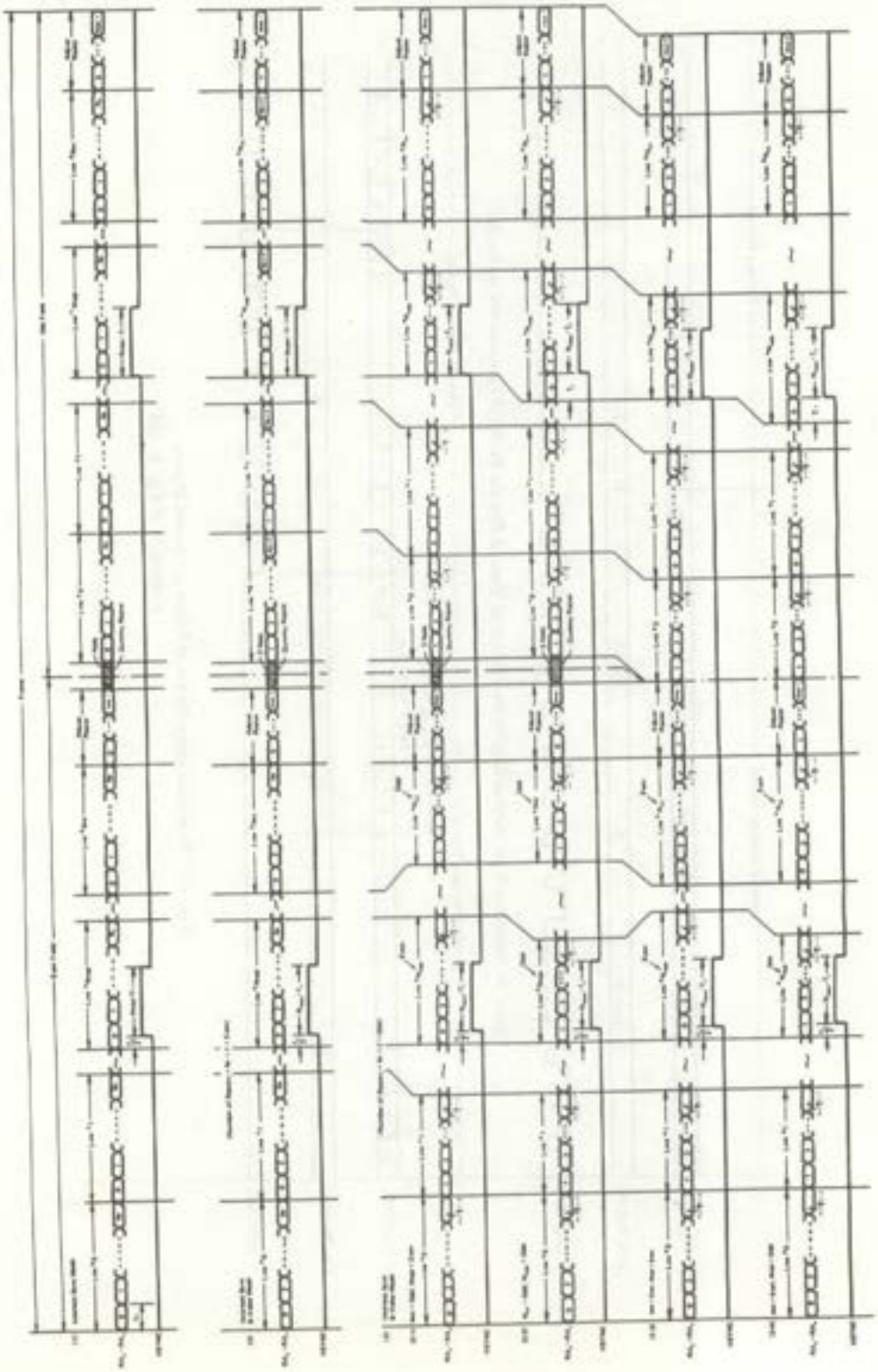


Figure 12 Interlace Control

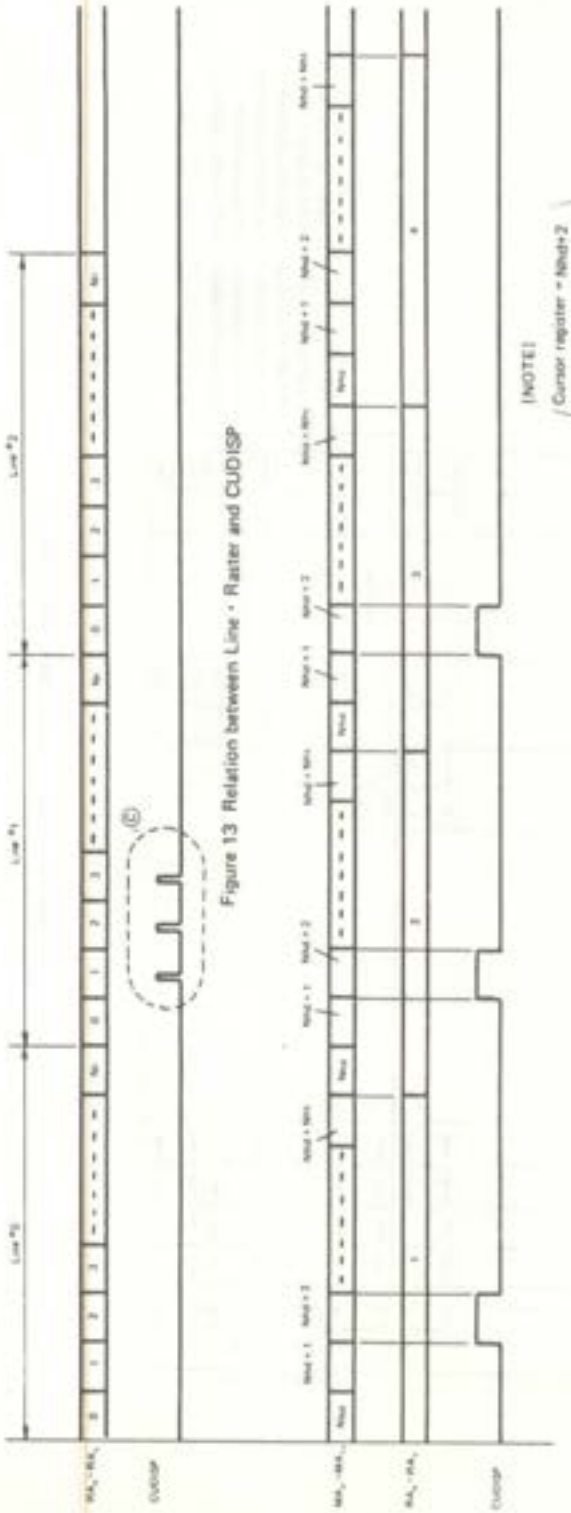


Figure 13 Relation between Line * Raster and CUDISP

[NOTE]
(Cursor register = Nhd+2
Cursor Start
Raster Register = 1
Cursor End
Raster Register = 3
are Programmed in cursor display mode.

In blink mode, it is changed into display or non-display mode when field period is 16 or 32-time period.

Figure 14 CUDISP Output Timing (Expansion of Fig. 13 ©)

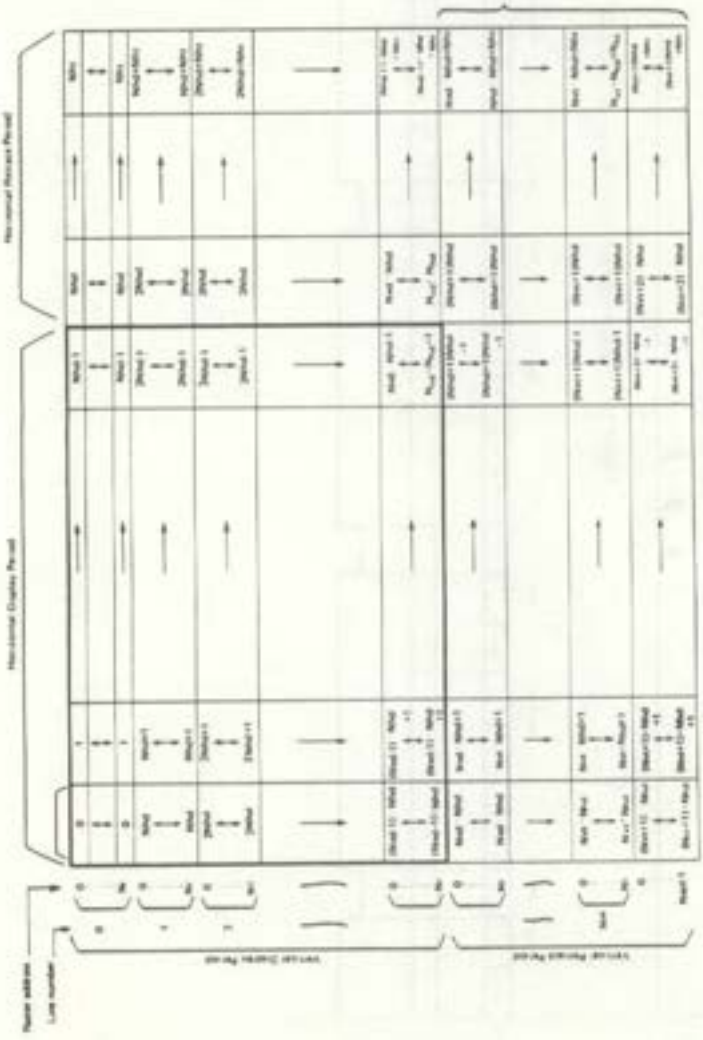


Figure 15 Refresh Memory Address (MA_0~MA_{13})

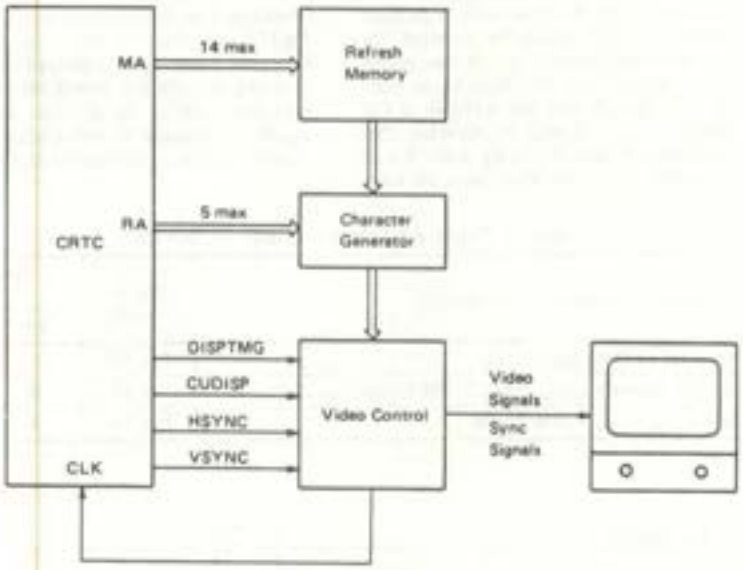


Figure 16 Interface to Display Control Unit

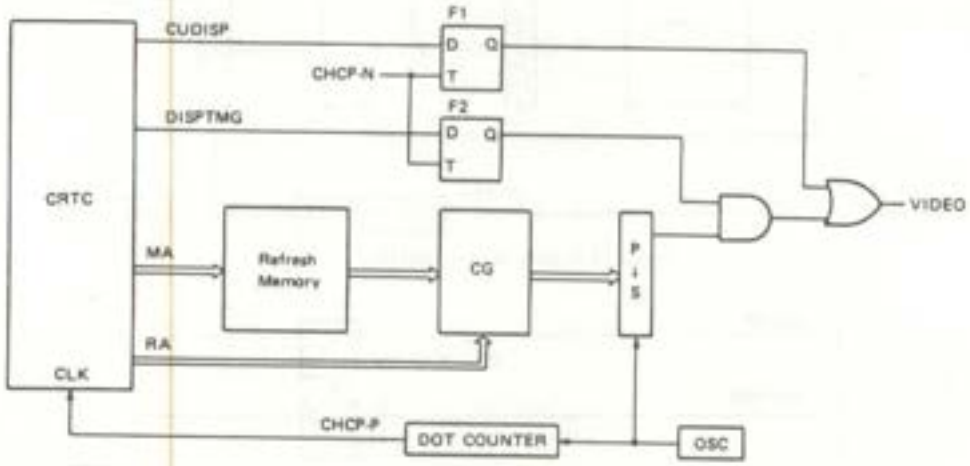


Figure 17 Display Control Unit (1)

When many characters are displayed in horizontal direction on the screen, and horizontal one-character time is so short that both refresh memory and CG cannot be accessed, the circuitry shown in Fig. 18 should be used. In this case refresh memory output shall be latched and CG shall be accessed at the next cycle. The time chart in this case is shown in Fig. 21. CUDISP and DISPTMG signals should be provided after being delayed by one-character time by using skew bit of interlace & skew register (R8). Moreover, when there are some troubles about delay time of MA during horizontal one-character time on high-speed display operation, system shown in Fig.19 is adopted. The time chart in this case is shown in Fig.22. Character video signal is delayed for two-character time because each MA outputs and refresh memory outputs are latched, and they are made to be in phase with CUDISP and DISPTMG signals by delaying for two-character time. Table 10 shows the circuitry selection standard of display units.

Table 10 Circuitry Standard of Display Control Unit

Case	Relation among t_{CH}, RM and CG	Block Diagram	Interlace & Skew Register Bit Programming			
			C1	C0	D1	D0
1	$t_{CH} >$ RM Access + CG Access + t_{MAD}	Fig. 17	0	0	0	0
2	RM Access + CG Access + $t_{MAD} \geqq t_{CH} >$ RM Access + t_{MAD}	Fig. 18	0	1	0	1
3	RM Access + $t_{MAD} \geqq t_{CH} >$ RM Access	Fig. 19	1	0	1	0

t_{CH} : CHCP Period; t_{MAD} : MA Delay

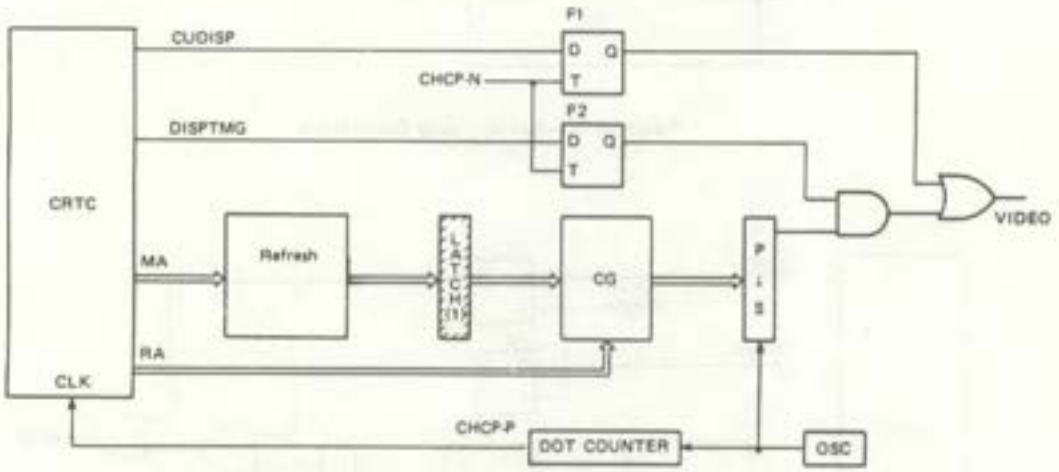


Figure 18 Display Control Unit (2)

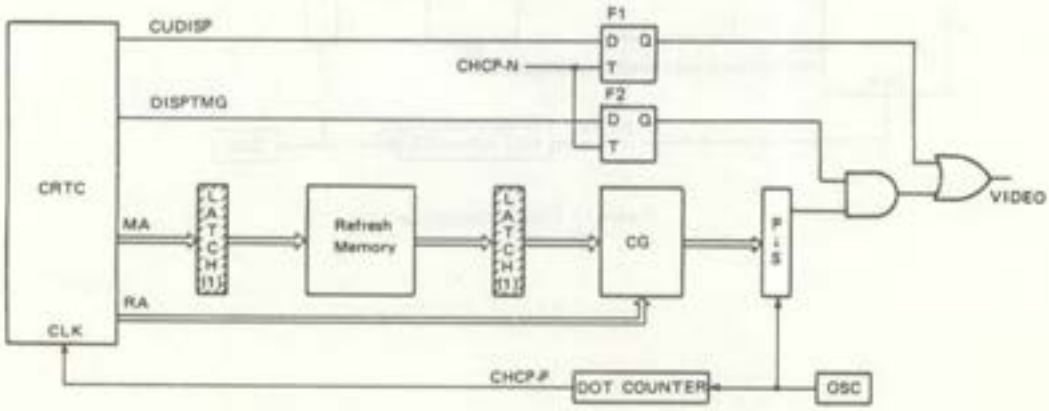


Figure 19 Display Control Unit (For high-speed display operation) (3)

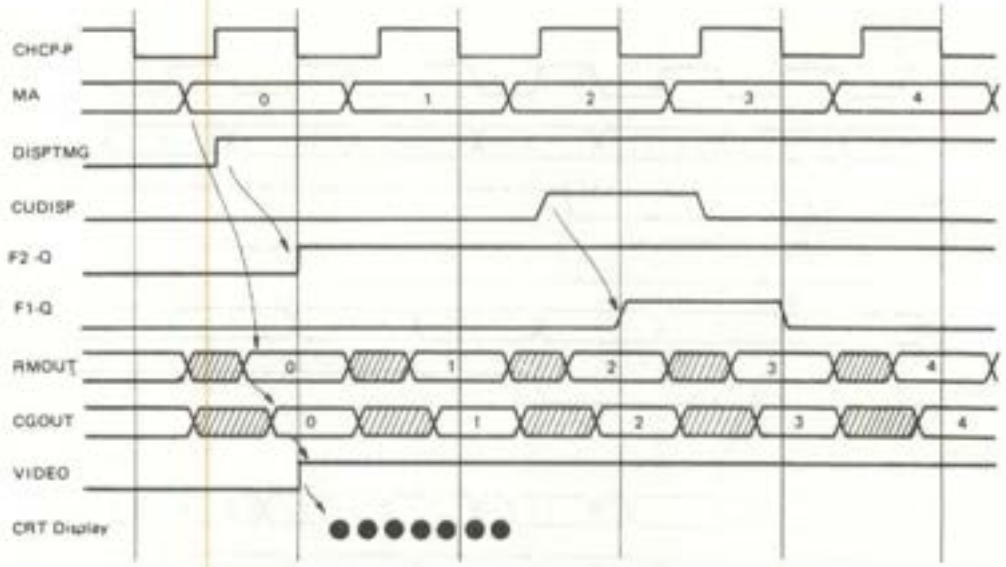


Figure 20 Time Chart of Display Control Unit (1)

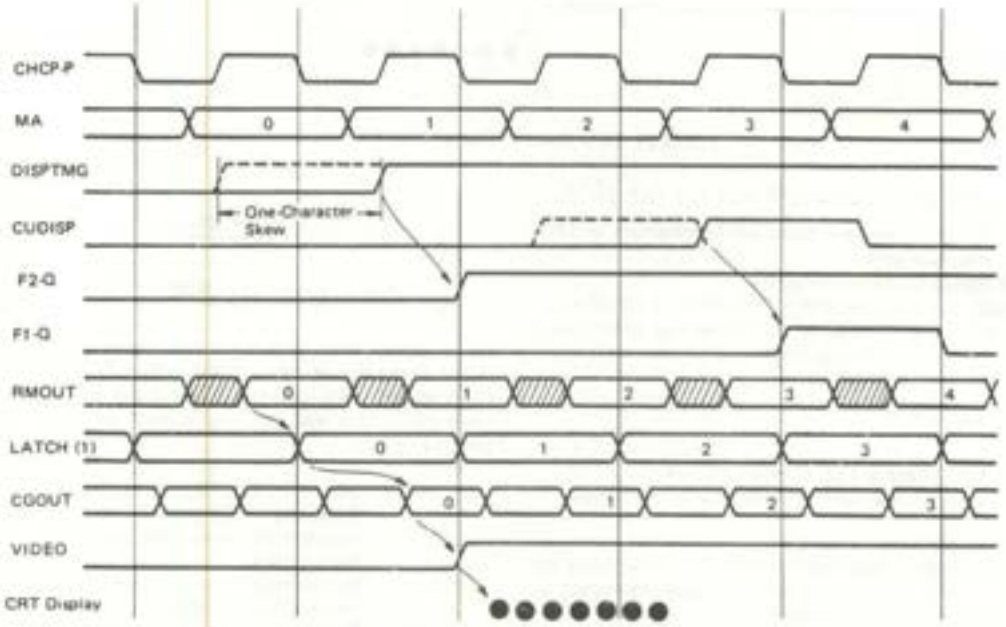


Figure 21 Time Chart of Display Control Unit (2)

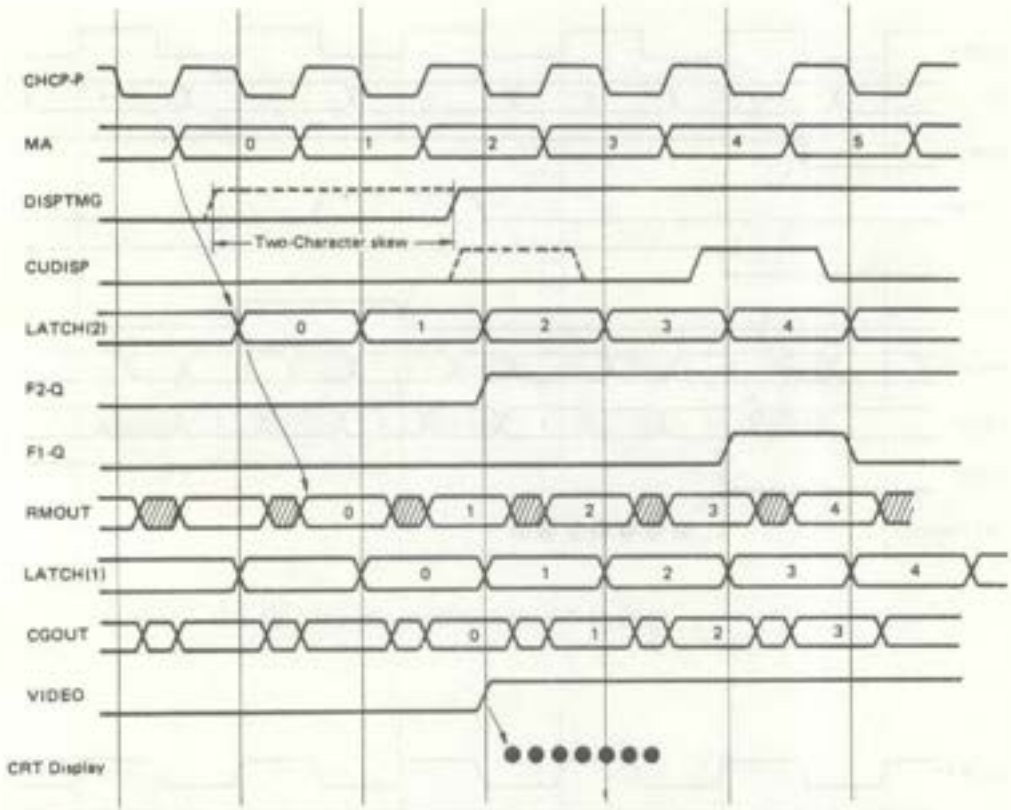


Figure 23 Time Chart of Display Unit (3)

■ HOW TO DECIDE PARAMETERS SET ON THE CRTC

• How to Decide Parameters Based on Specification of CRT Display Unit (Monitor)

Number of Horizontal Total Characters

Horizontal deflection frequency fh is given by specification of CRT display unit. Number of horizontal total characters is determined by the following equation.

$$f_h = \frac{1}{t_C\,(N_{ht} + 1)}$$

where,

t_C : Cycle Time of CLK (Character Clock)
N_{ht} : Programmed Value of Horizontal Total Register (R0)

Number of Vertical Total Characters

Vertical deflection frequency is given by specification of CRT display unit. Number of vertical Total characters is determined by the following equation.

1) Non-interlace Mode
$R_t = (N_{vt} + 1)(N_r + 1) + N_{adj}$
2) Interlace Sync Mode
$R_t = (N_{vt} + 1)(N_r + 1) + N_{adj} + 0.5$
3) Interlace Sync & Video Mode

$$R_t = \frac{(N_{vt} + 1)(N_r + 2) + 2N_{adj}}{2} \quad \text{..... (a)}$$

$$R_t = \frac{(N_{vt} + 1)(N_r + 2) + 2N_{adj} + 1}{2} \quad \text{..... (b)}$$

(a) is applied when both total numbers of vertical characters (Nvt + 1) and that of rasters in a line (Nr + 2) are odd.
(b) is applied when total number of rasters (Nr + 2) is even, or when (Nr + 2) is odd and total number of vertical characters (Nvt + 1) is even.

where,

R_t : Number of Total Rasters per frame (Including retrace period)
N_{vt} : Programmed Value of Vertical Total Register (R4)
N_r : Programmed Value of Maximum Raster Address Register (R9)
N_{adj} : Programmed Value of Vertical Total Adjust Register (R5)

Horizontal Sync Pulse Width

Horizontal sync pulse width is programmed to low order 4-bit of horizontal sync width register (R3) in unit of horizontal character time. Programmed value can be selected within from 1 to 15.

Horizontal Sync Position

As shown in Fig. 24, horizontal sync position is normally selected to be in the middle of horizontal blank period. But there are some cases where its optimum sync position is not located in the middle of horizontal blank period according to specification of CRT. Therefore, horizontal sync position should be determined by specification of CRT. Horizontal sync pulse position is programmed in unit of horizontal character time.

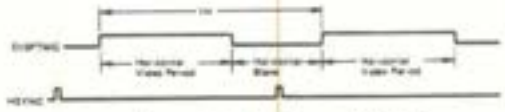


Figure 24 Time Chart of HSYNC

Vertical Sync Pulse Width

Vertical Sync Pulse Width is programmed to high order 4-bit of vertical sync pulse width register (R3) in unit of raster period. Programmed value can be selected within from 1 to 16.

Vertical Sync Position

As shown in Fig. 25, vertical sync position is normally selected to be in the middle of vertical blank period. But there are some cases where its optimum sync position is not located in the middle of vertical blank period according to specification of CRT. Therefore, vertical sync position should be determined by specification of CRT. Vertical sync pulse position is programmed to vertical sync position register (R7) in unit of line period.

• How to Decide Parameters Based on Screen Format

Dot Number of Characters (Horizontal)

Dot number of characters (horizontal) is determined by character font and character space. An example is shown in Fig. 26. More strictly, dot number of characters (horizontal) N is determined by external N-counter. Character space is set by means shown in Fig. 27.

Dot Number of Characters (Vertical)

Dot number of characters (vertical) is determined by characters font and line space. An example is shown in Fig. 26. Dot number of characters (vertical) is programmed to maximum raster address (register R9) of CRTC. When N_R is programmed

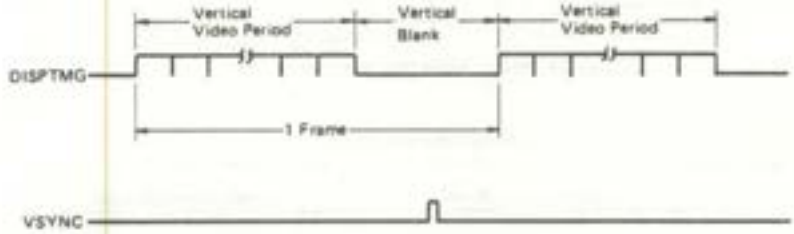


Figure 25 Time Chart of VSYNC

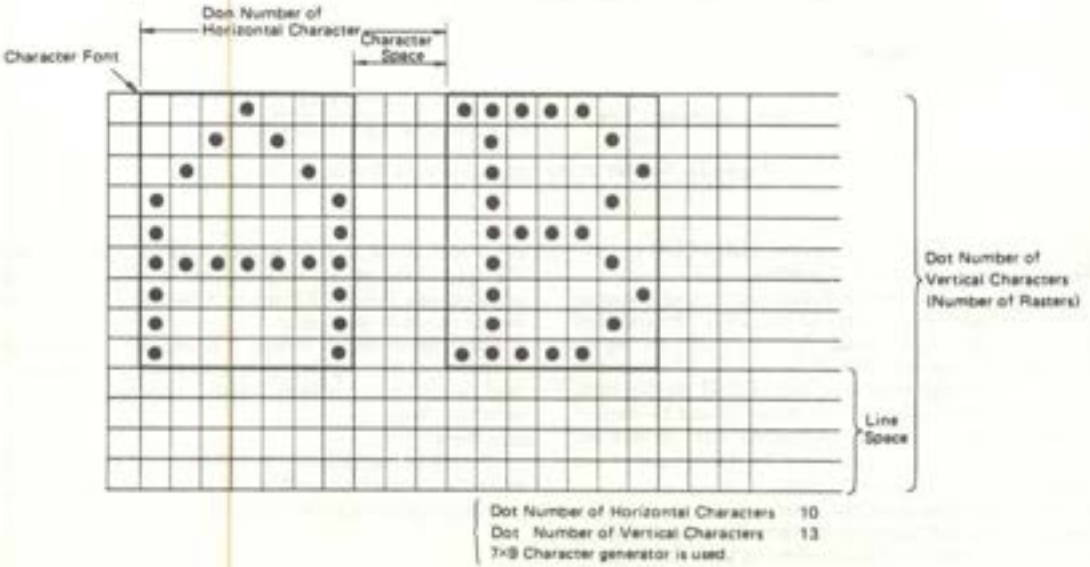


Figure 26 Dot Number of Horizontal and Vertical Characters

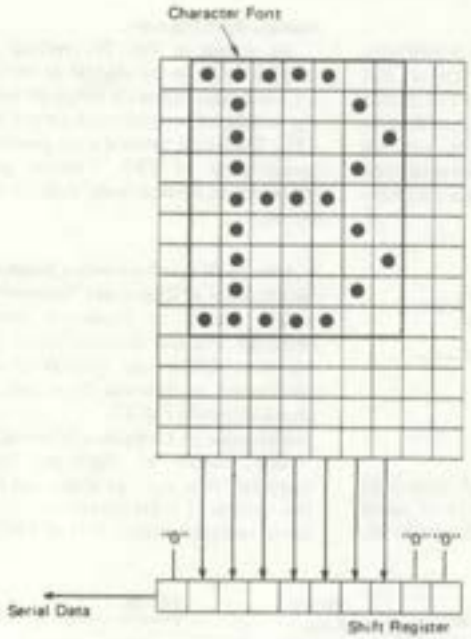


Figure 27 How to Make Character Space

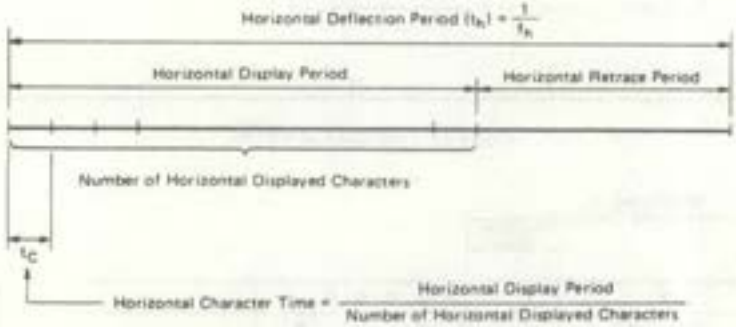


Figure 28 Number of Horizontal Displayed Characters

value of R9, dot number of characters (vertical) is (Nr+1).

Number of Horizontal Displayed Characters

Number of horizontal displayed characters is programmed to horizontal displayed register (R1) of the CRTC. Programmed value is based on screen format. Horizontal display period, which is given by specification of horizontal deflection frequency and horizontal retrace period of CRT display unit, determines horizontal character time, being divided by number of horizontal displayed characters. Moreover, its cycle time and access time which are necessary for CRT display system are determined by horizontal character time.

Number of Vertical Displayed Characters

Number of vertical displayed characters is programmed to vertical displayed register (R6). Programmed value is based on screen format. As specification of vertical deflection frequency of CRT determines number of total rasters (Rt) including vertical retrace period and the relation between number of vertical displayed character and total number of rasters on a screen is as mentioned above, CRT which is suitable for desired screen format should be selected.

For optimum screen format, it is necessary to adjust number of rasters per line, number of vertical displayed characters, and total adjust raster (Nadj) within specification of vertical deflection frequency.

Scan Mode

The CRTC can program three-scan modes shown in Table 11 to interlace mode register (R8). An example of character display in each scan mode is shown in Fig. 7.

Table 11 Program of Scan Mode

2^1	2^0	Scan Mode	Main Usage
0	0	Non-interlace	Normal Display of Characters & Figures
1	0		
0	1	Interlace Sync	Fine Display of Characters & Figures
1	1	Interlace Sync & Video	Display of Many Characters & Figures Without Using High-resolution CRT

[NOTE] In the interlace mode, the number of times per sec. in raster scanning on one spot on the screen is half as many as that in non-interlace mode. Therefore, when persistence of luminescence is short, flickering may happen. It is necessary to select optimum scan mode for the system, taking characteristics of CRT, raster scan speed, and number of displayed characters and figures into account.

Cursor Display Method

Cursor start raster register and cursor end raster register (R10, R11) enable programming the display modes shown in Table 7 and display patterns shown in Fig. 8. Therefore, it is possible to change the method of cursor display dynamically according to the system conditions as well as to realize the cursor display that meets the system requirements.

Start Address

Start address resisters (R12, R13) give an offset to the address of refresh memory to read out. This enables paging and scrolling easily.

Cursor Register

Cursor registers (R14, R15) enable programming the cursor display position on the screen. As for cursor address, it is not X, Y address but linear address that is programmed.

■ EXAMPLES OF APPLIED CIRCUIT OF THE CRTC

Fig. 30 shows an example of application of the CRTC to monochrome character display. Its specification is shown in Table 12. Moreover, specification of CRT display unit is shown in Table 13 and initializing values for the CRTC are shown in Table 14.

Table 12 Specification of Applied Circuit

Item	Specification															
Character Format	5 × 7 Dot															
Character Space	Horizontal : 3 Dot Vertical : 5 Dot															
One Character Time	1 μs															
Number of Displayed Characters	40 characters × 16 lines = 640 characters															
Access Method to Refresh Memory	Snychronous Method (DISPTMG Read)															
Refresh Memory	1 kB															
Address Map		2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	Refresh Memory	0	0	0	0	0	0	*	*	*	*	*	*	*	*	*	*
	CRTC Address Register	0	0	0	1	0	0	×	×	×	×	×	×	×	×	×	0
	CRTC Control Register	0	0	0	1	0	0	×	×	×	×	×	×	×	×	×	1
	× · · · don't care, * · · · 0 or 1															
Synchronization Method	HVSYNC Method															

Table 13 Specification of Character Display

Item	Specification
Scan Mode	Non-interlace
Horizontal Deflection Frequency	15.625 kHz
Vertical Deflection Frequency	60.1 Hz
Dot Frequency	8 MHz
Character Dot (Horizontal × Vertical)	8 × 12 (Character Font 5 × 9)
Number of Displayed Characters (Row × Line)	40 × 16
HSYNC Width	4 μs
VSYNC Width	3 H
Cursor Display	Raster 9 ~ 10, Blink 16 Field Period
Paging, Scrolling	Not used

Table 14 Initializing Values for Character Display

Register	Name	Symbol	Initializing Value Hex (Decimal)	
R0	Horizontal Total	Nht	3F	(63)
R1	Horizontal Displayed	Nhd	28	(40)
R2	Horizontal Sync Position	Nhsp	34	(52)
R3	Sync Width	Nvsw, Nhsw	34	
R4	Vertical Total	Nvt	14	(20)
R5	Vertical Total Adjust	Nadj	08	(8)
R6	Vertical Displayed	Nvd	10	(16)
R7	Vertical Sync Position	Nvsp	13	(19)
R8	Interlace & Skew		00	
R9	Maximum Raster Address	Nr	08	(11)
R10	Cursor Start Raster	B, P, NCSTART	49	
R11	Cursor End Raster	NCEND	0A	(10)
R12	Start Address (H)		00	(0)
R13	Start Address (L)		00	(0)
R14	Cursor (H)		00	(0)
R15	Cursor (L)		00	(0)

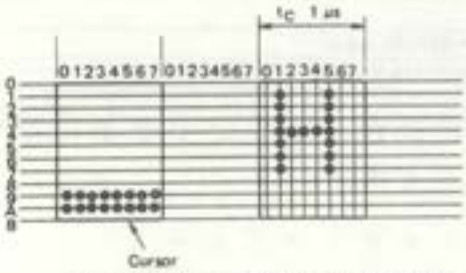


Figure 29 Non-interlace Display (Example)

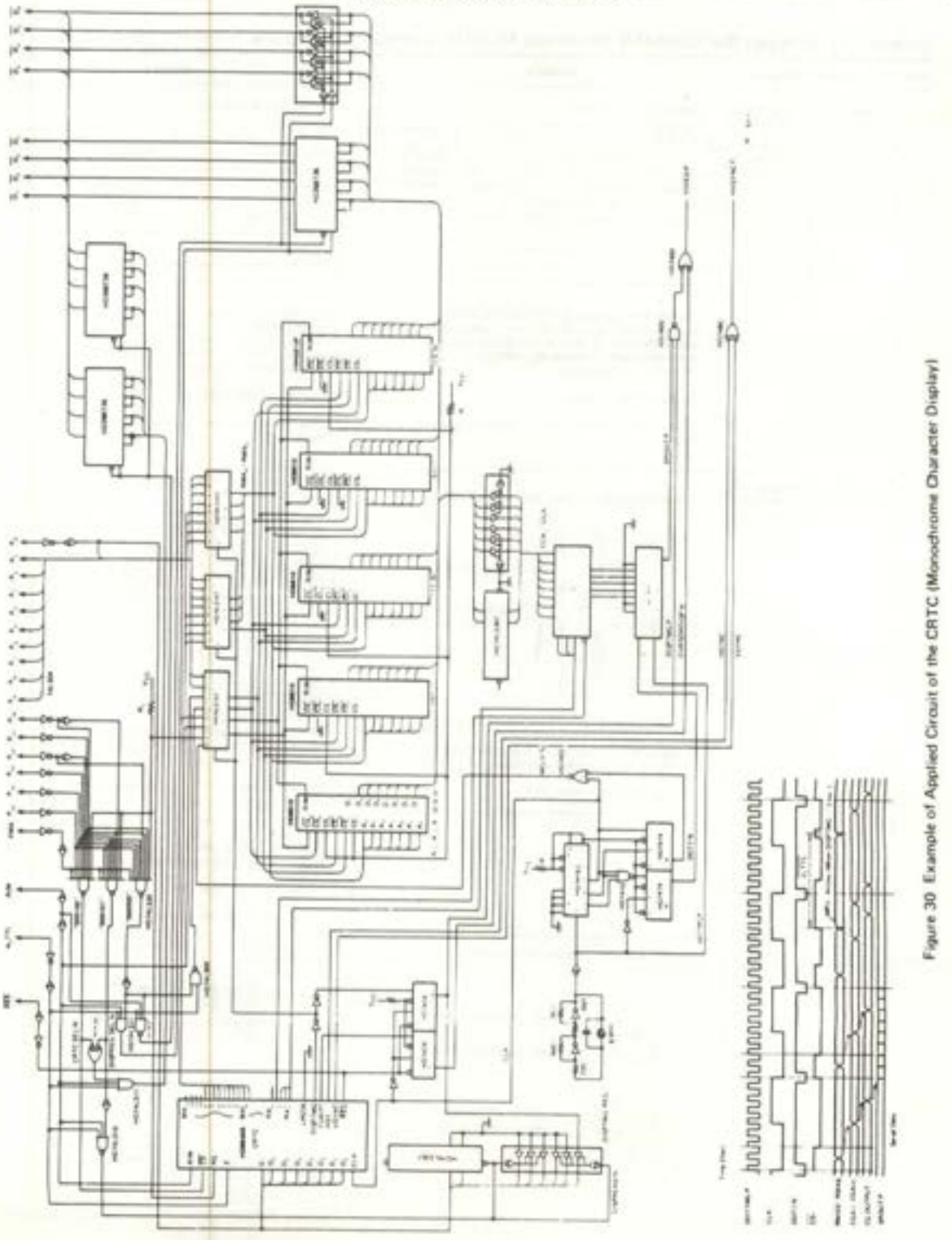
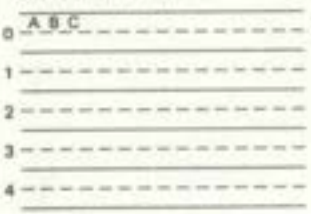
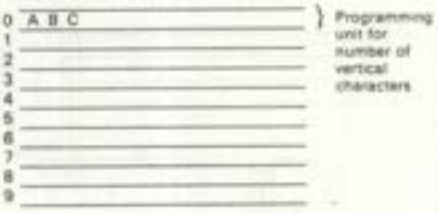
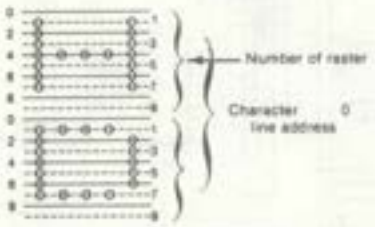
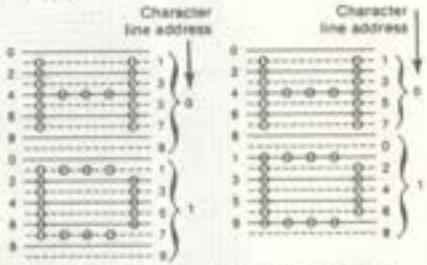
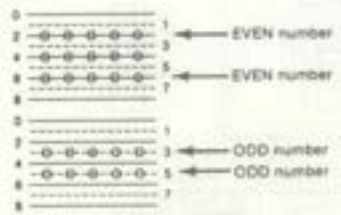
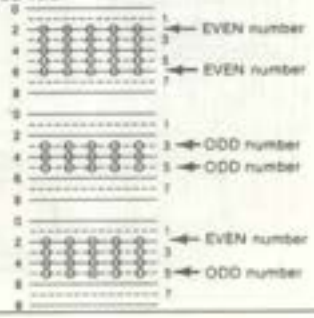
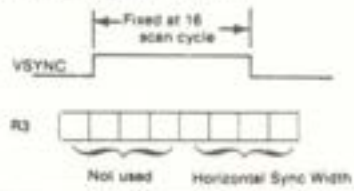
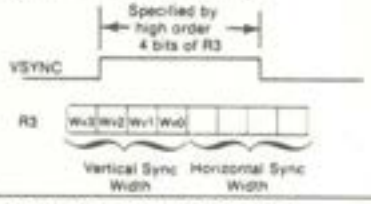
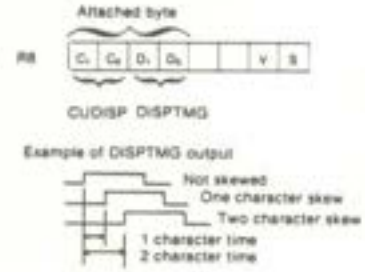


Figure 30 Example of Applied Circuit of the CRTC (Monochrome Character Display)

Differences between the HD6845R (Motorola MC6845 Compatible) and the HD6845S (Enhanced)

No.	Functional Difference		HD6845R	HD6845S
1	Interface Sync & Video Mode Display	Programming Method of number of vertical characters	Character line address  In HD6845R, number of characters is vertically programmed in units of two lines, as illustrated above. (Number of vertical total characters, Number of vertical displayed characters, Vertical Sync Position) Example of above figure Programmed number into Vertical Displayed Register = 5	Character line address  In HD6845S, number of characters is vertically programmed in unit of one line, as illustrated above. (Number of vertical total characters, Number of vertical displayed characters, Vertical Sync Position) Example of above figure Programmed number into Vertical Displayed Register = 10
		Number of raster per character line	Only even number can be specified.  Number of raster = 10 scanline (specified) However, number which is programmed into register is calculated as follows. Programmed number (Nr) = (Number specified) − 1	Both even number and odd number can be specified.  When number of raster per character line is EVEN Number of raster = 10 scan line (specified) When number of raster per character line is ODD Number of raster = 9 scan line (specified) However, number which is programmed into register is calculated as follows. Programmed number (NR) = (Number specified) − 2
		Cursor Display	Cursor is displayed in either EVEN field or ODD field. 	Cursor is displayed in both EVEN field and ODD field. 

No.	Functional Difference	HD6845R	HD6845S
2	Vertical Sync Pulse Width (VSYNC output)	Fixed at 16 raster scan cycle (16H) 	Programmable (1 – 16 raster scan cycle) 
3	SKEW Function	Not included 	SKEW capability is included in DISPTMG, CUDISP signals. 
4	Start Address Register	Write Only	Read or Write
5	RESET Signal (RES)	MA_0 – MA_{13} Output, RA_0 – RA_4 Output ——Synchronous reset Other Outputs ——Asynchronous reset Output signals of MA_0 – MA_{13}, RA_0 – RA_4, synchronized with CLK "LOW" level, go to "LOW" level, after RES has gone to "LOW." Other outputs go to "LOW" immediately after RES has gone to "LOW" level.	MA^* – MA_{13} Output, RA_0 – RA_4 Output, Other Outputs ——Asynchronous reset Output signals of MA_0 – MA_{13}, RA_0 – RA_4 and others go to "LOW" level immediately after RES has gone to "LOW" level.

AC Characteristic Differences between HD6845R (Motorola MC6845 Compatible) and HD6845S (Enhanced)

No.	Characteristic Difference	Symbol	HD46505R			HD46505S			Unit
			min.	typ.	max.	min.	typ.	max.	
1	Clock Cycle Time	tcycc	330	—	—	270	—	—	ns
2	Clock Pulse Width "High"	PW_{CH}	150	—	—	130	—	—	ns
3	Clock Pulse Width "Low"	PW_{CL}	150	—	—	130	—	—	ns
4	Rise and Fall Time for Clock Input	T_{CR}, T_{CF}	—	—	15	—	—	20	ns
5	Horizontal Sync Delay Time	T_{HSD}	—	—	250	—	—	200	ns
6	Light Pen Strobe Pulse Width	PW_{LPH}	80	—	—	60	—	—	ns
7	Light Pen Strobe, Uncertain Time of Acceptance	T_{LPS1}	—	—	80	—	—	70	ns
		T_{LPS0}	—	—	10	—	—	0	ns

SERVICE MODULE

Video Card

Z-309A

ZENITH | data systems

The purpose of this page is to make sure that all service bulletins are entered in this manual. When a service bulletin is received, annotate the manual and list the information in the record below.

Record of Service Bulletins

SERVICE BULLETIN NUMBER	DATE OF ISSUE	CHANGED PAGE(S)	PURPOSE OF SERVICE BULLETIN	INITIALS

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Abbreviations

ASCII	American Standard Code for Information Interchange
Addr	Address
B	Blue
Char	Character
CPU	Central Processing Unit
CRT	Cathode Ray Tube
CRTC	Cathode Ray Tube (monitor) Controller
D/A	Digital-to-Analog
Dispd	Displayed
G	Green or (buffer) Gate
Hex	Hexadecimal
Horiz	Horizontal
I	Intensity
IC	Integrated Circuit
I/O	Input/Output
K-byte	Kilobyte
LED	Light-Emitting Diode
LSB	Least-Significant Bit
Max	Maximum
MHz	Megahertz
MSB	Most-Significant Bit
PAL	Programmable Array Logic
pF	Picofarad
Pixel	Picture Element
R	Red
RGB	Red, Green, Blue
RAM	Random Access Memory
Reg	Register
RF	Radio Frequency
ROM	Read-Only Memory
R/W	Read/Write
Stat	Status
Sync	Synchronization
TTL	Transistor-Transistor Logic
µF	Microfarad
µH	Microhenry
Vert	Vertical
XOR	Exclusive OR

Chapter 1

Introduction and Specifications

Introduction

The Z-309A Video Card provides an interface between the computer and various display output devices, including a monochrome monitor and a color monitor. An optional light pen also may be interfaced through this card. The monochrome output is connected to an RCA phono jack, and the RGB, or color output, to a 9-pin D-type connector. Both connectors are located on the video card and project through the rear of the computer cabinet. The 309A Video Card also provides a connector for interconnecting an optional Z-100 Video Card.

Following are features, functions, and capabilities of the 309A Video Card.

Specifications

- Addressing, and reading and writing to the 16K video RAM;
- Foreground, background, and border color selection;
- Mode selection (text mode or all-points-addressable graphics);
- Alphanumeric and special character generation;
- 7 or 14 MHz video bandwidth, mode-dependent;
- Monochrome and/or color (RGB) output;
- Internal and external vertical, horizontal, and/or composite sync selection;
- Light pen interface;
- Cursor-type selection (block, line, blinking, etc.);
- ROM-based or user-designed character font selection.

Chapter 2

Configuration

Introduction

This chapter describes the optional functions obtainable through positioning the configuration jumpers located on the 309A Video Card.

When using the following instructions, should it become necessary to access and/or remove the video card, refer to the base unit cabinet disassembly and video card removal and replacement procedures in the appropriate *Base Unit Service Module*.

CAUTION: This card contains electrostatic-sensitive devices (ESD). Exercise extreme care when handling these devices to prevent damage.

Refer to Figure 2.1 for the location of the hardware jumpers mentioned in the following paragraphs.

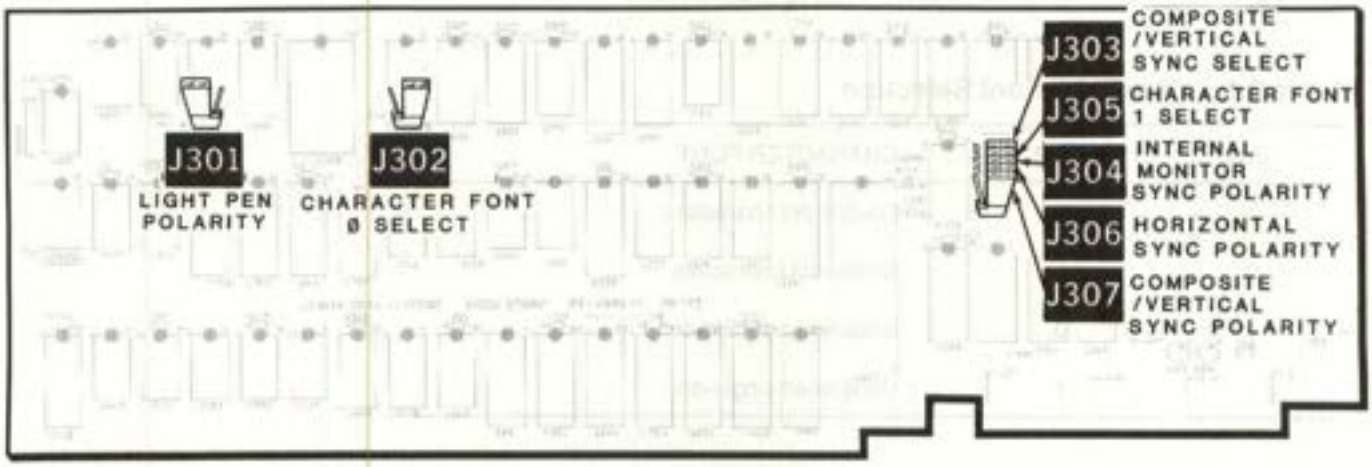


Figure 2.1. Video Card Jumper Locations

The eight programming jumpers located on your video interface card can be used to set initial power-up parameters:

- to drive different types of monitors;
- configure proper input polarity from a light pen device;
- and select the desired character font.

Light Pen Polarity

If a light pen with a positive-going pulse output is being used, position J301, the light pen jumper, to "+". If the pen outputs a negative-going pulse, position J301 to "−".

Character Font Selection

J302 and J305 are the character font selection jumpers. The condition of these jumpers is polled when you first turn on the computer, and will determine which of the character fonts to use. Position the jumpers to the "0" or "1" markings on the card corresponding to the desired font. The logic outlined in Table 2.1 determines font selection.

Table 2.1. Character Font Selection

J305	J302	CHARACTER FONT
0	0	Double-dot characters
0	1	Single-dot characters
1	0	Underlined double-dot
1	1	Underlined single-dot

Monitor Synchronization

If an RGB monitor which requires composite (horizontal and vertical) sync is being used, position J304 to "C". If the monitor requires separate horizontal and vertical sync, position J304 to "V".

Position J303 to the card markings corresponding to the horizontal sync polarity required by the internal monochrome monitor, positive "+" or negative "−".

Position J306 to the markings corresponding to the vertical sync polarity required by the internal monochrome monitor, positive "+" or negative "−".

Position J307 to the markings which correspond to the horizontal sync polarity required by the RGB monitor, positive "+" or negative "−".

Position J308 to the markings which correspond to the vertical/composite sync polarity required by the RGB monitor, positive "+" or negative "−".

Chapter 3

Basic Theory of Operation

The following paragraphs detail the various functions and features of the Z-309A Video Card.

Major Components

Refer to Figure 3.1, the video interface block diagram, for the following descriptions.

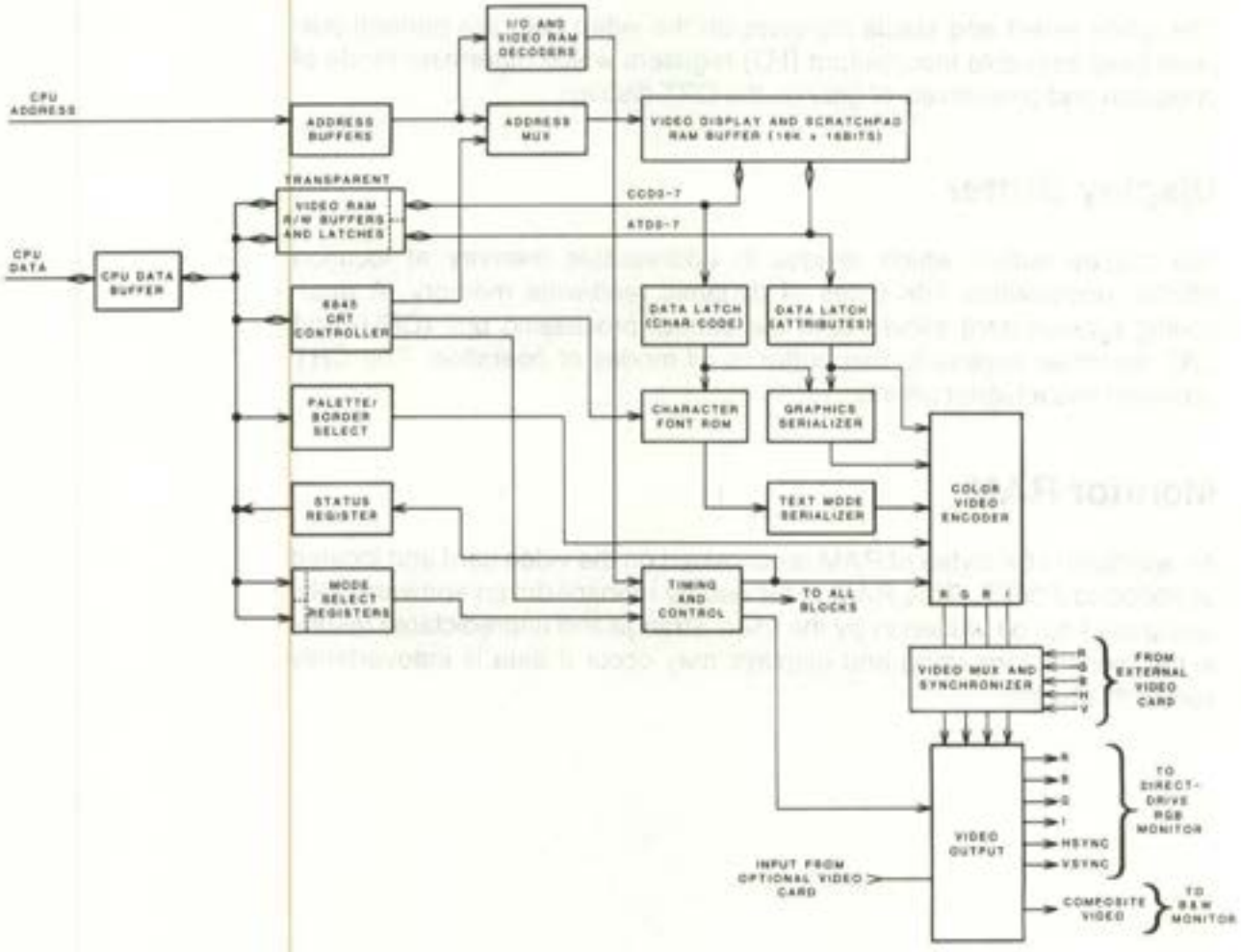


Figure 3.1. Video Interface Block Diagram

CRT Controller

A 6845 CRT controller integrated circuit (IC) provides the proper drive signals for a raster-scan type CRT. The device is highly programmable with regard to raster and character manipulation, and allows for the implementation of many display modes.

Mode Select and Status Registers

The mode select and status registers on the video card are general purpose programmable input/output (I/O) registers which determine mode of operation and color/levels of gray on the CRT display.

Display Buffer

The display buffer, which resides in addressable memory at location B8000, incorporates 16K-bytes of dynamic read/write memory. A dual-porting arrangement allows both the central processing unit (CPU) and CRT controller access to this buffer in all modes of operation. The CRT controller has a higher priority.

Monitor RAM

An additional 16K-bytes of RAM is contained on the video card and located at F0000 to F3FFF. This RAM is for use by monitor-driven software only, and should not be written to by the user. Strange and unpredictable results in the monitor formatting and displays may occur if data is inadvertently sent to this buffer.

Character Font ROM

The ROM character generator on the video card, when in text mode, generates characters from dot patterns stored in the ROM. Two character configurations are provided: a 7 × 7 double-dot and a 5 × 7 single-dot width character set. You may install the hardware jumpers supplied to enable either of the fonts at power up, and use 8088 input/output (I/O) OUT commands to program-select the fonts.

Timing Generator

The timing generator creates the timing signals for the 6845 CRT controller and the dynamic display memory. It also handles traffic control between the CPU and CRT controller for display buffer access.

Color Video Encoder

The color video encoder accepts the color and mode-select information along with appropriate timing and control signals, then generates color video dots information. This is sent to the video output circuitry for further processing.

Video Output

The video output circuitry routes the video information to the proper output connector. It sends color dots to an RGB connector, and generates levels of gray for a monochrome monitor.

Modes of Operation

The Z-309A Video Card can be selected to operate in one of two major modes of operation: text mode or all-points-addressable graphics mode. Additional submodes are available within each mode for either color or monochrome display.

Text Mode

In text mode, the display formats in either a 40-column by 25-line submode, or in an 80-column by 25-line submode. In either submode, characters are formed in an 8 dot × 8 dot matrix.

In either submode, characters only use a 7 × 7 portion of the dot matrix, with one line of descender for lowercase alphabetical characters. Both uppercase and lowercase characters are available in all modes.

On a monochrome display, several features are available: reverse video; blinking; highlighting; and 16 levels of gray for foreground and background, on an individual character basis. On an RGB monitor, 16 foreground, background, or border colors, blinking, and highlighting are available on a per-character basis.

Using 40 × 25 resolution requires 1000 bytes for character information storage, and 1000 bytes for attribute or color information for one screen page of information. Since there are 16K-bytes of video memory, up to eight pages of screens can be stored in video memory; additionally, since all the video memory is directly addressable by the CPU, extreme flexibility in manipulation of screen contents is obtainable.

Using 25 × 80 format, the same rules apply, but since there are twice as many characters per row at this resolution, 4000 bytes of video memory are required to store one screen. Hence, only four screens may be stored at one time.

Text Mode Display Architecture

A two-byte character/attribute format is used to define each character display position. These two bytes are mapped into assigned locations in the screen video RAM (this buffer is part of the video interface, not system memory). Table 3.1 shows the codes assigned to the particular character attribute desired for a monochrome display. The starting address (character byte) must be an even-numbered location.

Table 3.1. Monochrome Character/Attribute Selection

CHARACTER BYTE (M)	ATTRIBUTE BYTE (M + 1)
7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0
Function	7 6 5 4 3 2 1 0
Normal video	B 0 0 0 I 1 1 1
Reverse video	B 1 1 1 I 0 0 0
Non-display (black)	B 0 0 0 I 0 0 0
Non-display (white)	B 1 1 1 I 1 1 1
Underline (normal)	B 1 0 0 I 1 1 1

If B (bit 7) is logic one, foreground blinks. If I (bit 3) is logic one, foreground is intensified.

Note that bits 0 through 2 and bits 4 through 6 are either all logic ones (white) or all logic zeroes (black), in monochrome submode. All other combinations of these bits are used to obtain the desired foreground and background colors on an RGB monitor, or levels of gray on a monochrome monitor.

Table 3.2 shows the attribute byte breakdown. As before, bits 7 and 3 determine blink and intensity, respectively, of the foreground character.

Table 3.2. Color Attribute Byte Logic

COLOR	BACKGROUND 6 5 4	FOREGROUND 2 1 0
Black	0 0 0	0 0 0
Blue	0 0 1	0 0 1
Green	0 1 0	0 1 0
Cyan	0 1 1	0 1 1
Red	1 0 0	1 0 0
Magenta	1 0 1	1 0 1
Brown	1 1 0	1 1 0
Light Gray	1 1 1	1 1 1

Intensified brown is yellow. Intensified light gray is white. Intensified black is dark gray.

Graphics Mode

In graphics mode, two degrees of resolution are available: 320 × 200 and 640 × 200. 640 × 200 resolution is obtainable only as a monochrome display, since the full 16 K-bytes of video memory is needed to define the ON or OFF states of a screenful of pixels (picture elements). If a color other than white is desired for the ON state of a given pixel, one of the 16 border colors may be selected. In the 320 × 200 resolution, each pixel may be one of four colors. This color may be one of the 16 background colors or one of three other colors software-selected from the red/green/brown palette or the cyan/magenta/white palette.

Color (Medium Resolution) Graphics

Pixel information is stored in video memory in two banks of 8000 bytes each, as shown in Figure 3.2, with address B8000 containing color selection data for the pixels in the upper-left corner of the display area. Addresses B8000 to B9F3F contain information for pixels in even-numbered rows 0 through 198, and addresses BA000 to BBF3F for odd-numbered rows 1 through 199.

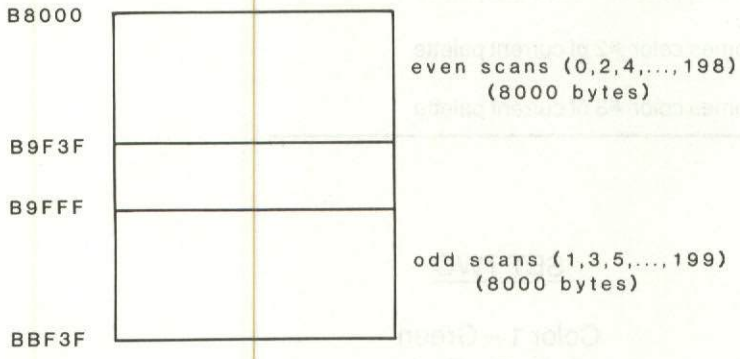


Figure 3.2. Graphics Storage Map

Each video memory byte contains color information for four pixels in two-bit pairs, as in the following format:

```
          7  6  5  4  3  2  1  0

C1  C0  |  C1  C0  |  C1  C0  |  C1  C0
```

For a given pixel bit-pair composed of bits C0 and C1, the following logic, Table 3.3, determines which color is selected from one of four colors: the current background color or one of the colors from the current palette.

Table 3.3. Color Select Logic

C1	C0	COLOR SELECT CODE
0	0	Pixel becomes the current background color
0	1	Pixel becomes color #1 of current palette
1	0	Pixel becomes color #2 of current palette
1	1	Pixel becomes color #3 of current palette

The palettes are structured as follows:

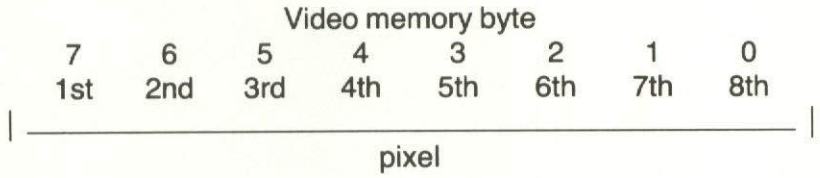
SET ONE	SET TWO
Color 1 – Cyan	Color 1 – Green
Color 2 – Magenta	Color 2 – Red
Color 3 – White	Color 3 – Brown

The possible background colors are the same eight basic colors used in low resolution graphics, plus the lighter shades of these colors which result when intensified, for a total of sixteen colors including black and white (see Table 3.2).

In order to obtain the lighter (intensified) shades, the monitor being used must be capable of recognizing the "I" bit.

High Resolution (640 × 600) Graphics

The high resolution graphics submode, as mentioned previously, may be implemented only in a monochrome format because of memory limitations. Addressing and mapping is the same as medium resolution, but formatting of the data is different. In this submode, each bit, as opposed to a bit-pair, represents a pixel on the screen as shown:



For detailed information on implementing the various modes and submodes, refer to the register descriptions in "Troubleshooting," Chapter 5.

Chapter 4

Detailed Circuit Description

General

Before studying this material, it is suggested that you read Chapter 3, "Basic Theory of Operation," for an overall view of video card functions and operations.

Refer to the video card schematic, and to the individual schematic breakdowns in Chapter 9 for each of the following circuit descriptions.

Bus Interface

Refer to Figure 9.1 in "Foldouts," Chapter 9, which shows the manner in which system I/O interfaces with the video card. U359, U360, U361, and U340 are buffers for the I/O signals used by the video card. The backplane edge connector, an integral part of the video card, provides these signals, as well as D0 through D7, the data information, +12 VDC, +5 VDC, and the I/O CHRDY (ready) signal which is applied to the video timing and control circuitry.

After buffering, the 20 address lines, BA0 through BA19, and BMW*, BMR*, BIOW*, BIOR*, DACK0*, AEN, CLK, RESET*, and OSC are sent out to other portions of the video circuitry.

U358 is a bidirectional data buffer which determines whether data is routed to the video card from the system bus, or to the I/O channel data bus from the video card.Two sections of U303, configured as negative-logic AND gates, and sections of U301 and U347, configured as negative-logic OR gates, determine the direction and enabled/disabled state of U358, in accordance with the states of the BMR*, BIOR*, AEN, VMEMSEL*, SEL3DX*, and IOAXS* signals.

The G input of U358 will be enabled if either UMEMSEL* or SEL3DX* and IOAXS* are active-low. The direction of data travel is determined by the logic state on the DIR input. When BMR* is low, the DIR line also is low and the data flows from the video card to the bus. If the G input is high, the buffer is isolated or tri-stated, and data does not transfer in either direction regardless of DIR state.

+5 VDC is filtered, decoupled, and filtered again by C342, C341, C338, C337, C336, C335, C334, C333, and C301 through C332, before being used as operating power by the video board TTL devices.

Video I/O Ports

The video I/O ports, Figure 9.2, perform video mode selection and status transfer between the video card and the system in accordance with port-select signals routed from the video I/O decoder circuits.

Data lines D0 through D7 provide the values for the various register operations.

Ports 3D8 and 3D9 are output (write) only registers. 3D8 acts as a mode-select register to configure the video interface for the desired operation. This register determines low, medium, or high resolution mode, monochrome or color, and enables or disables the video interface and character blink. Port 3D9 determines color palette in use and screen border color. It also selects intensified background colors.

The port at 3DA is either read or written to, determined by the condition of BIOW* or BIOR* signal. If BIOW* (write) is active-low, U357, the mode-select register, is written to. If BIOR* is active-low, the status register, U351, is read from.

Refer to Chapter 5, "Troubleshooting," for details on these register functions.

This video card uses two character fonts — font 0 and font 1 — and J302 and J304 should be positioned accordingly, as described in Chapter 2, "Configuration."

CRT Controller, Buffers, and Latches

Figure 9.3 details the main video control circuit and the character and attribute byte data latches and input buffers.

U337 is the video card CRT controller IC. It uses the signals at its input to select and control desired parameters and video memory addresses.

The input signals to the CRT controller are defined in Chapter 5, "Troubleshooting."

BA3, the buffered address bit 3 signal, in conjunction with SEL3DX, selects the CRT controller. BA0 acts as the CRT controller register select signal.

In addition to video memory addressing information, U337 supplies vertical and horizontal sync timing, character row information, and cursor and display-enable status signals to appropriate circuitry on the video card.

U356 and U354 are the character code data latch and input buffer, respectively. D0 through D7, representing the character code, are written onto the character data bus and into video RAM as CCD0 through CCD7 when U354 is enabled by the write video RAM, WVRAM*, signal.

The character code is read from video RAM as U356 receives an active-high CPU access, CPUAXS, signal and an active-low read video character code, RVCC*, signal.

U355 and U353 are the attribute code data latch and input buffer, respectively. Following receipt of the character code, the next D0 through D7 byte representing the attribute code are driven onto the attribute data bus as ATD0 through ATD7 when U353 is enabled by WVRAM*.

The attribute code is read from attribute memory as U355 receives the CPUAXS and read video attribute code, RVAT*, signals.

Bytes always must be written in pairs, the first byte always representing the character code, and the second the attribute code.

Video RAM Address Multiplexers

Figure 9.4 represents the address multiplexers used to interface to the video RAM. U315, U310, U316, and U336 use ADMUX as a bit-group select signal to form the two 8-bit (RAM0 through RAM7) locations. Q3P and Q3P* select either the bus (CPU) or CRT controller as the addressing device.

Bits BA0 through BA13 are the buffered CPU address lines, and MA0 through MA13 the CRT controller lines. Arbitration is determined by Q3P and Q3P*, which are alternately low and high.

U336 is a programmable array logic (PAL) chip used as a quad 4-to-1 decoder, which uses the PSEL, SA11, and SA12 signals to support scrolling operations in the different video modes. Chapter 7 contains the equations which determine the logical functioning of this device.

Video RAM, Data Latches, Serial Output

Refer to Figure 9.5.

U312 and U308 form the video RAM for character code storage. U309 and U314 store attribute codes. There are 8 K-bytes of RAM available for character code storage, and 8 K-bytes for attribute code storage, resulting in 16 K-bytes total for monitor screen information storage.

Eight K-bytes of each bank are used as scratchpad RAM for ROM-based functions.

To access a given memory location in the character RAM bank, the first 8-bit address byte is latched off the RAM0-RAM7 bus when row-address select signal RASCC*, from the RAM controller, goes low and is retained as the row-address byte. A few nanoseconds later, the column-address select, CAS*, signal goes low and the next 8-bit byte is fetched, to complete the cycle. The two bytes together determine the desired physical address.

If WVRAM* is low, the D0-D7 data is written into the banks.

The attribute memory banks function in much the same fashion, except that proper timing must be preserved between character and attribute data access. This is accomplished by using RASAT* as the row-address select. The attribute data is retrieved off the ATD0-ATD7 data bus.

Data is applied to U306, the character font ROM IC, and the value represented used to select the desired character from the font. The dot pattern corresponding to this character code is then sent to U305, a text mode serializer, which takes the parallel data and translates it to a serial format. The output, a stream of coded character dots, is then sent to the dot synchronizer part of the timing and control circuitry.

In graphics mode, even-numbered code bits are applied to U328, and odd-numbered bits to U348, to contribute to the forming of the serialized C0 and C1 graphics information.

Data on ATD0 through ATD7, the attribute bus, is applied to U352, the attribute code latch, which picks off the attribute value and sends it to U327, another latch, to U348, which forms the C1 composite serial signal, and to U328, which forms the C0 composite serial signal.

U327, the additional attribute latch, is used to provide proper timing of the attribute bits, AT0 to AT7, in text mode, before application to the color encoder circuitry.

Q0 and Q1* are applied to a negative-logic AND gate, part of U345, the output of which, along with Φ 1 and CLR S/R*, becomes the S/L* CLK and CLR signals for the three graphic serializer ICs.

U344, a D-type flip-flop, provides the proper blink attribute timing. It uses inputs composed of ATD7, Q1*, and HI-B on its D, CLK, and PR/CLR lines, respectively.

Video Timing and Control

Figures 9.6 and 9.7 depict the video timing and control circuits. These circuits are responsible for insuring that the video functions occur when they should.

Refer to Figure 9.6. The system OSC signal, which switches at a rate of 14.3 MHz, is the basic timing unit from which are derived the video timing signals.

U331, a divide-by-two counter, derives the 7.15 MHz signal from the system OSC signal and applies it to U332, the RAM controller logic, and to part of U343 (Figure 9.7), the horizontal sync timing flip-flop.

U332 is the RAM controller logic IC. The logic which dictates its operation is detailed in the PAL equations of Chapter 7. The XCLK signal on pin 12 of this device is derived from either the system 14.3 MHz OSC signal or 7.15 MHz, depending on whether HRES (high resolution) is high or low. Two sections of U307, exclusive ORs, then use the XCLK signal to clock the two timing flip-flops, U335 and U334.

DCLK, the dot clock signal, is the output of an exclusive OR segment of U307, derived from the DOTS signal from U332.

RASCC*, RASAT*, and CAS* are used to select the memory row and column of the video RAM character and attribute banks. ADMUX enables the RAM address multiplexers.

U335 and U334 are two quad D-type flip-flops wired as a multiple counter to provide the video clock timing pulses, Q0, Q1*, Q2*, Q3P*, Q0P*, and Q3P.

Part of U302, U331, U330, and parts of U313 and U323 form the decision circuitry for CPU/CRT controller video memory access. VMEMSEL*, the video memory select signal, after inversion by U302, is applied to the D input of U331, the CLR input of U330, and one input of NAND gate U323. As long as CPUAXS is active-high, U330 Q* is low, and RDY is high. When BMW* goes active-low, and if U331, pin 6, Q* is low, WVRAM* goes active-low to enable data to enter video RAM.

VMEMSEL*, BMR*, and BA0 together arbitrate between a character or attribute memory read operation, with BA0 used to determine which bank to access. If BA0 is high, the attribute code is read; if low, the character code is fetched.

Refer to Figure 9.7, which shows the horizontal and vertical sync and timing, cursor and display enable, and the dot synchronization and blink control circuits.

U326 is a PAL chip programmed as a video synchronizer. The logic equations which dictate its operation are detailed in Chapter 7. Upon receipt of the proper input signals, U326 generates text dots (A/N DOTS), display enable delayed (DISPENDLY*, C1 DLY, and C0 DLY) for use by the B/I dots color encoder, U325, and the R/G dots color encoder, U324, on Figure 9.9.

U343 is the horizontal sync and timing circuit. It is a binary counter configured to divide the 7.15 MHz signal by 32 to create a 4.76 μsec horizontal sync pulse width. U321 acts as the horizontal start/stop control. Horizontal trace starts when U321 is clocked active and stops when HSYNC goes low to clear the flip-flop. The resulting output is applied to the D4 input of U333, and the Q4 output eventually becomes the delayed horizontal sync signal for the RGB monitor output.

VSYNC is applied to the D5 input of U333, to emerge from Q5 as the vertical (V) timing signal for the color encoders, and as one of the clock signals for the character and cursor blink generator, U322.

CURSOR is inverted and applied to the D0 input of U333. Q0 is fed back to the D1 input and the resultant cursor output from Q1 is delayed by two character clocks. Cursor output from Q1 is applied to pin 2 of U326 as the CDLY* (cursor delayed) signal.

Display enable (DISPEN) is inverted by U302 and applied to pin 6, the D2 input of U333, and also goes to U351, the status register, as the DISPLAY* signal. The Q2 output of U333 is used as one possible signal source for the CLR S/R* signal, and also is fed back to U333, D3. The Q3 output emerges as the display enable delayed (DDLY*) signal, and is supplied to the dot synchronizer and blink controller from which it emerges as DISPENDLY* for use by the color encoders.

If neither VIDEO EN, nor VIDEO ON is active, the CLR S/R* signal also is issued.

VIDEO ON, VIDEO EN, and COMP SYNC are NORed together to create the BLANK* signal for the color encoding circuitry.

U322 uses the V output of U333 to create the cursor BLINK* and the character CBLINK* signals, and is configured to blink the cursor approximately two times faster than characters.

Other inputs to the sync decoder are GATE*, derived from the HI-A signal, DCLK, CDOTS, EBLINK, ATBLINK, Φ 1, 640 $\times$ 200, C0, and C1.

Memory and I/O Decoders

Figure 9.8 shows the circuitry for the video RAM and I/O port address decoders.

U362 is a PROM device programmed to act as a memory address decoder. It uses BA15, BA16, BA17, BA18, BA19, and BA14 buffered address lines, and the negative-ORed BMR* and BMW* signal lines to make its selections. When signal conditions are correct, O3 emerges as the video memory select (VMEMSEL*) signal, and O4 becomes XRAM, scratchpad RAM select.

The read or write decision is made by U321, using system CLK, HI-B, and BIOW* as inputs. The R/W* signal produced is the CRT controller read/write timing signal.

The CRT controller enabling clock (ECLK) signal is produced by U344 based on the input states of CLK, HI-B, BIOW*, and BIOR*. BIOW* and BIOR* are negative-ORed and inverted before application to the CLR and D inputs of the flip-flop. The ORed output, before inversion, becomes the data buffer enable signal, IOAXS* (I/O access), for U303 on Figure 9.1, and also is used as a gate-enable input signal by I/O decoder U329.

Part of U301, U317, and U329 comprise the video I/O port address decoders. BA9 and BA8 are ANDed to become the gate 1, G1, signal for U317. BA5 is G2B and AEN is G2A. BA4, BA6, and BA7 are the actual address selection lines, A, B, and C, for U317. When the status of these signals indicates a valid video I/O port address, the Y7 output becomes the G2B enable for U329. U329 then uses BA0, BA1, BA2, and BA3 to determine the actual video port address. Y7 of U317 also is the SEL3DX* signal used by the CRT controller and bidirectional data bus for I/O read/write decisions.

U330 and two U304 inverters form the interface for an optional light pen. P302, a 6-pin terminal strip, supplies +5 VDC, +12 VDC, and ground to the device. The light pen switch connects to pin 3 to become the LPSW* signal.

The light pen output connects to pin 9 of the strip, is inverted, applied to pin 3 of J302 (the light pen polarity select jumper), is inverted again, and routed to pin 1. In this manner, when a female jumper connector is placed between pins 2 and 3, or between pins 2 and 1, either a negative- or a positive-going light pen pulse is seen by the CLK line of flip-flop U330.

A decoupled +5 VDC signal (HI-B) always is present on the D input, so that as long as valid video addresses cause U329 to prevent lows on the CLR and PR inputs, a pulse from a light pen will clock the flip-flop and generate the LPEN signal for use by the status register and the CRT controller.

Color Video Encoder and Synchronization

Figure 9.9 details the color encoder and video sync generator.

U324 and U325, two PAL devices, generate the encoded color signal before application to the video timing and output circuits. The functional equations for these devices are detailed in Chapter 7. U324 encodes the red and green signals, and U325 the blue and intensity bits.

C0 DLY, C1 DLY, DISPEN DLY*, GRPH, A/N DOTS, BLANK*, and 640 × 200 are common inputs to both devices.

Attribute bits AT1, AT2, AT5, and AT6, and the OVERSCAN R and OVERSCAN G signals, determine whether the R (red) or G (green) signals, or both, are output to U338 from the R/G encoder.

Attribute bits AT0, AT3, AT4, and AT7, and the OVERSCAN B and OVERSCAN I signals, determine whether the B (blue) and I (intensity) signals from the B/I encoder are used. The I bit also is dependent on the ON or OFF states of the BGNDI and ENABLINK signals, and the B bit also is dependent on the SELBLUE signal derived from COLORSEL and BW signals.

U338 is responsible for the synchronization of the dot stream to be sent to the video output circuit via the video multiplexer, U319.

The U319 video multiplexer provides the capability of selecting an optional video card. The optional signals R, G, B, H, and V are entered onto the card through connector P303. The U319 is a hex 2-to-1 universal multiplexer which outputs these signals to the video output circuit.

Video Output

Refer to Figure 9.10 for the description of the video output circuits.

HSYNC DLY and VSYNC DLY are XORed by U339 with HI-B or GND, depending on how J303, J304, J306, J307, and J308 are configured. The XORed signals and RDOTS, GDOTS, BDOTS, and IDOTS are applied to "D" connector P305 which connects to the direct drive color monitor. The dot signals also are routed to the inputs of U318, an open-collector buffer.

VSYNC DLY is exclusive ORed with the internal vertical sync selection jumper, J306. The XORed output of U339 is buffered by part of U318 and connected to pin 6 of P302 for use by an internal display monitor.

HSYNC DLY also is buffered and connects to pin 5 of P302. HSDLY and the HSYNC polarity select jumper, J307, are exclusive ORed and, after inversion and filtering, applied to pin 8 of the RGB video output connector, P304.

J304, the composite/vertical sync selector jumper, and J308, the vertical sync polarity select jumper, are exclusive ORed, inverted, filtered, and connected to pin 9 of P304.

When the dots signals leave U340, they are filtered and placed on pins 3 through 6 of the RGB output connector, P304, for use by the attached RGB monitor.

U318, R302, and RP303 form a digital-to-analog (D/A) converter, changing the color information into voltage levels for use in creating gray scales. These signals are fed into Q303 which then feeds Q304 (drives an internal monitor from P302, pin 10), and Q305 (drives an external monochrome monitor from J309).

Chapter 5

Troubleshooting

General

Use of the information in this chapter assumes that one or more malfunctions have been traced to the Z-309A Video Card, and the power-on, menu-selected, and disk-based diagnostics have not isolated the problem. The information provided here will supplement the procedures provided by the built-in debugging routines of system ROM. Refer to the troubleshooting chapter in the *Base Units Service Modules* for details on the use of these routines.

In the following descriptions, all address and register values are given in hexadecimal notation. The term "set" in a given bit position indicates a logic one (1) state. The term "reset" indicates a logic zero (0).

The memory required by the video interface is a self-contained 16K-byte bank with no parity bit. It is used in text mode for storage and retrieval of character and attribute information. In graphics mode, it contains data to define color attributes of the graphics pixels. The buffer address starts at B8000.

CRT Controller

The following paragraphs define the functions and interrelationships of the signals appearing on the pins of the 6845. For more detailed information, refer to the 6845 CRT Controller data sheets in Chapter 8.

The signals fall into three categories: signals which interface the controller with the microprocessor and system busses; signals which interface the controller with the video memory bank and character generator logic; and signals which directly relate to controller/monitor interfacing.

Microprocessor Interface Signals

Table 5.1 defines the signals used to provide communication and data transfer between the video card and the rest of the system.

Table 5.1. Video Card to System Interface Signals

SIGNAL	FUNCTION
D0 to D7	Bidirectional data lines which transfer information between the CPU and the internal registers of the 6845.
CS*	Chip select signal typically generated by system address decoding logic. CS* must be low to read information from, or write information to, one of the 6845 internal registers.
RS	6845 register select signal. Rather than sacrifice five of the 40 available pins to 6845 register-addressing, one of the registers is used as an address register to access the other 18 registers. When the RS signal is low, the address register is accessed and can then be loaded with the address of the internal register to be accessed next. When RS is high, the addressed register may be accessed.
R/W*	The read/write signal. It determines whether data is to be written into or read from an internal register. R/W* is low for a write operation, high for a read operation.
E	The enabling (synchronizing clock) signal required by the 6845 which enables the internal I/O buffers and clocks data into and out of the internal registers via the data buffers. In this computer, the E input connects to the system ECLK signal.
CLK	Synchronizes the 6845's control signals. It is derived from the system clock to become the character rate clock in text mode. Although this signal is more closely related to the character generator and video interface, it is included here because it is the primary timing unit to the 6845.
RESET*	Initializes the 6845. When this pin goes low, the internal counters are cleared and the 6845 outputs go low, effectively stopping the video display operation. As the RESET* signal does not affect the program-accessible counters within the 6845, display may continue when RESET* goes high.
V_{cc} (+5V) and V_{ss} (Ground)	Standard TTL power levels which enable proper operation of the video card ICs.

Screen Memory and Character Generator Signals

There are two sets of signals provided by the 6845 to implement screen memory and character generator logic interface. MA0 through MA13 are screen memory address outputs, and RA0 through RA4 are the raster address signals to character generator logic. The 14 screen memory address lines allow the 6845 to address the 16 K-bytes of video memory. The raster address lines are outputs from the 6845's scan line counter required by the character generator logic to determine which scan line of a character row is in progress.

CRT Monitor Signals

HSYNC and VSYNC are standard horizontal and vertical synchronization signals required by the CRT monitor for display stabilization. DISPEN is the display enable signal which goes high whenever the video signal to the CRT is to be active. DISPEN is low during horizontal and vertical retrace, and also could be called the video blanking signal. CURSOR is the cursor enable signal which allows a steady stream of dots to be produced on the CRT screen as a cursor symbol.

LPEN is the light pen strobe input signal which may be used to interface a light pen. A high on the LPEN line signals the 6845 to save the contents of the screen memory address in one of the internal register sets so the microprocessor can subsequently determine the position on the monitor screen at which the light pen was detected.

CRT Controller Register

The 19 internal registers of the 6845 CRT controller can be software-programmed to define display and control parameters of a raster-scanned monitor. One of these registers, the address register, is used only as a pointer to the addresses of the other 18 registers. The address register is write-only and is loaded from the CPU, using an I/O OUT instruction to I/O address 3D4. This register is loaded with the five least-significant bits of the I/O argument.

The other 18 registers are selected by the pointer information in the address register, then the CPU directs the information at address 3D5 to be loaded into the selected register. Transfers of address and parameter information to and from the registers is via data lines D0 through D7.

Programming the Registers

Table 1 in the data sheets illustrates the logic involved in accessing the 6845 internal registers. Table 5.2 in this chapter defines the individual registers in terms of values contained in them and the results obtained with these values. All values are expressed in hexadecimal.

Table 5.2. CRT Controller Register Functions

REG. ADDR.	REG. NO.	REG. TYPE	UNITS	REG. STAT.	VALUES 40 × 25 TEXT	80 × 25 TEXT	GRAPHICS MODE
0	R0	Horiz. Total	Char.	Write	38	71	38
1	R1	Horiz. Dispd.	Char.	Write	28	50	28
2	R2	Horiz. Sync. Position	Char.	Write	2D	5A	2D
3	R3	Horiz. Sync.	Char.	Write	0A	0A	0A
4	R4	Vert. Total	Row	Write	1F	1F	7F
5	R5	Vert. Total Adjust	Scan Line	Write	06	06	06
6	R6	Vert. Dispd.	Row	Write	19	19	64
7	R7	Vert. Sync. Position	Row	Write	1C	1C	70
8	R8	Interlace Mode	–	Write	02	02	02
9	R9	Max. Scan Line Addr.	Scan Line	Write	07	07	01
A	R10	Cursor Start	Scan Line	Write	06	06	06
B	R11	Cursor End	Scan Line	Write	07	07	07
C	R12	Start Addr.	High	Write	00	00	00
D	R13	Start Addr.	Low	Write	00	00	00
E	R14	Cursor Addr.	High	Read/ Write	XX	XX	XX
F	R15	Cursor Addr.	Low	Read/ Write	XX	XX	XX
10	R16	Light Pen	High	Read	XX	XX	XX
11	R17	Light Pen	Low	Read	XX	XX	XX

The first group of registers, R0 through R3, establishes the horizontal format and timing parameters. Registers R4 through R9 determine vertical format and timing parameters. The remaining registers, R10 through R17, deal with cursor characteristics, screen memory addressing, and the light pen interface. Typically, registers R0 through R11 are loaded when the system is turned on and should not need to be accessed thereafter. The other six registers, R12 through R17, need to be accessed on an ongoing basis during display operations. R12 and R13 establish the 14-bit starting (top-of-page) address of screen memory. The contents of these registers may be manipulated to perform scrolling of the screen contents. R14 and R15 establish the 14-bit cursor address which establishes the cursor symbol position on the screen. R16 and R17 are used only if a light pen is interfaced.

Horizontal Timing and Format Registers

The contents of register R0 determines the total time allotted for one scan line in terms of character clock (CLK) cycles (total of displayed and undisplayed characters minus 1) per horizontal line, thus determining the horizontal sync (HSYNC) frequency.

R1 is the character row register. It is loaded with the total number of characters minus 1 in character clock (CLK) units.

The horizontal sync register, R2, establishes the point at which the HSYNC signal makes its negative-to-positive transition, specified in terms of CLKs. The reference point for the beginning of the HSYNC pulse is the left-most character position displayed on the scan line.

R3, the HSYNC width register, uses only the four least-significant bits of data to establish the duration of the HSYNC pulse in the range of 1 to 16 character clocks. This allows you to adjust the HSYNC pulse duration to the requirements of the applicable CRT monitor.

Figure 5.1 shows the interrelationship between the four horizontal timing and format registers (R0 through R3) in terms of CLK.

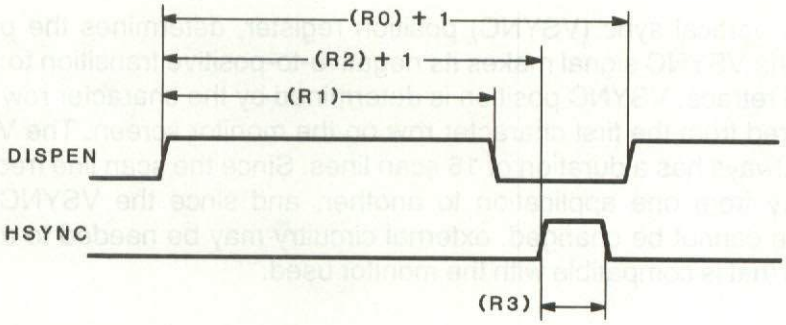


Figure 5.1. Horizontal Timing and Format

Vertical Timing and Format Registers

Registers R4 through R9 normally are loaded at system startup and normally are not changed thereafter. The point of reference for these registers is the top-most character position displayed on the monitor screen.

The vertical total register, R4, and the vertical sync adjust register determine the total number of scan line times in a frame, including vertical retrace, establishing the overall frame rate or VSYNC frequency.

R4 is a 7-bit register loaded with the total number of character rows. Since a character row can consist of up to 32 scan lines, it may be difficult for you to establish a refresh frequency close to the line frequency. Register R5, a 5-bit VSYNC adjust register, may then be used to fine-tune the VSYNC frequency. R5 is loaded with a value representing scan line times.

The character-rows-displayed register, R6, is a 7-bit register which allows you to select the number of rows of characters to be displayed, up to 128. What you specify for this register does not determine the positions of the VSYNC pulse, but the point at which display enable (DISPEN) will be reset for vertical retrace.

R7, the vertical sync (VSYNC) position register, determines the point at which the VSYNC signal makes its negative-to-positive transition to initiate vertical retrace. VSYNC position is determined by the character row times, measured from the first character row on the monitor screen. The VSYNC pulse always has a duration of 16 scan lines. Since the scan line frequency will vary from one application to another, and since the VSYNC pulse duration cannot be changed, external circuitry may be needed to achieve a pulse that is compatible with the monitor used.

The interlace mode register, R8, determines whether interlaced or non-interlaced scan is used.

The value in register R9 determines the number of scan lines per character row. This 5-bit register may be programmed for a character row of up to 32 scan lines. The value used will dictate the maximum count output by the raster address signals (RA0 through RA4) to the character generator logic. Load R9 with the desired scan line count minus 1.

The cursor formatting registers are comprised of the cursor start and cursor stop registers, R10 and R11, respectively. The five least-significant bits of each register determine the scan lines within a character row where the cursor symbol is to be activated. The scan line specified in R10 is the first scan in which the CURSOR signal is to be set and it will remain set until the scan line specified in R11 has been completed. Accordingly, if the cursor symbol is to occupy a single scan line, the same value must be loaded into both registers. If different values are loaded, a block-type cursor will be formed. In interlaced sync and video mode, both registers must be loaded with either odd or even values. Bits 5 and 6 determine whether or not the cursor is to blink, and if so, at either 1/16th or 1/32th of the field rate. See the data sheets in Chapter 8 for clarification of cursor format programming.

Primary Operating Registers

The remaining six registers, R12 through R17, are considered the primary operating registers since, in the course of display programming, the contents will undoubtedly change on an ongoing basis rather than being loaded one-shot at system startup. The six registers are arranged as three 14-bit register pairs (bits 6 and 7 of the most-significant byte are not used).

R12 and R13 comprise the top-of-page register which specifies the screen memory address containing the first character from the top-left corner to be displayed. At the end of each vertical retrace, the first screen memory address generated will be the one contained in these registers. Since the 6845 addresses memory linearly, rather than on a row/column basis, scrolling can be performed on either a character-by-character or row-by-row basis.

The cursor position registers, R14 and R15, generate a cursor signal when the 6845 generates a screen memory address on MA0 through MA13 that matches the contents of this register pair, and when the scan line counter (RA0 through RA4) outputs fall within the limits established by registers R10 and R11. It may be necessary to delay the cursor signal with external logic circuitry to achieve display at the desired position. Cursor movement on the screen is accomplished by loading new values into R14 and R15. These registers are the 6845's only read/write registers so they also can be used to keep track of the cursor position, rather than copying this information from another memory location.

R16 and R17 are the light pen register pair, which will be loaded with the screen memory address corresponding to the screen position at which the LPEN signal was detected. Since there are several critical timing parameters involved with this signal, be sure to carefully study the documentation supplied with this option.

Raster Scan Signals

The raster scan outputs, RA0 through RA4, provide the interface between the 6845 and the character generator logic. These outputs may represent scan line counts of from 0 to 31, or up to 32 scan lines per character row. Register R9, the scan lines/row register, determines the maximum count from the scan output registers before reset occurs. Scan line counts are incremented at the HSYNC rate, but also are dependent on the interlace format selected.

Video Card I/O Devices

Table 5.3 defines the I/O devices contained on the video interface.

Table 5.3. Video Card I/O Port Assignments

PORT ADDRESS	REGISTER
3D0	6845
3D1	6845
3D8	Mode Control
3D9	Color Select
3DA	Status/Mode I/O
3DB	Light Pen Latch CLEAR
3DC	Light Pen Latch PRESET

To address a given port, the address lines are programmed as defined in Table 5.4.

Table 5.4. Video Card I/O Port Selection

PORT	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
3D0	1	1	1	1	0	1	1	X	X	0
3D1	1	1	1	1	0	1	1	X	X	1
3D8	1	1	1	1	0	1	1	0	0	0
3D9	1	1	1	1	0	1	1	0	0	1
3DA	1	1	1	1	0	1	1	0	1	0
3DB	1	1	1	1	0	1	1	0	1	1
3DC	1	1	1	1	0	1	1	1	0	0

X = Don't care

The 6845 CRT controller occupies two I/O port addresses. The RS (register select) line is connected to the least-significant bit, A0. When A0 is reset, the address register is accessed to load it with the register address of the desired parameter, which would then be accessed by setting A0 (RS). A typical register access operation then would consist of two consecutive device write cycles, or a write cycle followed by a read cycle, and these cycles would be directed to consecutive memory or I/O locations.

Color Select Register

The color select register, located at address 3D9, is a 6-bit output-only device (it cannot be read) which can be written to using the I/O OUT command. Only the six least-significant bits of the instruction are used, as shown in Table 5.5.

Table 5.5. Color Select Register Logic

Bit 0	B (blue) border color select (text mode) or 640 × 200 graphics dot color
Bit 1	G (green) border color select (text mode) or 640 × 200 graphics dot color
Bit 2	R (red) border color select (text mode) or 640 × 200 graphics dot color
Bit 3	I (intensity) intensifies border color (text mode) or 640 × 200 graphics dot color
Bit 4	Selects alternate background color palette for text mode color
Bit 5	320 × 200, graphics color palette selection

Bits 6 and 7 are not used.

In text mode, bits 0, 1, 2, and 3 determine the screen border color. In 320 × 200 graphics submode, these bits select the screen background color (C0 and C1).

Bit 4, when set, selects an alternate, intensified palette of background colors in text mode if bit 5 in the mode select register, I/O port 3D8, is reset.

Bit 5 is used only in the 320 × 200 graphics submode to select the active palette of screen display colors. If bit 5 is a logical 1, color is determined by the logic of Table 5.6.

Table 5.6. Palette Number 1 Selection

C1	C0	BACKGROUND COLOR
0	0	Defined by bits 0-3 of I/O port 3D9
0	1	Cyan
1	0	Magenta
1	1	White

If bit 5 is a logical 0, color is determined by the logic of Table 5.7.

Table 5.7. Palette Number 2 Selection

C1	C0	BACKGROUND COLOR
0	0	Defined by bits 0-3 of I/O port 3D9
0	1	Green
1	0	Red
1	1	Yellow

Mode Select Registers

The mode select registers are also write-only registers. One is a 6-bit register at port address 3D8; the other is an 8-bit register at 3DA. Both can be written to using I/O OUT commands. The output register at 3D8 functions according to the logic of Table 5.8.

Table 5.8. Mode-Select Port 3D8 Logic

Bit 0	A logical 1 selects 80 × 25 text submode. A logical 0 selects 40 × 25 submode.
Bit 1	A logical 1 selects 320 × 200 graphics submode. A logical 0 selects text mode.
Bit 2	A logical 1 selects monochrome submode. A logical 0 selects color submode.
Bit 3	Disables the video signal during mode changes. The video signal should be re-enabled following a mode change. A logical 1 enables the video.
Bit 4	A logical 1 selects 640 × 200 monochrome graphics submode. Use I/O port 3D9 to select one of eight colors when using a direct drive monitor in this submode.
Bit 5	A logical 1 selects blinking feature in alphanumeric mode (normal setting). A logical 0 intensifies whichever of the 16 background colors is selected to yield a lighter shade of that color.

Bits 6 and 7 are not used.

The register at 3DA functions according to the logic of Table 5. 9.

Table 5.9. Mode-Select Port 3DA Logic

Bit 0	A logical 1 overrides the VIDEO ENABLE signal from 3D8; will eliminate monitor display flicker when in text mode.
Bit 1	Character font selection. A logical 1 selects the single-dot width font if jumper J302 on the video card is positioned to "0", and the double-dot width font if J302 is positioned to "1". A logical 0 reverses this condition. The purpose for allowing this either/or situation is to enable your selection of either font at power on.
Bit 2	A logical 1 will underline any character which has a logic one in bit 6 (RED background) of the attribute byte.
Bit 3	Reserved for video diagnostics; used to light the LED located on the video card.
Bit 4	A logical 1 disables the color video interface and connects video output from an alternate video card located within your central computing unit to output connectors on the resident video card.
Bit 5	A logical 1 enables fast hardware scrolling in the 80 × 25 submode only.
Bits 6 and 7	Used to select one of four pages of display text from the 16K video RAM according to the following logic:

BIT 7	BIT 6	SCREEN PAGE SELECT
0	0	First page
0	1	Second page
1	0	Third page
1	1	Fourth page

Status Register

The status register, an 8-bit read-only buffer, resides at input port address 3DA. Table 5.10 summarizes the logical operation of this register.

Table 5.10. Status Select Logic

Bit 0	A logical 1 indicates that a horizontal or vertical retrace is in progress. This bit can be used to update the video memory during screen refresh intervals.
Bit 1	A logical 1 in this bit position indicates that a positive-going light pen signal has set the light pen trigger. This trigger is reset at power up and also may be cleared by issuing an I/O OUT command to port address 3DB. The reset is address-activated; no specific data need be output.
Bit 2	A logical 0 indicates that the light pen switch is on. The switch signal is not latched or debounced.
Bit 3	A logical 1 indicates that a vertical retrace is in progress.
Bit 4	Least-significant bit (LSB) of the character font number.
Bit 5	Most-significant bit (MSB) of the character font number.

Bits 6 and 7 are not used.

Programming Sequence

In general, observe the following sequence when selecting operating parameters for the video interface:

1. Determine desired mode of operation: text mode or all-points-addressable graphics.
2. Reset video enable bit. Also reset video override bit 0 in port address 3DA if not already reset.
3. Program the CRT controller to desired mode.
4. Determine desired submode(s), then program mode and color select registers.
5. Set video enable bit. Also set the video override bit, if desired.

Video Output Adjustment

The following paragraphs detail the procedure for setting the video output black level and contrast.

Connect the oscilloscope vertical input to the monochrome video output connector, J308. Connect oscilloscope external sync input to pin 5 of P301, HSDLY. Obtain a stable waveform resembling Figure 5.2.

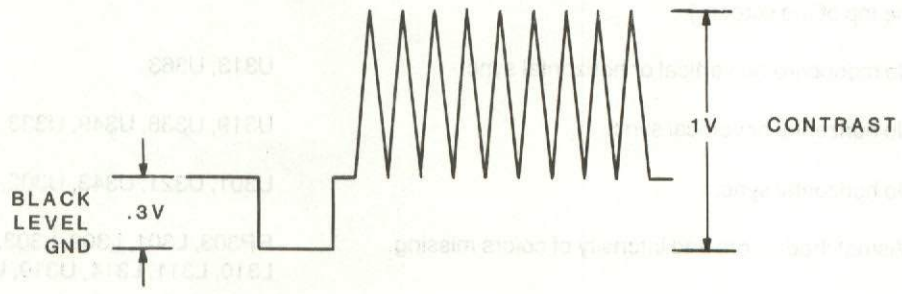


Figure 5.2. Video Output Adjustment Waveform

Adjust black level control, R310, for a pulse height of .3 volt. Then adjust the contrast control, R311, for a peak waveform height of 1 volt. The adjustments may be slightly interactive, so repeat these two operations as necessary to obtain the specified results.

Troubleshooting Table

NOTE: Use of the Disk-Based Diagnostics package, if available, is recommended for troubleshooting.

Table 5.11 lists some problems that may be encountered and some possible causes.

Table 5.11. Troubleshooting Chart

PROBLEM	POSSIBLE CAUSE
System dies when card inserted.	U330, U331, U351, U359, U360, U340, U358
No video dots.	Q303, U319, U338, U324, U325, U326, U305, U306, U311, U312, U308
Horizontal sync problems. (Starting characters off the left of screen, or first line does not start on the left side of the screen.)	U318, U303, U363
Vertical sync problems. (Rolling or starting point off the top of the screen.)	J306, U318, U339, J308, U369
No monochrome vertical or horizontal sync.	U313, U363
No horizontal or vertical sync.	U319, U338, U349, U333, U337
No horizontal sync.	U301, U321, U343, U302, U337
Mismatched colors and intensity of colors missing.	RP303, L301, L302, L303, L304, RP302, U318, U340, L310, L311, L314, U319, U338, U324, U325
Background colors bad.	U324, U325, U327, U352, U309, U314, U350
No RAM data output.	U332, U334, U335, U307, U362, U359, U360, U361, U308, U309, U312, U314

Chapter 6

309A Video Card Component Parts List

Introduction

This portion of the service module contains a component view of the Z-309A Video Card (part numbers HE 181-4937, HE 181-5084, and HE 181-5427) and related parts list. Refer to Figure 6.1 for location of parts and components.

CAUTION: This card contains electrostatic-sensitive devices (ESD). Exercise extreme care when handling these devices to prevent damage.

Refer to Chapter 7, "Semiconductor Identification," or to the data sheets in Chapter 8 for descriptions of semiconductor devices.

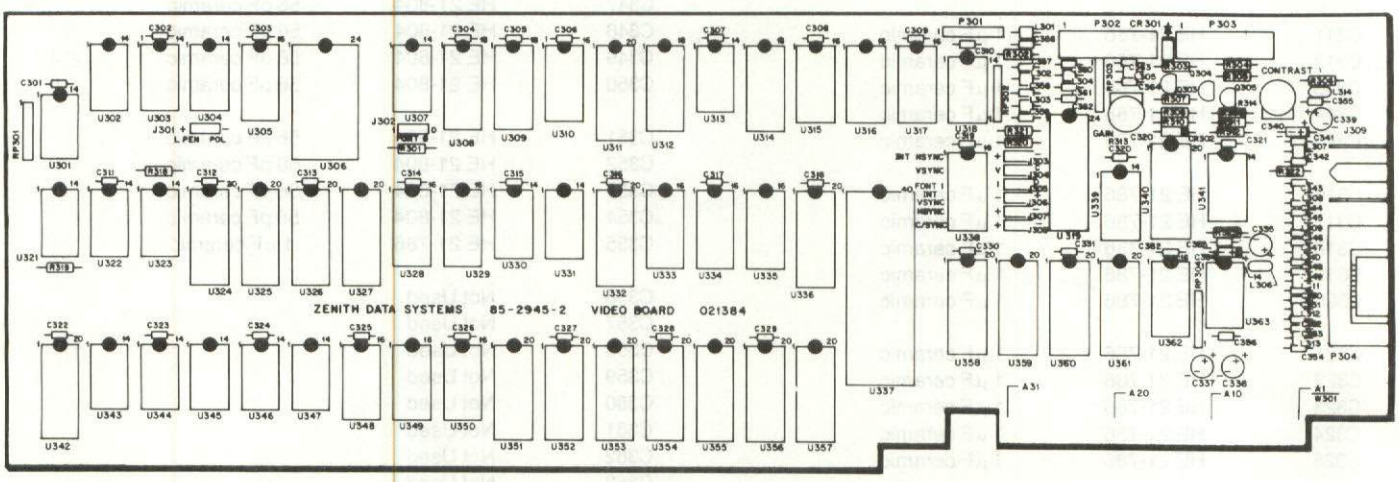


Figure 6.1. Video Card Component Layout

Parts List

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
Capacitors		
C301	HE 21-786	.1 μF ceramic
C302	HE 21-786	.1 μF ceramic
C303	HE 21-786	.1 μF ceramic
C304	HE 21-786	.1 μF ceramic
C305	HE 21-786	.1 μF ceramic
C306	HE 21-786	.1 μF ceramic
C307	HE 21-786	.1 μF ceramic
C308	HE 21-786	.1 μF ceramic
C309	HE 21-786	.1 μF ceramic
C310	Not Used	
C311	HE 21-786	.1 μF ceramic
C312	HE 21-786	.1 μF ceramic
C313	HE 21-786	.1 μF ceramic
C314	HE 21-786	.1 μF ceramic
C315	HE 21-786	.1 μF ceramic
C316	HE 21-786	.1 μF ceramic
C317	HE 21-786	.1 μF ceramic
C318	HE 21-786	.1 μF ceramic
C319	HE 21-786	.1 μF ceramic
C320	HE 21-786	.1 μF ceramic
C321	HE 21-786	.1 μF ceramic
C322	HE 21-786	.1 μF ceramic
C323	HE 21-786	.1 μF ceramic
C324	HE 21-786	.1 μF ceramic
C325	HE 21-786	.1 μF ceramic
C326	HE 21-786	.1 μF ceramic
C327	HE 21-786	.1 μF ceramic
C328	HE 21-786	.1 μF ceramic
C329	HE 21-786	.1 μF ceramic
C330	HE 21-786	.1 μF ceramic
C331	HE 21-786	.1 μF ceramic
C332	HE 21-786	.1 μF ceramic
C333	HE 21-786	.1 μF ceramic
C334	HE 21-197	1 μF tantalum
C335	HE 25-820	10 μF electrolytic
C336	HE 21-786	.1 μF ceramic
C337	HE 25-820	10 μF electrolytic
C338	HE 25-820	10 μF electrolytic
C339	HE 25-820	10 μF electrolytic
C340	HE 21-197	1 μF tantalum
C341	HE 21-804	56 pF ceramic
C342	HE 21-804	56 pF ceramic
C343	HE 21-804	56 pF ceramic
C344	HE 21-804	56 pF ceramic
C345	HE 21-804	56 pF ceramic
C346	HE 21-804	56 pF ceramic
C347	HE 21-804	56 pF ceramic
C348	HE 21-804	56 pF ceramic
C349	HE 21-804	56 pF ceramic
C350	HE 21-804	56 pF ceramic
C351	HE 21-804	56 pF ceramic
C352	HE 21-804	56 pF ceramic
C353	HE 21-804	56 pF ceramic
C354	HE 21-804	56 pF ceramic
C355	HE 21-786	.1 μF ceramic
C356	Not Used	
C357	Not Used	
C358	Not Used	
C359	Not Used	
C360	Not Used	
C361	Not Used	
C362	Not Used	
C363	Not Used	
C364	Not Used	
Diodes		
CR301	HE 56-24	LED, red
CR302	HE 56-655	

Parts List

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
Chokes and Pins		
L301	Bare Wire	
L302	Bare Wire	
L303	Bare Wire	
L304	Bare Wire	
L305	Bare Wire	
L306	HE 235-229	Choke, RF, ferrite, 35 μH
L307	HE 45-73	Choke, ferrite, 2.2 μH
L308	HE 45-73	Choke, ferrite, 2.2 μH
L309	HE 45-73	Choke, ferrite, 2.2 μH
L310	HE 45-73	Choke, ferrite, 2.2 μH
L311	HE 45-73	Choke, ferrite, 2.2 μH
L312	HE 45-73	Choke, ferrite, 2.2 μH
L313	HE 45-73	Choke, ferrite, 2.2 μH
L314	HE 235-229	Choke, RF, ferrite, 35 μH
Integrated Circuits		
U301	HE 443-816	AND, quad
	or	
	HE 443-1229	
	HE 434-298	Socket
U302	HE 443-755	Inverter, hex
	or	
	HE 443-1082	
	HE 434-298	Socket
U303	HE 443-875	OR, quad
	or	
	HE 443-1072	
	HE 434-298	Socket
U304	HE 443-755	Inverter, hex
	or	
	HE 443-1082	
	HE 434-298	Socket
U305	HE 443-892	Register
	HE 434-299	Socket
U306	HE 444-292	Character ROM
	or	
	HE 444-230-1	
	or	
	HE 444-230-2	
	HE 434-307	Socket
U307	HE 443-915	XOR, quad
	HE 434-298	Socket
U308	HE 443-1165	RAM, dynamic, 16 K × 4
	HE 434-310	Socket
U309	HE 443-1165	RAM, dynamic, 16 K × 4
	HE 434-310	Socket
U310	HE 443-1037	Selector, quad, 2-to-1
	HE 434-299	Socket
U311	HE 443-1031	Flip-flop, octal, D
	HE 434-311	Socket
U312	HE 443-1165	RAM, dynamic, 16 K × 4
	HE 434-310	Socket
U313	HE 443-875	OR, quad
	or	
	HE 443-1072	
	HE 434-298	Socket
U314	HE 443-1165	RAM, dynamic, 16 K × 4
	HE 434-310	Socket
U315	HE 443-1037	Selector, quad, 2-to-1
	HE 434-299	Socket
U316	HE 443-1037	Selector, quad, 2-to-1
	HE 434-299	Socket
U317	HE 443-877	Decoder
	HE 434-299	Socket
U318	HE 443-1020	Buffer interface gate
	HE 434-299	Socket
U319	HE 443-805	Flip-flop, octal, D
	or	
	HE 443-1198	Hex 2-to-1 universal multiplexer
	HE 434-311	Socket
U320	Not Used	
U321	HE 443-1051	Flip-flop, octal, D
	HE 434-298	Socket
U322	HE 443-973	Counter, binary
	HE 434-298	Socket
U323	HE 443-1034	Buffer, quad, NAND
	or	
	HE 443-1232	
	HE 434-298	Socket
U324	HE 444-274	Generator, dot, R/G
	HE 434-311	Socket
U325	HE 444-234	Generator, dot, B/I
	HE 434-311	Socket
U326	HE 444-232	Video sync
	HE 434-311	Socket
U327	HE 443-1031	Flip-flop, octal, D
	HE 434-311	Socket
U328	HE 443-892	Register
	HE 434-299	Socket

Parts List

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
Integrated Circuits (continued)		
U329	HE 443-877	Decoder
	HE 434-299	Socket
U330	HE 443-1051	Flip-flop, octal, D
	HE 434-298	Socket
U331	HE 443-1051	Flip-flop, octal, D
	HE 434-298	Socket
U332	HE 444-235	PAL, RAM control
	HE 434-311	Socket
U333	HE 443-879	Flip-flop, hex, D
	HE 434-299	Socket
U334	HE 443-983	Flip-flop, quad, D
	HE 434-299	Socket
U335	HE 443-983	Flip-flop, quad, D
	HE 434-299	Socket
U336	HE 444-235	Multiplexer, scroll
	HE 434-311	Socket
U337	HE 443-906	Controller, CRT
	HE 434-253	Socket
U338	HE 443-1053	Flip-flop, hex, D
	HE 434-299	Socket
U339	HE 443-891	XOR, quad, 2-input, 8-bit
	HE 434-298	Socket
U340	HE 443-1058	Buffer, octal
	HE 434-311	Socket
U341	HE 443-967	Inverter, hex
	or	
	HE 443-1072	
	HE 434-298	Socket
U342	Not Used	
U343	HE 443-973	Counter, binary
	HE 434-298	Socket
U344	HE 443-1051	Flip-flop, octal, D
	HE 434-298	Socket
U345	HE 443-875	OR, quad
	HE 434-298	Socket
U346	HE 443-779	NOR, quad, 2-input
	or	
	HE 443-1045	
	HE 434-298	Socket
U347	HE 443-780	AND, quad, 2-input
	or	
	HE 443-1073	
	HE 434-298	Socket
U348	HE 443-892	Register
	HE 434-299	Socket
U349	HE 443-1166	Flip-flop, hex, D
	HE 434-299	Socket
U350	HE 443-1166	Flip-flop, hex, D
	HE 434-299	Socket
U351	HE 443-1058	Buffer, octal
	HE 434-311	Socket
U352	HE 443-1031	Flip-flop, octal, D
	HE 434-311	Socket
U353	HE 443-1058	Buffer, octal
	HE 434-311	Socket
U354	HE 443-1058	Buffer, octal
	HE 434-311	Socket
U355	HE 443-1070	Transport latch, octal, D
	HE 434-311	Socket
U356	HE 443-1070	Transport latch, octal, D
	HE 434-311	Socket
U357	HE 443-1098	Flip-flop, octal, tri-state
	HE 434-311	Socket
U358	HE 443-1097	Transceiver, octal, tri-state
	HE 434-311	Socket
U359	HE 443-1058	Buffer, octal
	HE 434-311	Socket
U360	HE 443-1058	Buffer, octal
	HE 434-311	Socket
U361	HE 443-1058	Buffer, octal
	HE 434-311	Socket
U362	HE 444-241	PROM, decoder, video address
	or	
	HE 444-287	
	HE 434-299	Socket
U363	HE 443-967	Buffer, hex
	HE 434-298	Socket

Parts List

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
Interfaces and Jumpers		
J301	HE 432-1102	Pin, 3M Molex
	HE 432-1041	Pin, 2F Berg
J302	HE 432-1102	Pin, 3M Molex
	HE 432-1041	Pin, 2F Berg
J303	HE 432-1102	Pin, 3M Molex
	HE 432-1041	Pin, 2F Berg
J304	HE 432-1102	Pin, 3M Molex
	HE 432-1041	Pin, 2F Berg
J305	HE 432-1102	Pin, 3M Molex
	HE 432-1041	Pin, 2F Berg
J306	HE 432-1102	Pin, 3M Molex
	HE 432-1041	Pin, 2F Berg
J307	HE 432-1102	Pin, 3M Molex
	HE 432-1041	Pin, 2F Berg
J308	HE 432-1102	Pin, 3M Molex
	HE 432-1041	Pin, 2F Berg
J309	HE 434-107	Plug, Phono
Resistors		
R301	HE 6-102-12	1 KΩ, film
R302	HE 6-2001-12	6.2 KΩ, film
R303	HE 6-102-12	1 KΩ, film
R304	HE 6-181-12	180 Ω, film
R305	HE 6-102-12	1 KΩ, film
R306	HE 6-101-12	100 Ω, film
R307	HE 6-100-12	10 Ω, film
R308	HE 6-101-12	100 Ω, film
R309	HE 6-270-12	27 Ω, film
R310	HE 6-101-12	100 Ω, film
R311	HE 6-470-12	47 Ω, film
R312	HE 6-122-12	27 Ω, film
R313	HE 10-1204-12	1 KΩ, control linear
R314	HE 10-1204-12	1 KΩ, control linear
R315	Not Used	
R316	Not Used	
R317	Not Used	
R318	HE 6-102-12	1 KΩ, film
R319	HE 6-102-12	1 KΩ, film
R320	HE 6-102-12	1 KΩ, film
R321	HE 6-102-12	1 KΩ, film
R322	HE 6-102-12	1 KΩ, film
R323	HE 6-102-12	1 KΩ, film
RP301	HE 9-124	4.7 KΩ × 5
RP302	HE 9-131	390 Ω × 5
RP303	HE 9-156	Resistor ladder 5/2 KΩ 3/1 KΩ
Transistors		
Q303	HE 417-875	Silicon, NPN
Q304	HE 417-875	Silicon, NPN
Q305	HE 417-875	Silicon, NPN
Miscellaneous		
	HE 255-757	Spacer, hex, 4-40 × 4-40 .190
	HE 204-2719	Bracket
	HE 254-14	Washer
	HE 250-1411	Screw, Phillips, pan head
	HE 255-0757	Spacer, hex, threaded
P301	HE 432-1368	Connector, 6M Molex
P302	HE 432-1233	Pin, 10M Molex
P303	HE 432-1233	Pin, 10M Molex
P304	HE 432-1358	Receptacle, 9F Amps
	HE 434-378	IF Phono, 1/4-32 Bushing MTB

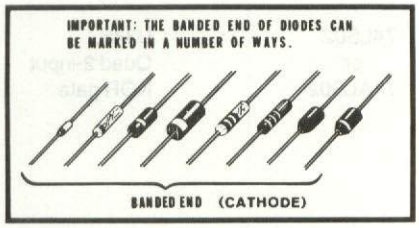
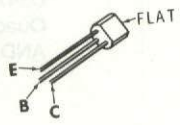
Chapter 7

Semiconductor Identification

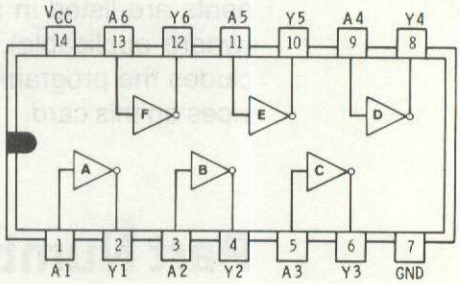
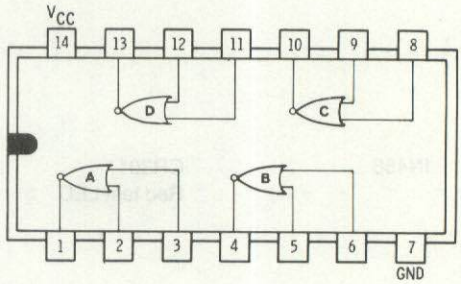
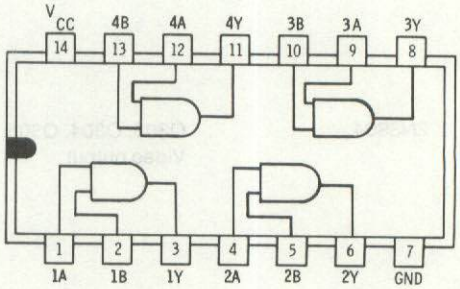
Introduction

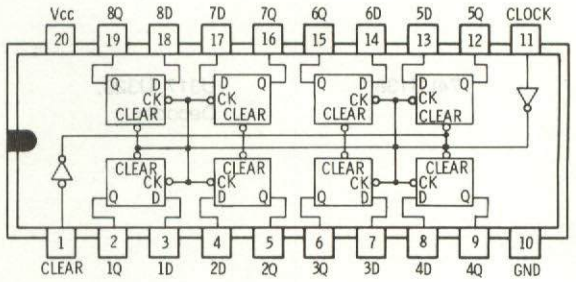
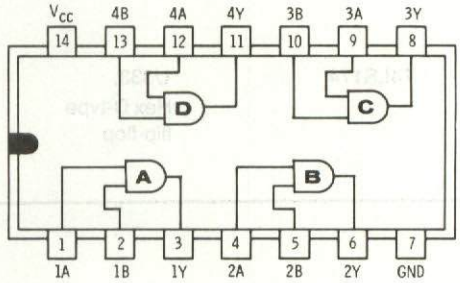
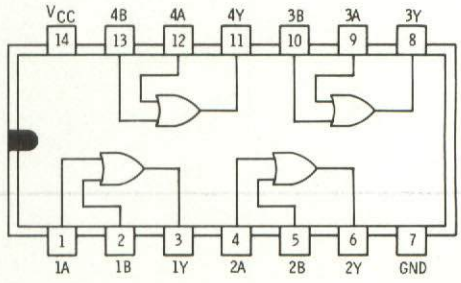
This chapter will help to identify the various semiconductor devices installed on the Z-309A Video Card by cross-referencing, where applicable, the Zenith/Heath part numbers with generic device numbers. The components are listed in ascending numerical order, along with device number (where applicable), and device lead configuration. This chapter also includes the programmable array logic (PAL) equations for the decoder devices on this card.

Part Number Index

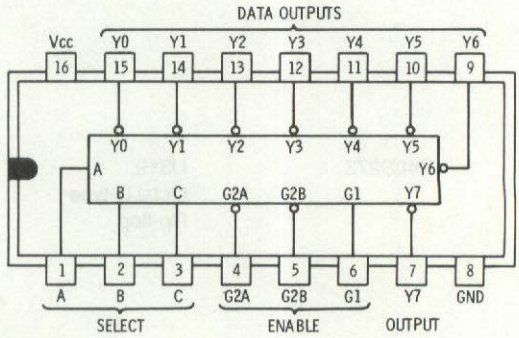
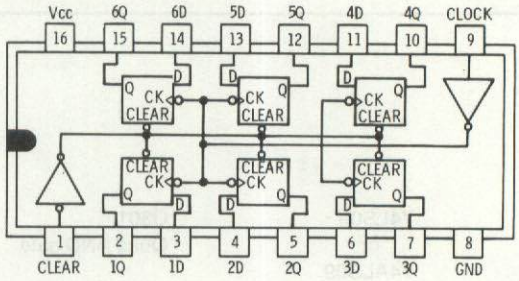
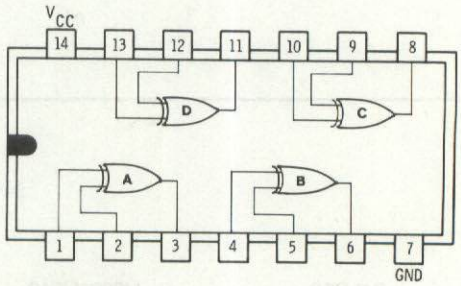
HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
56-24	IN458	CR301, Red test LED	
417-875	2N3904	Q303, Q304, Q305, Video output	

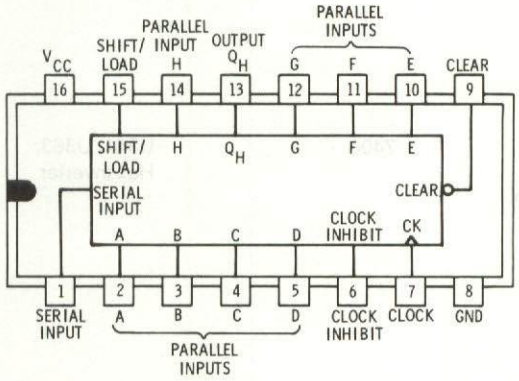
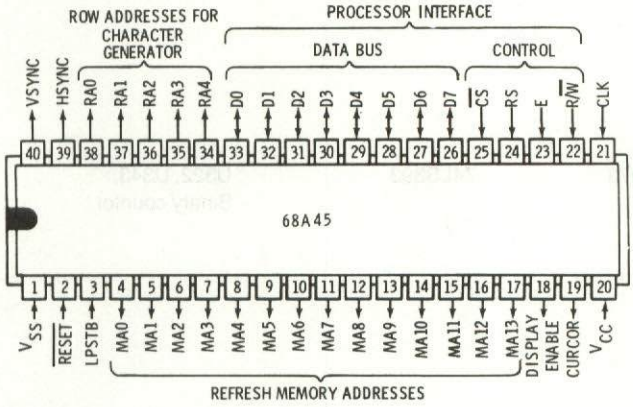
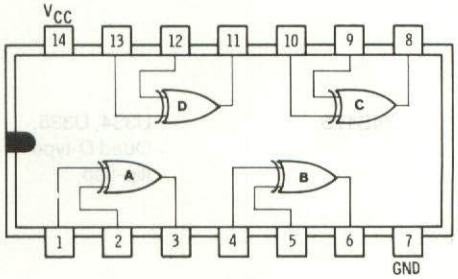
Semiconductor Identification

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
443-755 or 443-1082	74LS04 or 74ALS04	U302, U304, Hex inverter	
443-779 or 443-1045	74LS02 or 74ALS02	U346, Quad 2-input NOR gate	
443-780 or 443-1073	74LS08 or 74ALS08	U347, Quad 2-input AND gate	

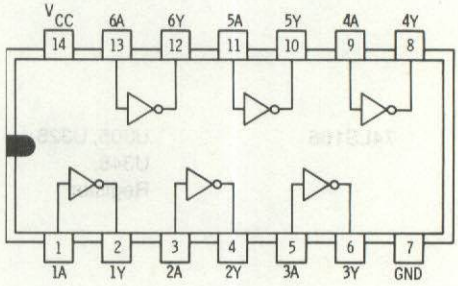
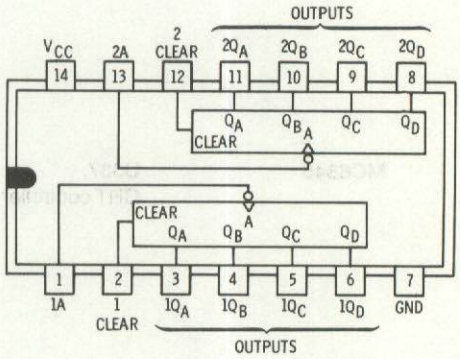
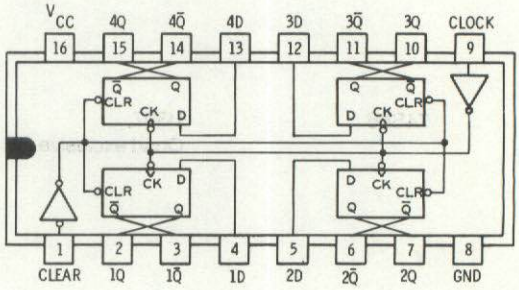
HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
443-805	74LS273	U319, Octal D-type flip-flop	
443-816 or 443-1229	74LS09 or 74ALS09	U301, Quad AND gate	
443-875 or 443-1072	74LS32 or 74ALS32	U303, U313, U345, Quad OR gate	

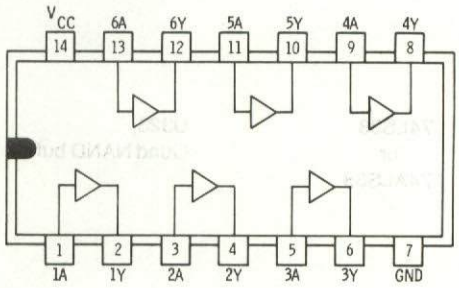
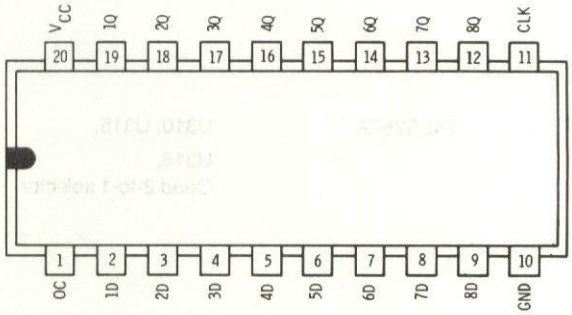
Semiconductor Identification

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
443-877	74LS138	U317, U329, Decoder	
443-879	74LS174	U333, Hex D-type flip-flop	
443-891	74LS86	U339, Quad 2-input exclusive OR	

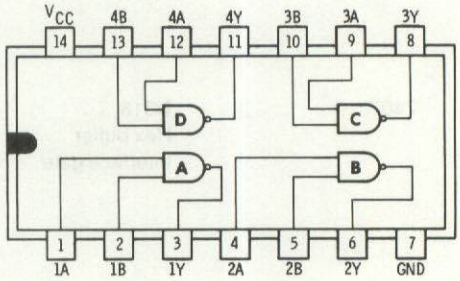
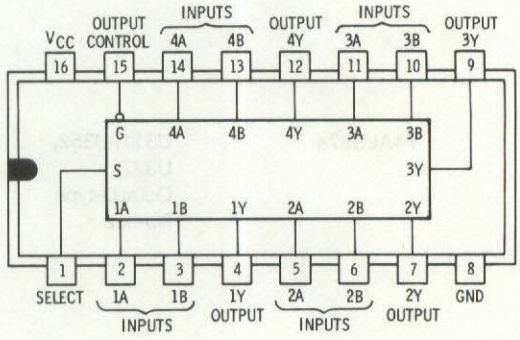
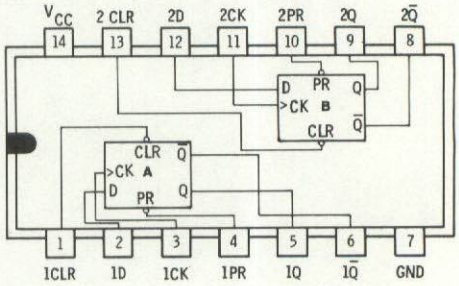
HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
443-892	74LS166	U305, U328, U348, Register	
443-906	MC6845	U337, CRT controller	
443-915	74S86	U307, Quad exclusive OR	

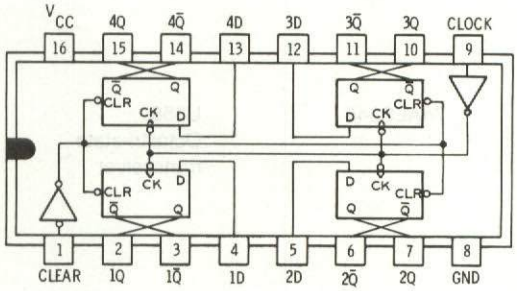
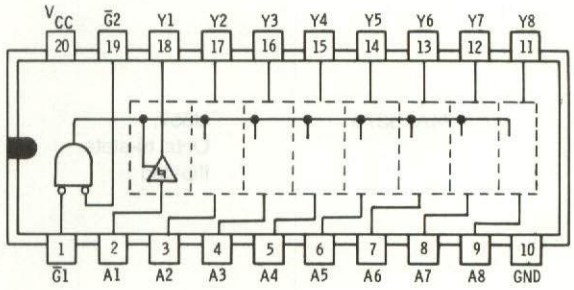
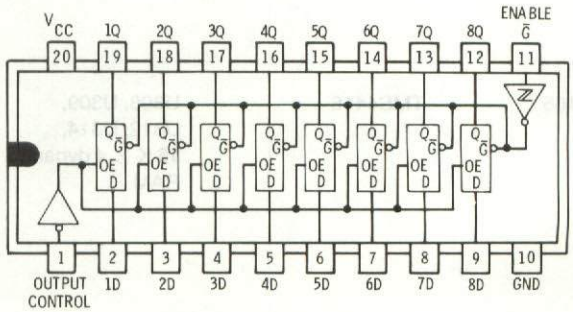
Semiconductor Identification

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
443-967 or 443-1072	7406	U341, U363, Hex inverter	
443-973	74LS393	U322, U343, Binary counter	
443-983	74S175	U334, U335, Quad D-type flip-flop	

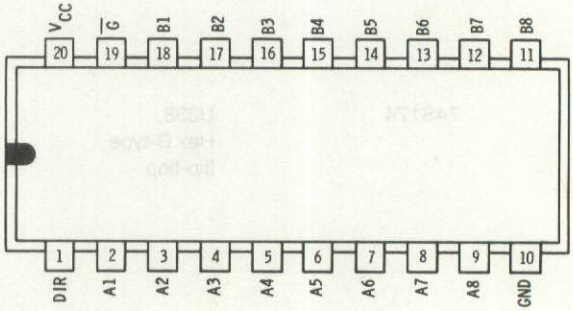
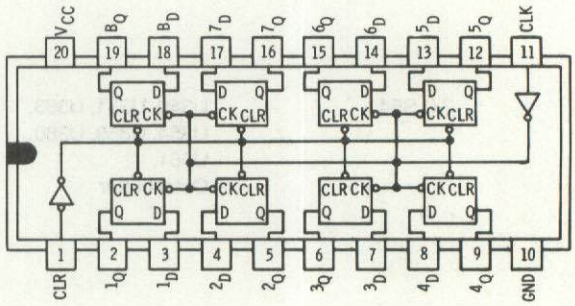
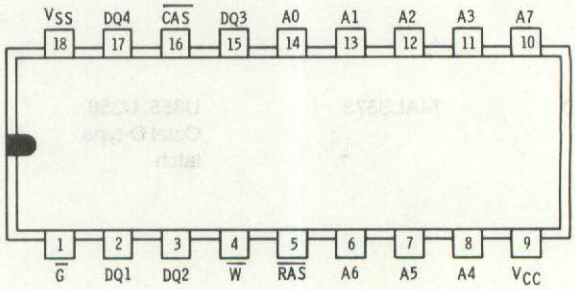
HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
443-1020	7407	U318, Hex buffer Interface gate	
443-1031	74ALS574	U311, U352, U327, Octal D-type flip-flop	

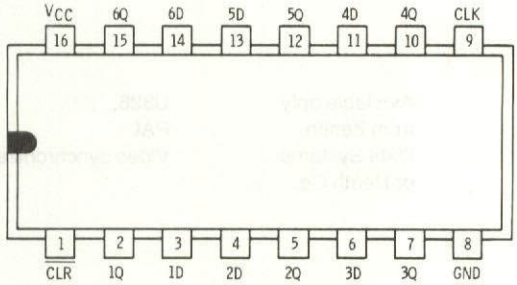
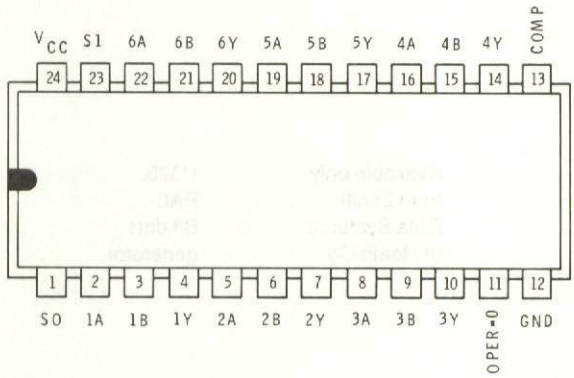
Semiconductor Identification

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
443-1034 or 443-1232	74LS38 or 74ALS38	U323, Quad NAND buffer	
443-1037	74LS257A	U310, U315, U316, Quad 2-to-1 selector	
443-1051	74ALS74	U321, U330, U331, U344, Octal D-type flip-flop	

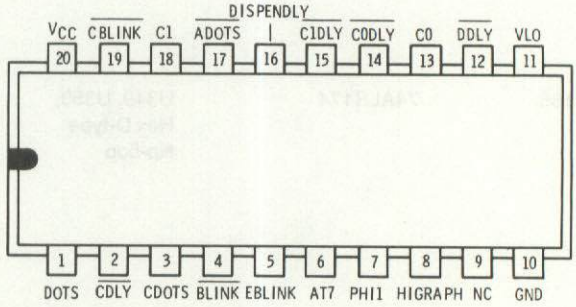
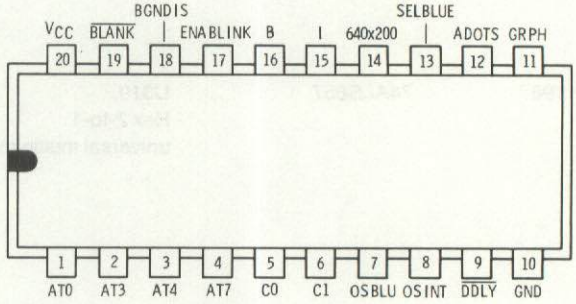
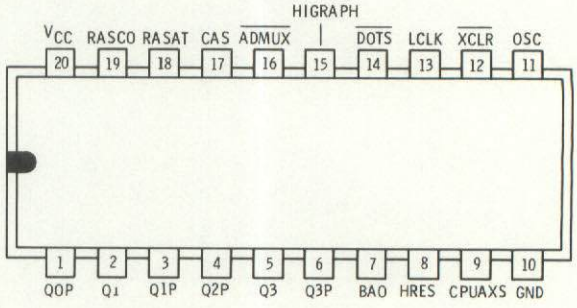
HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
443-1053	74S174	U338, Hex D-type flip-flop	
443-1058	74LS541	U340, U351, U353, U354, U359, U360, U361, Octal buffer	
443-1070	74ALS573	U355, U356, Octal D-type latch	

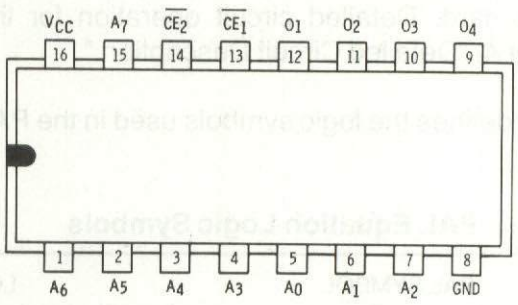
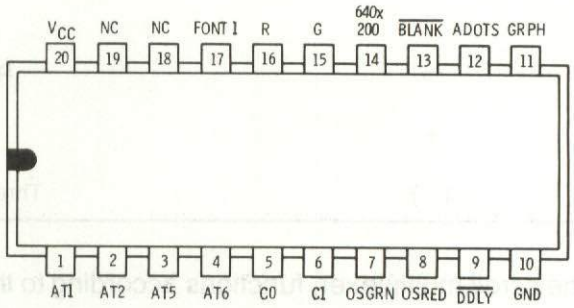
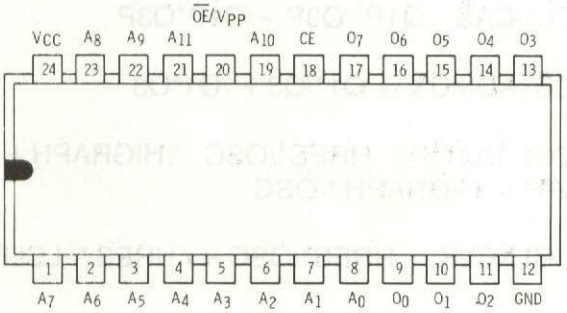
Semiconductor Identification

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
443-1097	74ALS245	U358, Octal tri-state transceiver	
443-1098	74ALS273	U357, Octal tri-state flip-flop	
443-1165	TMS4416	U308, U309, U312, U314, 16 K × 4 dynamic RAM	

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
443-1166	74ALS174	U349, U350, Hex D-type flip-flop	
443-1198	74ALS857	U319, Hex 2-to-1 universal multiplexer	

Semiconductor Identification

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
444-232	Available only from Zenith Data Systems or Heath Co.	U326, PAL Video synchronizer	
444-234	Available only from Zenith Data Systems or Heath Co.	U325, PAL B/I dots generator	
444-235	Available only from Zenith Data Systems or Heath Co.	U332, U336, PAL RAM control Multiplexer, scroll	

HEATH PART NUMBER	DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
444-241 or 444-287	Available only from Zenith Data Systems or Heath Co.	U362, PROM Video address decoder	
444-274	Available only from Zenith Data Systems or Heath Co.	U324, PAL R/G dots generator	
444-230-1 or 444-230-2 or 444-292	Available only from Zenith Data Systems or Heath Co.	U306 PROM Character font PROM	

PAL Equations

This section contains the logic equations for the PAL devices located on the video card. Detailed circuit operation for these devices is covered in Chapter 4, "Detailed Circuit Description."

Table 7.1 defines the logic symbols used in the PAL equations.

Table 7.1. PAL Equation Logic Symbols

PAL SYMBOL	LOGIC FUNCTION
/	Complement
*	AND
=	EQUAL
:=	Replaced by
+	OR
( )	Three state output

U336, the scroll multiplexer, functions according to the following logic:

IF (VCC)/RASCC = QOP*/Q3*CPUAXS*/BAO + /Q3

IF (VCC)/RASAT = QOP*/G3*CPUXS*BAO + /QOP*Q3

IF (VCC)/CAS = Q1P*/Q3P + /Q1P*Q3P

IF (VCC) ADMUX = Q1*/Q3 + /Q1*Q3

IF (VCC) DOTS = HRES*/OSC */HIGRAPH + /HRES*/LCLK* /HIGRAPH + HIGRAPH */OSC

IF (VCC) XCLK = HRES*/OSC + / HRES */ LCLK

U326, the video sync decoder, functions as follows:

ADOTS := /CDLY */CDOTS +/CBLINK */CDOTS +/CDLY *BLINK *EBLINK *AT7

/DISPENDLY := DDLY

C1DLY := /C1 */HIGRAPH +/C1 *PHI1 *HIGRAPH +/C0 */PHI1 *HIGRAPH

C0DLY := /C0 */HIGRAPH

U324, the red/green dot selector, functions as follows:

R = AT2 *DDLY */GRPH *ADOTS */BLANK
+AT6 *DDLY */GRPH */ADOTS */BLANK/FONT 1
+C1 *DDLY *GRPH */640X200 */BLANK
+OSRED */DDLY */BLANK */GRPH
+OSRED *DDLY *GRPH */CO */C1 */640X200 */BLANK
+OSRED *DDLY *GRPH *640X200 *C1 */BLANK
+AT5 *DDLY */GRPH*/ ADOTS*/ BLANK* FONT1

G = AT1 *DDLY */GRPH *ADOTS */BLANK
+AT5 *DDLY */GRPH */ADOTS */BLANK
+C0 *DDLY *GRPH */640X200 */BLANK
+OSGRN */DDLY */BLANK */GRPH
+OSGRN *DDLY *GRPH */C0 */C1 */640X200 */BLANK
+OSGRN *DDLY *GRPH *640X200 *C1 */BLANK

U325, the blue/intensity dot selector, functions as follows:

B = AT0 *DDLY */GRPH *ADOTS */BLANK
+AT4 *DDLY */GRPH */ADOTS */BLANK
+SELBLUE *DDLY *GRPH */640X200 *C1 */BLANK
+SELBLUE *DDLY *GRPH */640X200 *C0 */BLANK
+OSBLU */DDLY */BLANK */GRPH
+OSBLU *DDLY *GRPH */C0 */C1 */640X200 */BLANK
+OSBLU *DDLY *GRPH *640 × 200 *C1 */BLANK

I = AT3 *DDLY */GRPH *ADOTS */BLANK
+AT7 */ENABLINK *DDLY */GRPH */ADOTS */BLANK
+BGNDI *DDLY *GRPH */640X200 *C0 */BLANK
+BGNDI *DDLY *GRPH */640X200 *C1 */BLANK
+OSINT */DDLY */BLANK */GRPH
+OSINT *DDLY *GRPH */C0 */C1 */640X200 */BLANK
+OSINT *DDLY *GRPH *640X200 *C1 */BLANK

U332, the RAM controller, functions as follows:

IF (Vcc) /RASCC = Q0P */Q3 *CPUAXS */BA0 +/Q0P *Q3

IF (Vcc) /RASAT = Q0P */Q3 *CPUAXS *BA0 +/Q0P *Q3

IF (Vcc) /CAS = Q1P */Q3P +/Q1P *Q3P

IF (Vcc) /ADMUX = Q1 */Q3 +/Q1 *Q3

IF (Vcc) /DOTS = HRES */OSC */HIGRAPH +/HRES */LCLK */HIGRAPH +HIGRAPH */OSC

IF (Vcc) /XCLK = HRES */OSC +/HRES */LCLK

Chapter 8

Data Sheets

General

This chapter provides the necessary technical information to understand the 6845 CRT Controller. The following pages are reprinted with the permission of Hitachi.

HD6845S, HD68A45S, HD68B45S

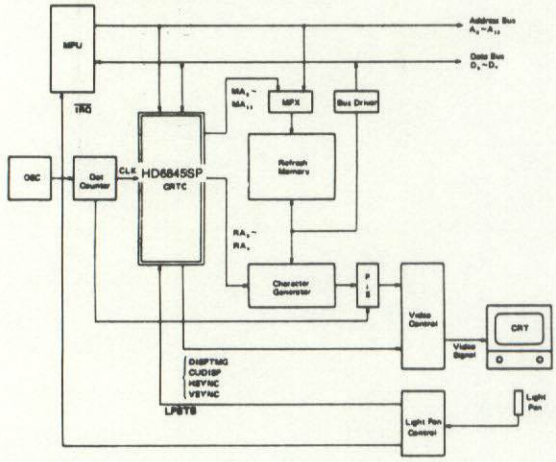
CRTC (CRT Controller)

The CRTC is a LSI controller which is designed to provide an interface for microcomputers to raster scan type CRT displays. The CRTC belongs to the HMCS6800 LSI Family and has full compatibility with MPU in both data lines and control lines. Its primary function is to generate timing signal which is necessary for raster scan type CRT display according to the specification programmed by MPU. The CRTC is also designed as a programmable controller, so applicable to wide-range CRT display from small low-functioning character display up to raster type full graphic display as well as large high-functioning limited graphic display.

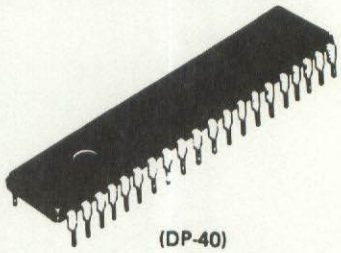
■ FEATURES

- Number of Displayed Characters on the Screen, Vertical Dot Format of One Character, Horizontal and Vertical Sync Signal, Display Timing Signal are Programmable
- 3.7 MHz High Speed Display Operation
- Line Buffer-less Refreshing
- 14-bit Refresh Memory Address Output (16k Words max. Access)
- Programmable Interlace/Non-interlace Scan Mode
- Built-in Cursor Control Function
- Programmable Cursor Height and its Blink
- Built-in Light Pen Detection Function
- Paging and Scrolling Capability
- TTL Compatible
- Single +5V Power Supply
- Upward compatible with MC6845

■ SYSTEM BLOCK DIAGRAM

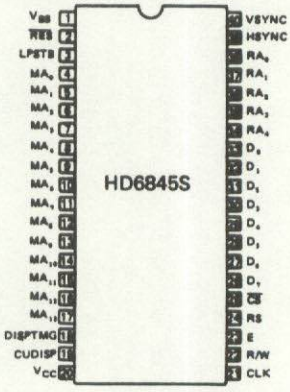


HD6845SP, HD68A45SP, HD68B45SP



(DP-40)

■ PIN ARRANGEMENT



(Top View)

■ ORDERING INFORMATION

CRTC	Bus Timing	CRT Display Timing
HD6845SP	1.0 MHz	3.7 MHz max.
HD68A45SP	1.5 MHz	
HD68B45SP	2.0 MHz	

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage	V_{CC} *	−0.3 ~ +7.0	V
Input Voltage	V_{in} *	−0.3 ~ +7.0	V
Operating Temperature	T_{opr}	− 20 ~ + 75	°C
Storage Temperature	T_{stg}	− 55 ~ +150	°C

* With respect to V_{SS} (SYSTEM GND)

[NOTE] Permanent LSI damage may occur if maximum ratings are exceeded. Normal operation should be under recommended operating conditions. If these conditions are exceeded, it could affect reliability of LSI.

■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC} *	4.75	5	5.25	V
Input Voltage	V_{IL} *	−0.3	–	0.8	V
	V_{IH} *	2.0	–	V_{CC}	V
Operating Temperature	T_{opr}	− 20	25	75	°C

* With respect to V_{SS} (SYSTEM GND)

■ ELECTRICAL CHARACTERISTICS

• DC CHARACTERISTICS (V_{CC} = 5V ± 5%, V_{SS} = 0V, Ta = −20~+75°C, unless otherwise noted.)

Item	Symbol	Test Condition		min	typ	max	Unit
Input "High" Voltage	V_{IH}			2.0	–	V_{CC}	V
Input "Low" Voltage	V_{IL}			−0.3	–	0.8	V
Input Leakage Current	I_{in}	V_{in} = 0 ~ 5.25V (Except D_0~D_7)		−2.5	–	2.5	μA
Three-State Input Current (off-state)	I_{TSI}	V_{in} = 0.4 ~ 2.4V V_{CC} = 5.25V (D_0~ D_7)		− 10	–	10	μA
Output "High" Voltage	V_{OH}	I_{LOAD} = −205 μA (D_0~ D_7)		2.4	–	–	V
		I_{LOAD} = −100 μA (Other Outputs)					
Output "Low" Voltage	V_{OL}	I_{LOAD} = 1.6 mA		–	–	0.4	V
Input Capacitance	C_{in}	V_{in} = 0 Ta = 25°C f = 1.0 MHz	D_0 ~ D_7	–	–	12.5	pF
			Other Inputs	–	–	10.0	pF
Output Capacitance	C_{out}	V_{in} = 0V, Ta = 25°C, f = 1.0 MHz		–	–	10.0	pF
Power Dissipation	P_D			–	600	1000	mW

• **AC CHARACTERISTICS** (V_{CC} = 5V ±5%, V_{SS} = 0V, Ta = -20~+75°C, unless otherwise noted.)

1. TIMING OF CRTC SIGNAL

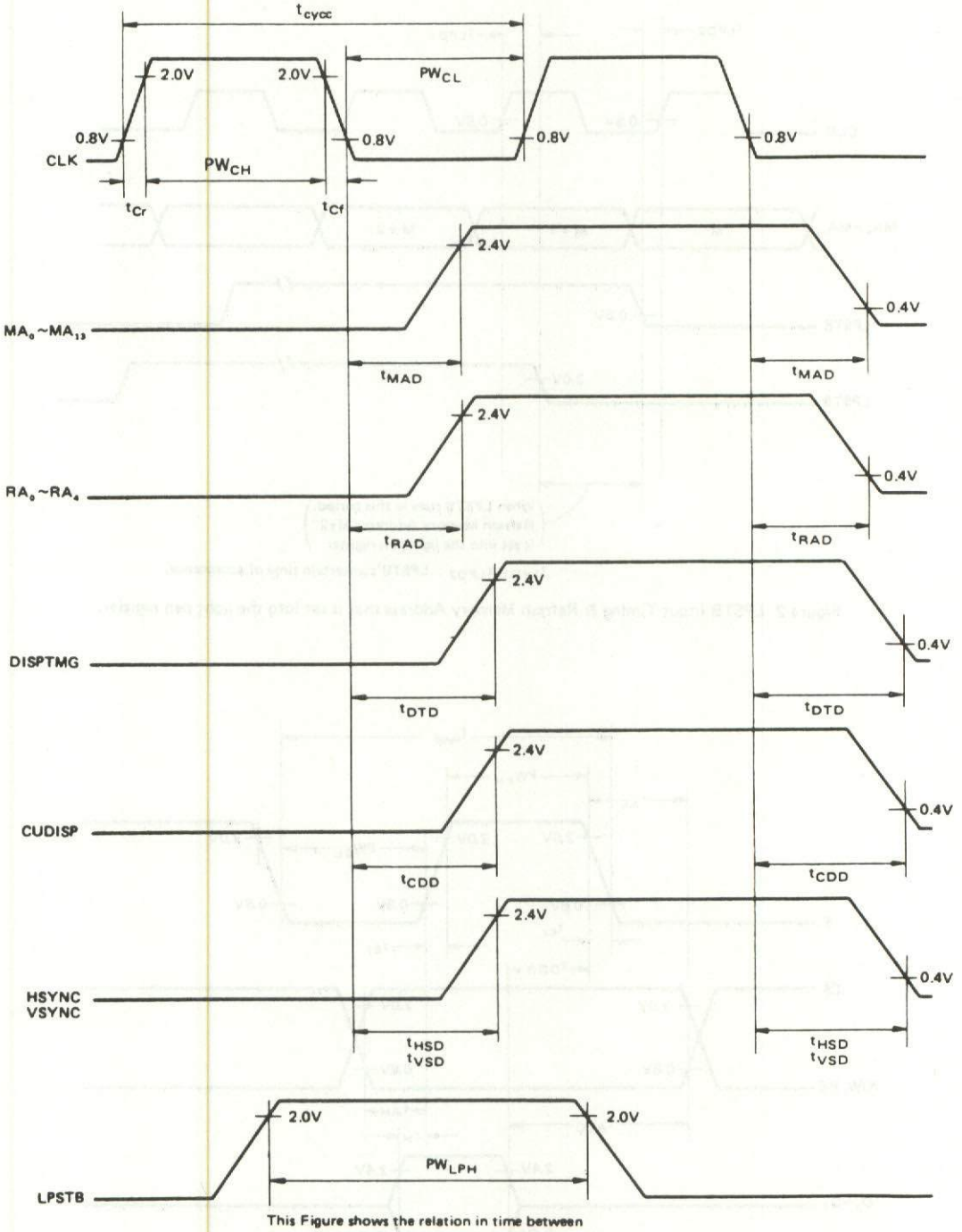
Item	Symbol	Test Condition	min	typ	max	Unit
Clock Cycle Time	t_{cycc}	Fig. 1	270	–	–	ns
Clock "High" Pulse Width	PW_{CH}		130	–	–	ns
Clock "Low" Pulse Width	PW_{CL}		130	–	–	ns
Rise and Fall Time for Clock Input	t_{Cr}, t_{Cf}		–	–	20	ns
Memory Address Delay Time	t_{MAD}		–	–	160	ns
Raster Address Delay Time	t_{RAD}		–	–	160	ns
DISPTMG Delay Time	t_{DTD}		–	–	250	ns
CUDISP Delay Time	t_{CDD}		–	–	250	ns
Horizontal Sync Delay Time	t_{HSD}		–	–	200	ns
Vertical Sync Delay Time	t_{VSD}		–	–	250	ns
Light Pen Strobe Pulse Width	PW_{LPH}		60	–	–	ns
Light Pen Strobe	t_{LPD1}	Fig. 2	–	–	70	ns
Uncertain Time of Acceptance	t_{LPD2}		–	–	0	ns

2. MPU READ TIMING

Item	Symbol	Test Condition	HD6845SP			HD68A45SP			HD68B45SP			Unit
			min	typ	max	min	typ	max	min	typ	max	
Enable Cycle Time	t_{cycE}	Fig. 3	1.0	–	–	0.666	–	–	0.5	–	–	μs
Enable "High" Pulse Width	PW_{EH}		0.45	–	–	0.280	–	–	0.22	–	–	μs
Enable "Low" Pulse Width	PW_{EL}		0.40	–	–	0.280	–	–	0.21	–	–	μs
Enable Rise and Fall Time	t_{Er}, t_{Ef}		–	–	25	–	–	25	–	–	25	ns
Address Set Up Time	t_{AS}		140	–	–	140	–	–	70	–	–	ns
Data Delay Time	t_{DDR}		–	–	320	–	–	220	–	–	180	ns
Data Hold Time	t_{H}		10	–	–	10	–	–	10	–	–	ns
Address Hold Time	t_{AH}		10	–	–	10	–	–	10	–	–	ns
Data Access Time	t_{ACC}		–	–	460	–	–	360	–	–	250	ns

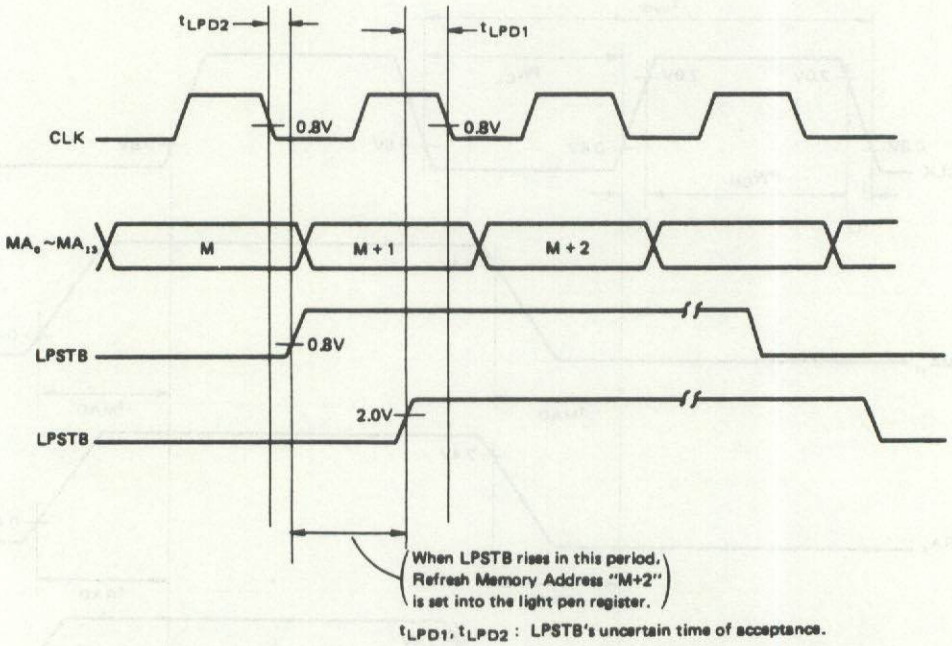
3. MPU WRITE TIMING

Item	Symbol	Test Condition	HD6845SP			HD68A45SP			HD68B45SP			Unit
			min	typ	max	min	typ	max	min	typ	max	
Enable Cycle Time	t_{cycE}	Fig. 4	1.0	–	–	0.666	–	–	0.5	–	–	μs
Enable "High" Pulse Width	PW_{EH}		0.45	–	–	0.280	–	–	0.22	–	–	μs
Enable "Low" Pulse Width	PW_{EL}		0.40	–	–	0.280	–	–	0.21	–	–	μs
Enable Rise and Fall Time	t_{Er}, t_{Ef}		–	–	25	–	–	25	–	–	25	ns
Address Set Up Time	t_{AS}		140	–	–	140	–	–	70	–	–	ns
Data Set Up Time	t_{DSW}		195	–	–	80	–	–	60	–	–	ns
Data Hold Time	t_{H}		10	–	–	10	–	–	10	–	–	ns
Address Hold Time	t_{AH}		10	–	–	10	–	–	10	–	–	ns



This Figure shows the relation in time between CLK signal and each output signals. Output sequence is shown in Figs. 9 ~ 15.

Figure 1 Time Chart of the CRTC



t_{LPD1}, t_{LPD2} : LPSTB's uncertain time of acceptance.

Figure 2 LPSTB Input Timing & Refresh Memory Address that is set into the light pen register.

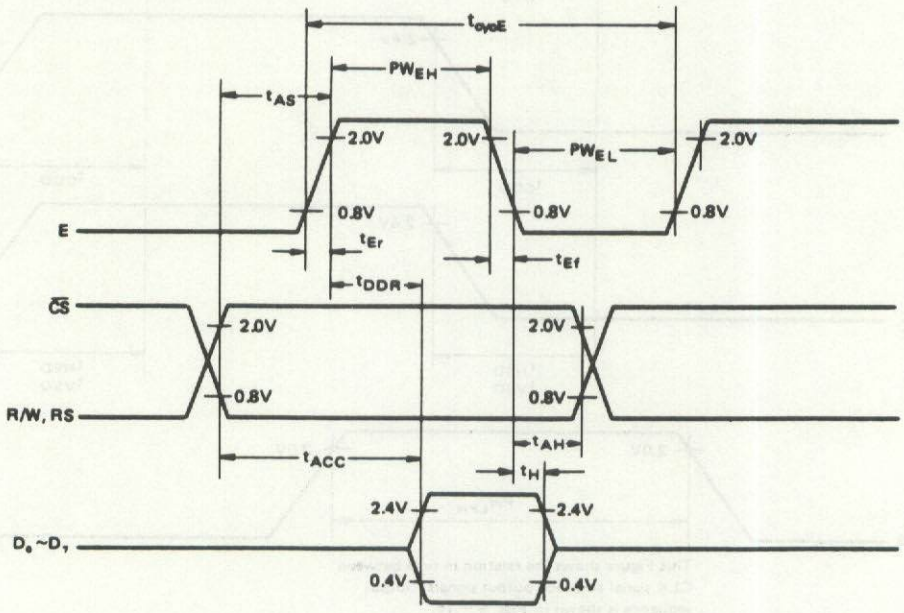


Figure 3 Read Sequence

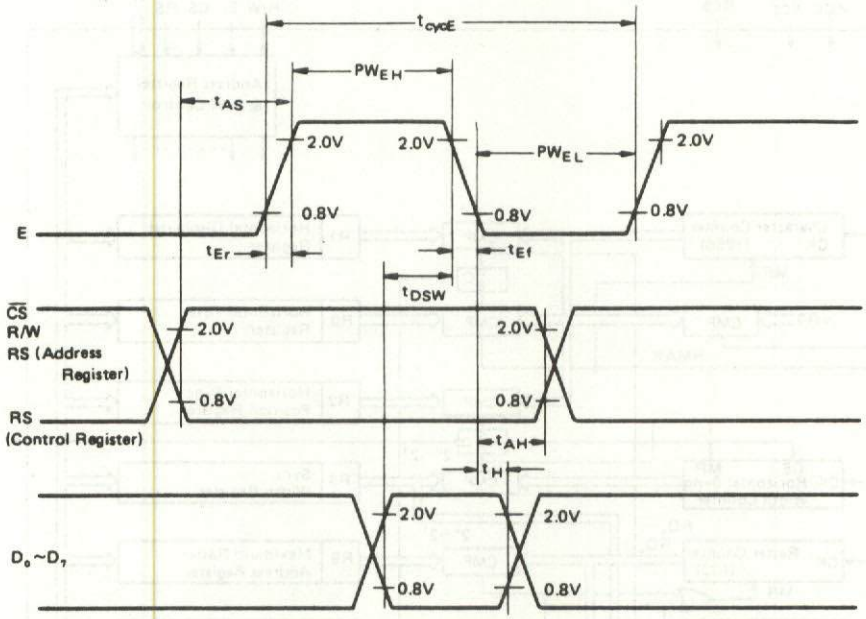


Figure 4 Write Sequence

■ SYSTEM DESCRIPTION

The CRTC is a LSI which is connected with MPU and CRT display device to control CRT display. The CRTC consists of internal register group, horizontal and vertical timing circuits, linear address generator, cursor control circuit, and light pen detection circuit. Horizontal and vertical timing circuit generate RA_0~RA_4, DISPTMG, HSYNC, and VSYNC. RA_0~RA_4 are raster address signals and used as input signals for Character Generator. DISPTMG, HSYNC, and VSYNC signals are received by video control circuit. This horizontal and vertical timing circuit consists of internal counter and comparator circuit. Linear address generator generates refresh memory address MA_0 ~MA_{13} to be used for refreshing the screen. By these address signals, refresh memory is accessed periodically. As 14 refresh memory address signals are prepared, 16k words max are accessible. Moreover, the use of start address register enables paging and scrolling. Light pen detection circuit detects light pen position on the screen. When light pen strobe signal is received, light pen register memorizes linear address generated by linear address generator in order to memorize where light pen is on the screen. Cursor control circuit controls the position of cursor, its height, and its blink.

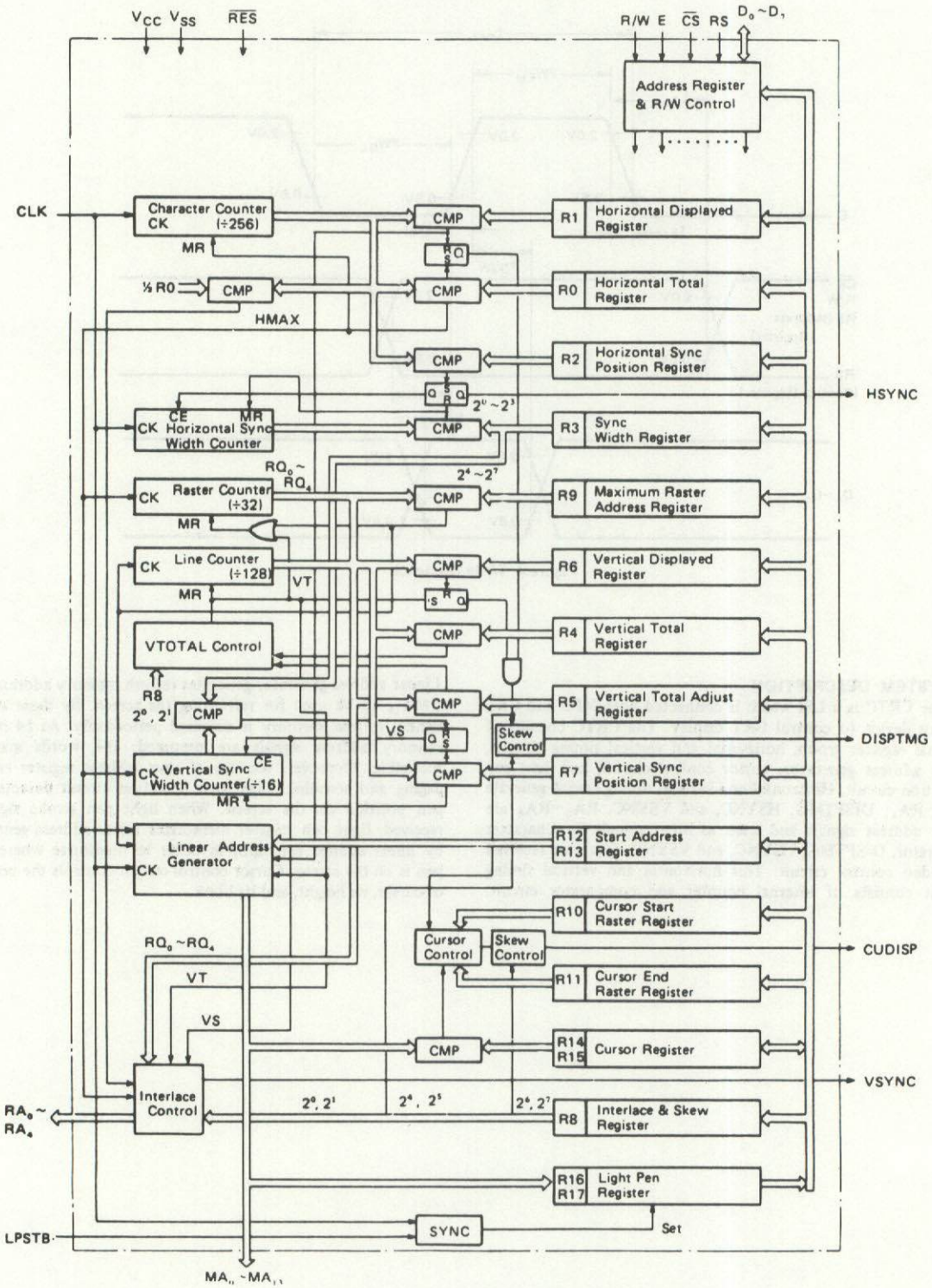


Figure 5 Internal Block Diagram of the CRTC

■ FUNCTION OF SIGNAL LINE

The CRTC provides 13 interface signals to MPU and 25 interface signals to CRT display.

• Interface Signals to MPU

Bi-directional Data Bus (D_0~D_7)

Bi-directional data bus(D_0~D_7) are used for data transfer between the CRTC and MPU. The data bus outputs are 3-state buffers and remain in the high-impedance state except when MPU performs a CRTC read operation.

Read/Write (R/W)

R/W signal controls the direction of data transfer between the CRTC and MPU. When R/W is at "High" level, data of CRTC is transfered to MPU. When R/W is at "Low" level, data of MPU is transfered to CRTC.

Chip Select ($\overline{CS}$)

Chip Select signal ($\overline{CS}$) is used to address the CRTC. When $\overline{CS}$ is at "Low" level, it enables R/W operation to CRTC internal registers. Normally this signal is derived from decoded address signal of MPU under the condition that VMA signal of MPU is at "High" level.

Register Select (RS)

Register Select signal (RS) is used to select the address register and 18 control registers of the CRTC. When RS is at "Low" level, the address register is selected and when RS is at "High" level, control registers are selected. This signal is normally a derivative of the lowest bit (A0) of MPU address bus.

Enable(E)

Enable signal (E) is used as strobe signal in MPU R/W operation with the CRTC internal registers. This signal is normally a derivative of the HMCS6800 System ϕ_2 clock.

Reset ($\overline{RES}$)

Reset signal ($\overline{RES}$) is an input signal used to reset the CRTC. When $\overline{RES}$ is at "Low" level, it forces the CRTC into the following status.

1) All the counters in the CRTC are cleared and the device stops the display operation.
2) All the outputs go down to "Low" level.
3) Control registers in the CRTC are not affected and remain unchanged.

This signal is different from other HMCS6800 family LSIs in the following functions and has restrictions for usage.

1) $\overline{RES}$ signal has capability of reset function only when LPSTB is at "Low" level.
2) The CRTC starts the display operation immediately after $\overline{RES}$ signal goes "High".

• Interface Signals to CRT Display Device

Character Clock (CLK)

CLK is a standard clock input signal which defines character timing for the CRTC display operation. This signal is normally derived from the external high-speed dot timing logic.

Horizontal Sync (HSYNC)

HSYNC is an active "High" level signal which provides horizontal synchronization for display device.

Vertical Sync (VSYNC)

VSYNC is an active "High" level signal which provides vertical synchronization for display device.

Display Timing (DISPTMG)

DISPTMG is an active "High" level signal which defines the display period in horizontal and vertical raster scanning. It is necessary to enable video signal only when DISPTMG is at "High" level.

Refresh Memory Address (MA_0~MA_{13})

MA_0~MA_{13} are refresh memory address signals which are used to access to refresh memory in order to refresh the CRT screen periodically. These outputs enables 16k words max. refresh memory access. So, for instance, these are applicable up to 2000 characters/screen and 8-page system.

Raster Address (RA_0~RA_4)

RA_0~RA_4 are raster address signals which are used to select the raster of the character generator or graphic pattern generator etc.

Cursor Display (CUDISP)

CUDISP is an active "High" level video signal which is used to display the cursor on the CRT screen. This output is inhibited while DISPTMG is at "Low" level. Normally this output is mixed with video signal and provided to the CRT display device.

Light Pen Strobe (LPSTB)

LPSTB is an active "High" level input signal which accepts strobe pulse detected by the light pen and control circuit. When this signal is activated, the refresh memory address (MA_0~MA_{13}) which are shown in Fig. 2 are stored in the 14-bit light pen register. The stored refresh memory address need to be corrected in software, taking the delay time of the display device, light pen, and light pen control circuits into account.

■ REGISTER DESCRIPTION

Table 1 Internal Registers Assignment

$\overline{CS}$	RS	Address Register 4 3 2 1 0	Register #	Register Name	Program Unit	READ	WRITE	Data Bit 7	6	5	4	3	2	1	0
1	×	× × × × ×			–	–	–								
0	0	× × × × ×	AR	Address Register	–	×	O								
0	1	0 0 0 0 0	R0	Horizontal Total *	Character	×	O								
0	1	0 0 0 0 1	R1	Horizontal Displayed	Character	×	O								
0	1	0 0 0 1 0	R2	Horizontal Sync* Position	Character	×	O								
0	1	0 0 0 1 1	R3	Sync Width	Vertical-Raster, Horizontal-Character	×	O	wv3	wv2	wv1	wv0	wh3	wh2	wh1	wh0
0	1	0 0 1 0 0	R4	Vertical Total *	Line	×	O								
0	1	0 0 1 0 1	R5	Vertical Total Adjust	Raster	×	O								
0	1	0 0 1 1 0	R6	Vertical Displayed	Line	×	O								
0	1	0 0 1 1 1	R7	Vertical Sync * Position	Line	×	O								
0	1	0 1 0 0 0	R8	Interlace & Skew	–	×	O	C1	C0	D1	D0			V	S
0	1	0 1 0 0 1	R9	Maximum Raster Address	Raster	×	O								
0	1	0 1 0 1 0	R10	Cursor Start Raster	Raster	×	O		B	P					
0	1	0 1 0 1 1	R11	Cursor End Raster	Raster	×	O								
0	1	0 1 1 0 0	R12	Start Address(H)	–	O	O								
0	1	0 1 1 0 1	R13	Start Address(L)	–	O	O								
0	1	0 1 1 1 0	R14	Cursor(H)	–	O	O								
0	1	0 1 1 1 1	R15	Cursor (L)	–	O	O								
0	1	1 0 0 0 0	R16	Light Pen(H)	–	O	×								
0	1	1 0 0 0 1	R17	Light Pen(L)	–	O	×								

[NOTE] 1. The Registers marked *: (Written Value) = (Specified Value) – 1
2. Written Value of R9 is mentioned below.
1) Non-interlace Mode / Interlace Sync Mode } (Written Value Nr) = (Specified Value) – 1
2) Interlace Sync & Video Mode
(Written Value Nr) = (Specified Value) – 2
3. C0 and C1 specify skew of CUDISP output signal.
D0 and D1 specify skew of DISPTMG output signal.
When S is "1", V specifies video mode. S specifies the Interlace Sync Mode.
4. B specifies the cursor blink. P specifies the cursor blink period.
5. wv0~wv3 specify the pulse width of Vertical Sync Signal.
wh0~wh3 specify the pulse width of Horizontal Sync Signal.
6. R0 is ordinally programmed to be odd number in interlace mode.
7. O; Yes, ×; No

- **Address Register (AR)**

This is a 5-bit register used to select 18 internal control registers (R0~R17). Its contents are the address of one of 18 internal control registers. Programming the data from 18 to 31 produces no results. Access to R0~R17 requires, first of all, to write the address of corresponding control register into this register. When RS and $\overline{CS}$ are at "Low" level, this register is selected.

- **Horizontal Total Register (R0)**

This is a register used to program total number of horizontal characters per line including the retrace period. The data is 8-bit and its value should be programmed according to the specification of the CRT. When M is total number of characters, (M-1) shall be programmed to this register. When programming for interlace mode, M must be even.

- **Horizontal Displayed Register (R1)**

This is a register used to program the number of horizontal displayed characters per line. Data is 8-bit and any number that is smaller than that of horizontal total characters can be programmed.

- **Horizontal Sync Position Register (R2)**

This is a register used to program horizontal sync position as multiples of the character clock period. Data is 8-bit and any number that is lower than the horizontal total number can be programmed. When H is character number of horizontal Sync Position, (H-1) shall be programmed to this register. When programmed value of this register is increased, the display position on the CRT screen is shifted to the left. When programmed value is decreased, the position is shifted to the right. Therefore, the optimum horizontal position can be determined by this value.

- **Sync Width Register (R3)**

This is a register used to program the horizontal sync pulse width and the vertical sync pulse width. The horizontal sync pulse width is programmed in the lower 4-bit as multiples of the character clock period. "0" cannot be programmed. The vertical sync pulse width is programmed in higher 4-bit as multiples of the raster period. When "0" is programmed in higher 4-bit, 16 raster period (16H) is specified.

- **Vertical Total Register (R4)**

This is a register used to program total number of lines per frame including vertical retrace period. The data is within 7-bit and its value should be programmed according to the specification of the CRTC. When N is total number of lines, (N-1) shall be programmed to this register.

- **Vertical Total Adjust Register (R5)**

This is a register used to program the optimum number to adjust total number of rasters per field. This register enables to decide the number of vertical deflection frequency more strictly.

- **Vertical Displayed Register (R6)**

This is a register used to program the number of displayed character rows on the CRT screen. Data is 7-bit and any number that is smaller than that of vertical total characters can be programmed.

Table 2 Pulse Width of Vertical Sync Signal

VSW				Pulse Width
2^7	2^6	2^5	2^4	
0	0	0	0	16H
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

H; Raster period

Table 3 Pulse Width of Horizontal Sync Signal

HSW				Pulse Width
2^3	2^2	2^1	2^0	
0	0	0	0	– (Note)
0	0	0	1	1 CH
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

CH; Character clock period
(Note) HSW = "0" cannot be used.

- **Vertical Sync Position Register (R7)**

This is a register used to program the vertical sync position on the screen as multiples of the horizontal character line period. Data is 7-bit and any number that is equal to or less than vertical total characters can be programmed. When V is character number of vertical sync position, (V-1) shall be programmed to this register. When programmed value of this register is increased, the display position is shifted up. When programmed value is decreased, the position is shifted down. Therefore, the optimum vertical position may be determined by this value.

- **Interlace and Skew Register (R8)**

This is a register used to program raster scan mode and skew (delay) of CUDISP signal and DISPTMG signal.

Interlace Mode Program Bit (V, S)

Raster scan mode is programmed in the V, S bit.

Table 4 Interlace Mode (2^1, 2^0)

V	S	Raster Scan Mode
0	0	Non-interlace Mode
1	0	
0	1	Interlace Sync Mode
1	1	Interlace Sync & Video Mode

In the non-interlace mode, the rasters of even number field and odd number field are scanned duplicatedly. In the interlace sync mode, the rasters of odd number field are scanned in the middle of even number field. Then it is controlled to display the same character pattern in two fields. In the interlace sync and video mode, the raster scan method is the same as the interlace sync mode, but it is controlled to display different character pattern in two field.

Skew Program Bit (C1, C0, D1, D0)

These are used to program the skew (delay) of CUDISP signal and DISPTMG signal.

Skew of these two kinds of signals are programmed separately.

Table 5 DISPTMG Skew Bit (2^7, 2^6)

D1	D0	DISPTMG Signal
0	0	Non-skew
0	1	One-character skew
1	0	Two-character skew
1	1	Non-output

Table 6 Cursor Skew Bit (2^5, 2^4)

C1	C0	Non-skew
0	0	Non-skew
0	1	One-character skew
1	0	Two-character skew
1	1	Non-output

Skew function is used to delay the output timing of CUDISP and DISPTMG signals in LSI for the time to access refresh memory, character generator or pattern generator, and to make the same phase with serial video signal.

- **Maximum Raster Address Register (R9)**

This is a register used to program maximum raster address within 5-bit. This register defines total number of rasters per character including space. This register is programmed as follows.

Non-interlace Mode, Interlace Sync Mode

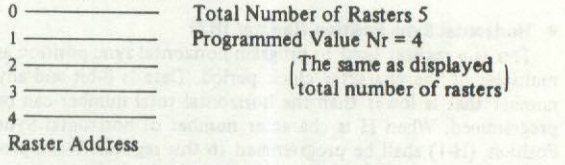
When total number of rasters is RN, (RN-1) shall be programmed.

Interlace Sync & Video Mode

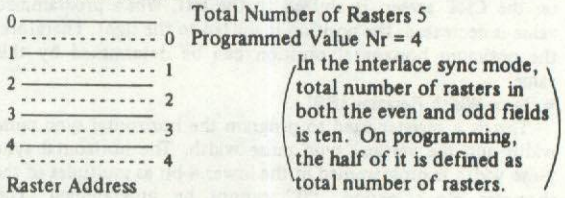
When total number of rasters is RN, (RN-2) shall be programmed.

This manual defines total number of rasters in non-interlace mode, interlace sync mode and interlace sync & video mode as follows:

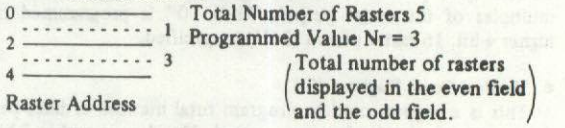
Non-interlace Mode



Interlace Sync Mode



Interlace Sync & Video Mode

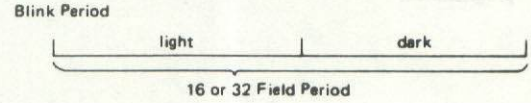


- **Cursor Start Raster Register (R10)**

This is a register used to program the cursor start raster address by lower 5-bit ($2^0 \sim 2^4$) and the cursor display mode by higher 2-bit (2^5, 2^6).

Table 7 Cursor Display Mode (2^6, 2^5)

B	P	Cursor Display Mode
0	0	Non-blink
0	1	Cursor Non-display
1	0	Blink, 16 Field Period
1	1	Blink, 32 Field Period



- **Cursor End Raster Register (R11)**
  This is register used to program the cursor end raster address.

- **Start Address Register (R12, R13)**
  These are used to program the first address of refresh memory to read out.
  Paging and scrolling is easily performed using this register. This register can be read but the higher 2-bit (2^6, 2^7) of R12 are always "0".

- **Cursor Register (R14, R15)**
  These two read/write registers stores the cursor location. The higher 2-bit (2^6, 2^7) of R14 are always "0".

- **Light Pen Register (R16, R17)**
  These read only registers are used to catch the detection address of the light pen. The higher 2-bit (2^6, 2^7) of R16 are always "0". Its value needs to be corrected by software because there is time delay from address output of the CRTC to signal input LPSTB pin of the CRTC in the process that raster is lit after address output and light pen detects it. Moreover, delay time shown in Fig. 2 needs to be taken into account.

Restriction on Programming Internal Register

1) $0 < Nhd < Nht + 1 \leqq 256$
2) $0 < Nvd < Nvt + 1 \leqq 128$
3) $0 \leqq Nhsp \leqq Nht$
4) $0 \leqq Nvsp \leqq Nvt$*
5) $0 \leqq N_{CSTART} \leqq N_{CEND} \leqq Nr$ (Non-interlace, Interlace sync mode)
   $0 \leqq N_{CSTART} \leqq N_{CEND} \leqq Nr + 1$ (Interlace sync & video mode)
6) $2 \leqq Nr \leqq 30$
7) $3 \leqq Nht$ (Except non-interlace mode)
   $5 \leqq Nht$ (Non-interlace mode only)

* In the interlace mode, pulse width is changed ±½ raster time when vertical sync signal extends over two fields.

Notes for Use

The method of directly using the value programmed in the internal register of LSI for controlling the CRT is adopted. Consequently, the display may flicker on the screen when the contents of the registers are changed from bus side asyncronously with the display operation.

Cursor Register

Writing into this register at frequent intervals for moving the cursor should be performed during horizontal and vertical retrace period.

Start Address Register

Writing into the start address register at frequent intervals for scrolling and paging should be performed during horizontal and vertical display period.

It is desirable to avoid programming other registers during display operation.

■ OPERATION OF THE CRTC

- **Time Chart of CRT Interface Signals**

The following example shows the display operation in which values of Table 8 are programmed to the CRTC internal registers. Fig. 6 shows the CRT screen format. Fig. 9 shows the time chart of signals output from the CRTC.

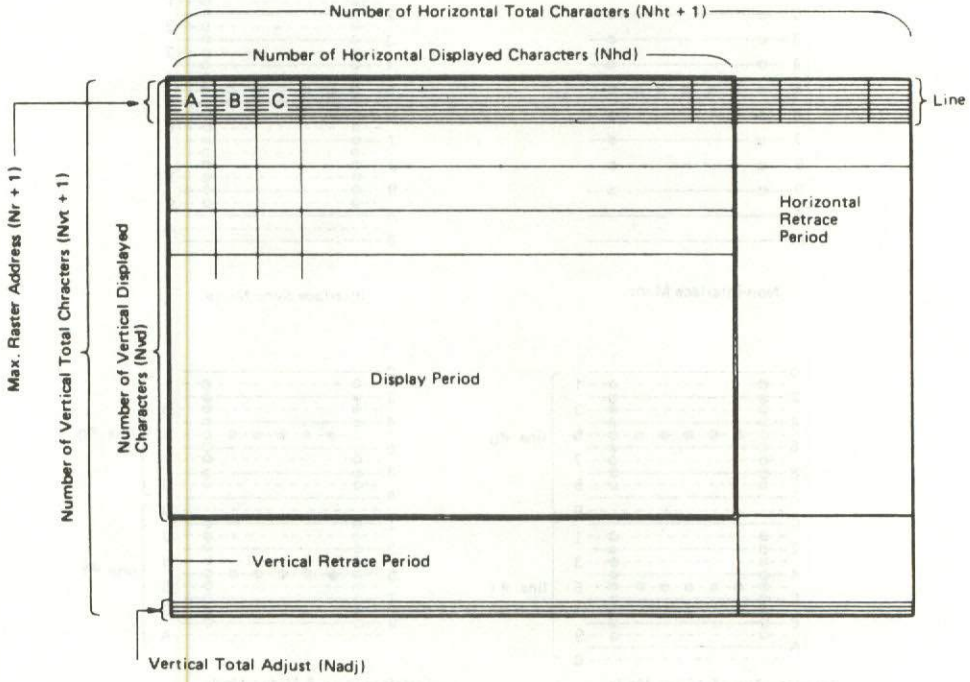


Figure 6 CRT screen Format

Table 8 Programmed Values into the Registers

Register	Register Name	Value	Register	Register Name	Value
R0	Horizontal Total	Nht	R9	Max. Raster Address	Nr
R1	Horizontal Displayed	Nhd	R10	Cursor Start Raster	
R2	Horizontal Sync Position	Nhsp	R11	Cursor End Raster	
R3	Sync Width	Nvsw, Nhsw	R12	Start Address (H)	0
R4	Vertical Total	Nvt	R13	Start Address (L)	0
R5	Vertical Total Adjust	Nadj	R14	Cursor (H)	
R6	Vertical Displayed	Nvd	R15	Cursor (L)	
R7	Vertical Sync Position	Nvsp	R16	Light Pen (H)	
R8	Interlace & Skew		R17	Light Pen (L)	

[NOTE] Nhd<Nht, Nvd<Nvt

The relation between values of Refresh Memory Address ($MA_0 \sim MA_{13}$) and Raster Address ($RA_0 \sim RA_4$) and the display position on the screen is shown in Fig. 15. Fig. 15 shows the case where the value of Start Address is 0.

- **Interlace Control**

Fig. 7 shows an example where the same character is displayed in the non-interlace mode, interlace sync mode, and video mode.

Non-interlace Mode Display

In non-interlace mode, each field is scanned duplicatedly. The values of raster addresses ($RA_0 \sim RA_4$) are counted up one from 0.

Interlace Sync Mode Display

In the interlace sync mode, raster addressed in the even field and the odd field are the same as addressed in the noninterlace mode. One character pattern is displayed mutually and its displayed position in the odd field is set at 1/2 raster space down from that in the even field.

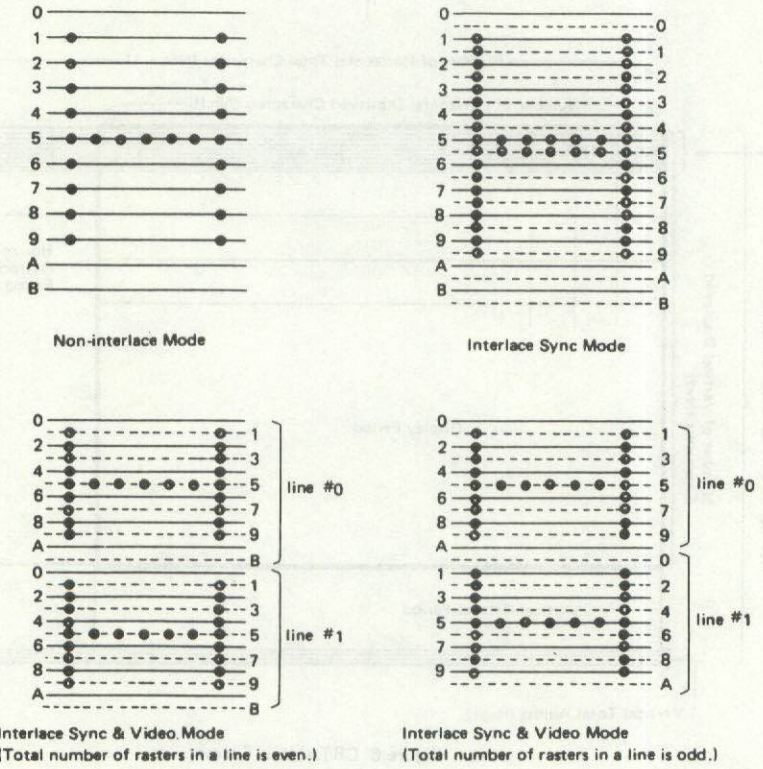


Figure 7 Example of Raster Scan Display

Interlace Sync & Video Mode Display

In interlace sync & video mode, the output raster address when the number of rasters is even is different from that when the number of rasters is odd.

Table 9 The Output of Raster Address in Interlace Sync & Video Mode

Total Number of Rasters in a Line \ Field		Even Field	Odd Field
Even		Even Address	Odd Address
Odd	Even Line*	Even Address	Odd Address
	Odd Line*	Odd Address	Even Address

* Internal line address begins from 0.

1) Total number of rasters in a line is even;

When number of rasters is programmed to be even, even raster address is output in the even field and odd raster address is output in the odd field.

2) Total number of rasters in a line is odd;

When total number of rasters is programmed to be odd, odd and even addresses are reversed according to the odd and even lines in each field. In this case, the difference in numbers of dots displayed between even field and odd field is usually smaller the case of 1). Then interlace can be displayed more stably.

[NOTE] The wide disparity of dots between number of dots between even field and odd field influences beam current of CRT. CRT, which has a stable high-voltage part, can make interlace display normal. On the contrary, CRT, which has unstable high-voltage part, moves deflection angle of beam current and also dots displayed in the even and odd fields may be shifted. Characters appears distroting on a border of the screen. So 2) programming has an effect to decrease such evil influences as mentioned above. Fig. 12 shows fine chart in each mode when interlace is performed.

- **Cursor Control**

Fig. 8 shows the display patterns where each value is programmed to the cursor start raster register and the cursor end raster register. Programmed values to the cursor start raster register and the cursor end raster register need to be under the following condition.

Cursor Start Raster Register $\leqq$ Cursor End Raster Register $\leqq$ Maximum Raster Address Register.

Time chart of CUDISP output signal is shown in Fig. 13 and Fig. 14.

■ INTERFACE TO DISPLAY CONTROL UNIT

Fig. 16 shows the interface between the CRTC and display control unit. Display control unit is mainly composed of Refresh Memory, Character Generator, and Video Control circuit. For refresh memory, 14 Memory Address line (0~16383) max are provided and for character generator, 5 Raster Address line (0~31) max are provided. For video control circuit, DISPTMG, CUDISP, HSYNC, and VSYNC signals are sent out. DISPTMG signal is used to control the blank period of video signal. CUDISP signal is used as video signal to display the cursor on the CRT screen. Moreover, HSYNC and VSYNC signals are used as drive signals respectively for CRT horizontal and vertical deflection circuits.

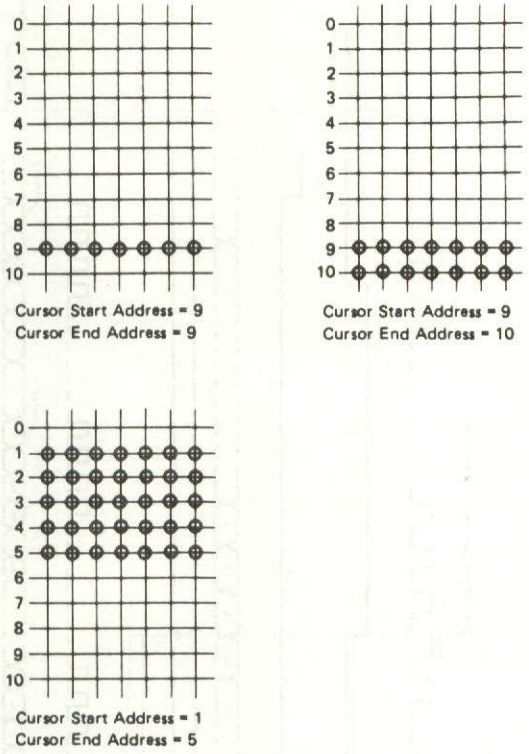


Figure 8 Cursor Control

Outputs from video control circuit, (video signals and sync signals) are provided to CRT display unit to control the deflection and brightness of CRT, thus characters are displayed on the screen.

Fig. 17 shows detailed block diagram of display control unit. This shows how to use CUDISP and DISPTMG signals. CUDISP and DISPTMG signals should be used being latched at least one time at external flip-flop F1 and F2. Flip-flop F1 and F2 function to make one-character delay time so as to synchronize them with video signal from parallel-serial converter. High-speed D type flip-flop as TTL is used for this purpose. After being delayed at F1 and F2 DISPTMG signal is AND-ed with character video signal, and CUDISP signal is OR-ed with output from AND gate. By using this circuitry, blanking of horizontal and vertical retrace time is controlled. And cursor video is mixed with character video signal.

Fig. 17 shows the example in the case that both refresh memory and CG can be accessed for horizontal one character time. Time chart for this case is shown in Fig. 20. This method is used when a few character needed to be displayed in horizontal direction on the screen.

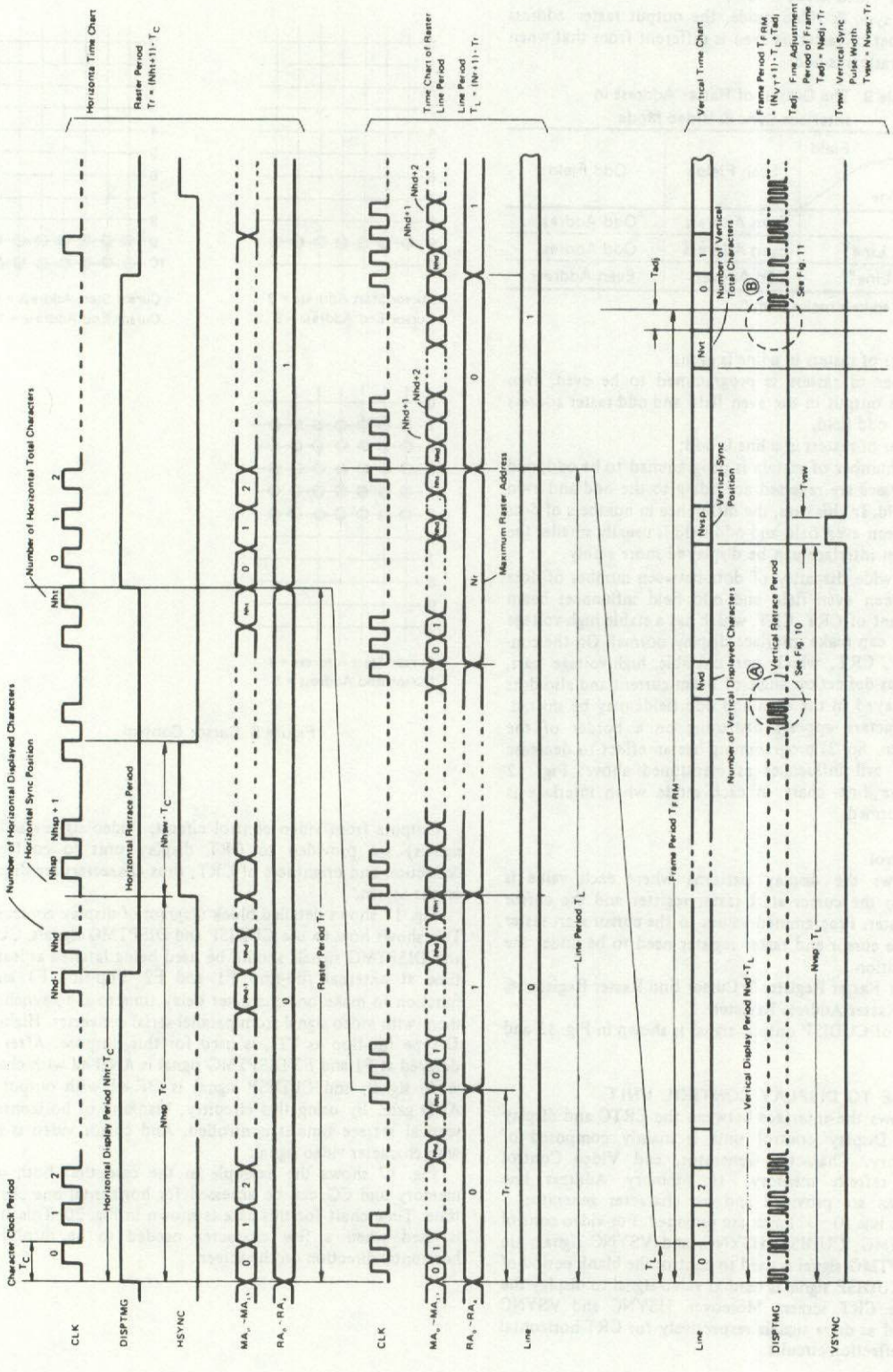


Figure 9 CRTC Time Chart

(Output waveform of horizontal & vertical display in the case where values shown in Table 8 are Programmed to each register.)

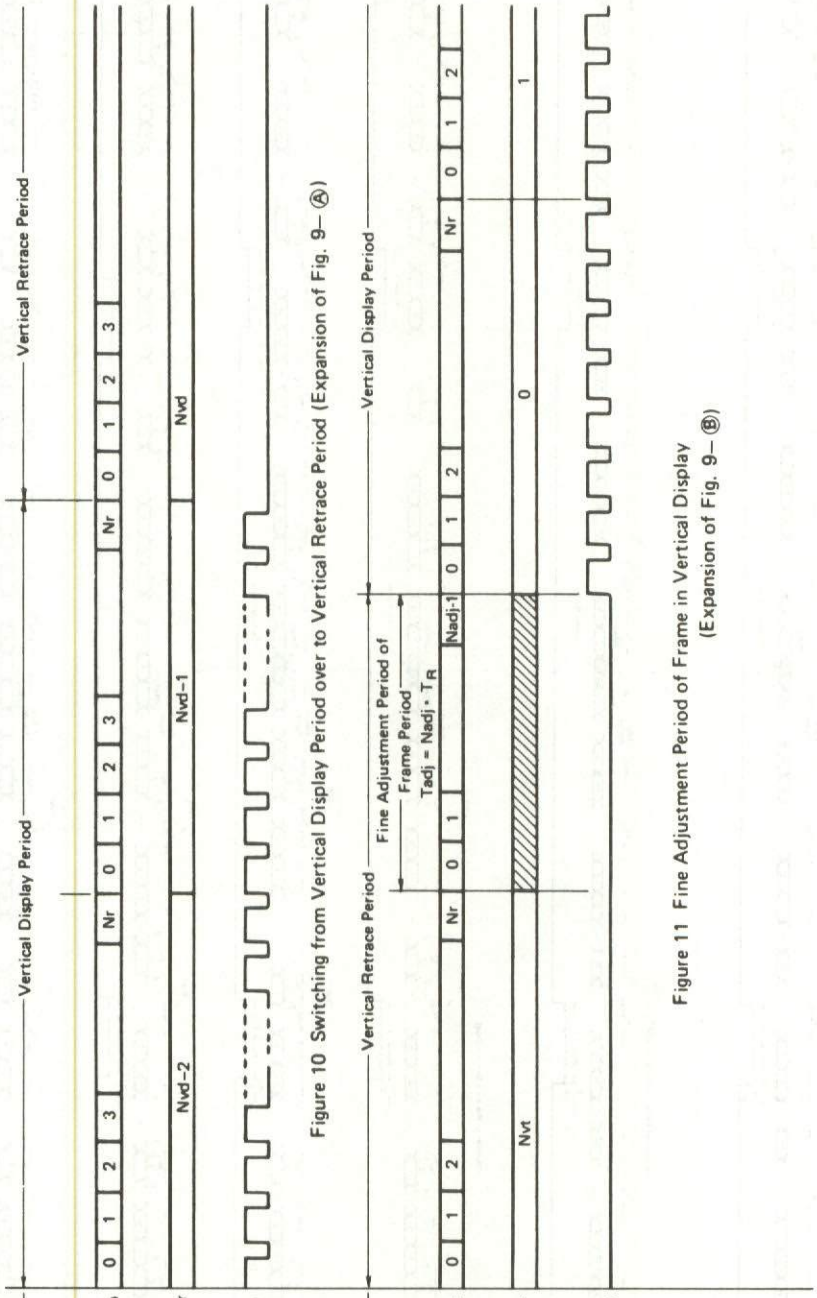


Figure 10 Switching from Vertical Display Period over to Vertical Retrace Period (Expansion of Fig. 9–Ⓐ)

Figure 11 Fine Adjustment Period of Frame in Vertical Display (Expansion of Fig. 9–Ⓑ)

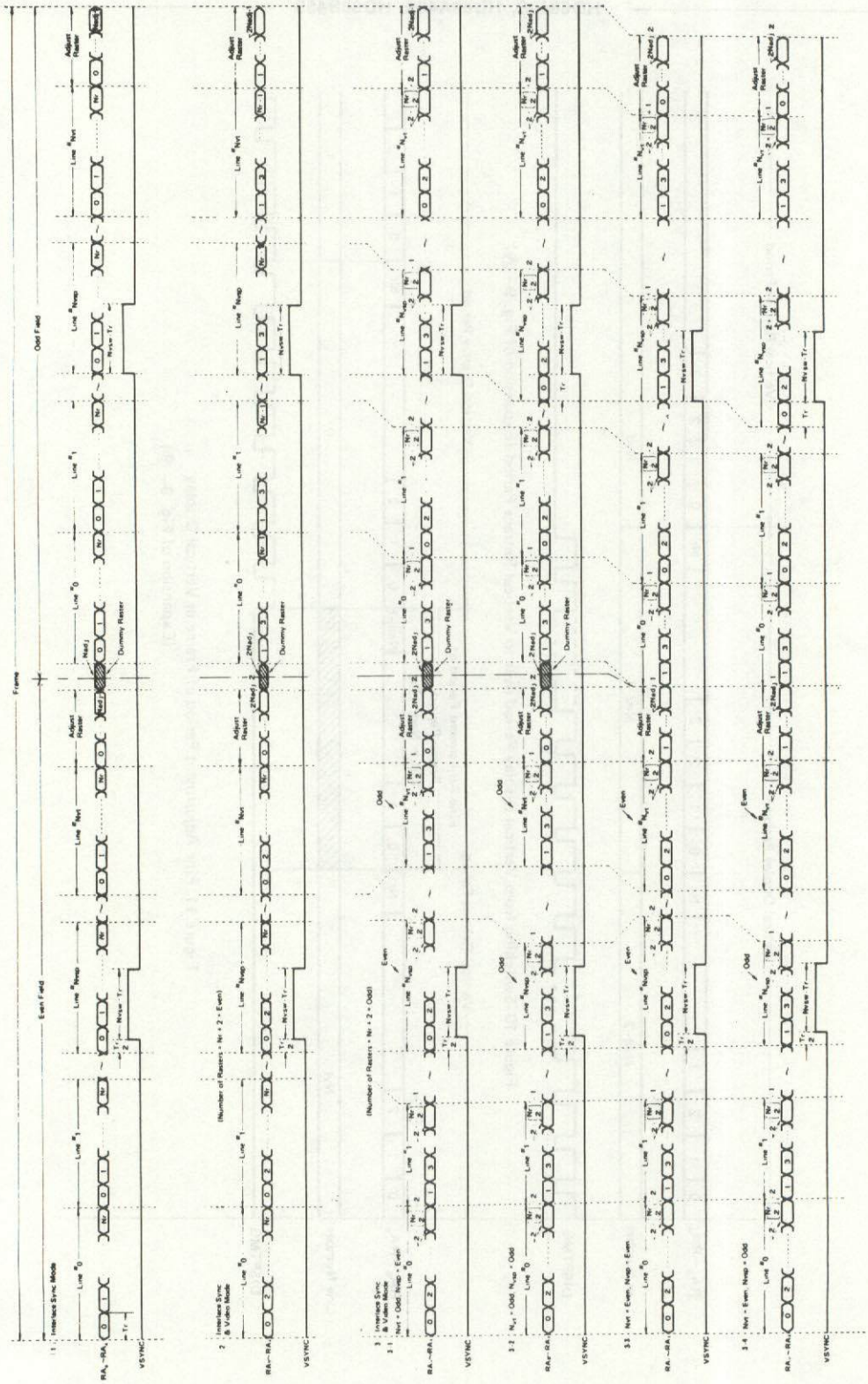


Figure 12 Interlace Control

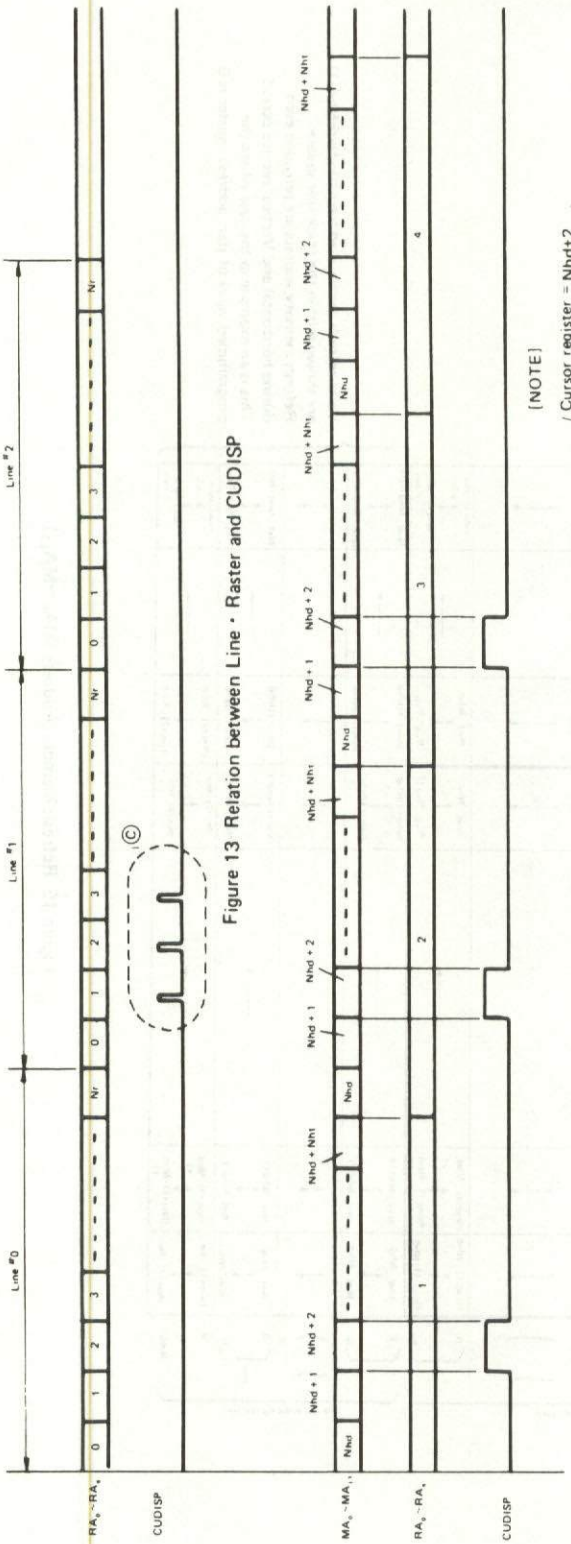


Figure 13 Relation between Line · Raster and CUDISP

[NOTE]

(Cursor register = Nhd+2
Cursor Start
Raster Register = 1
Cursor End
Raster Register = 3)
are Programmed in cursor display mode.

In blink mode, it is changed into display or non-display mode when field period is 16 or 32 time period.

Figure 14 CUDISP Output Timing (Exapnsion of Fig. 13-©)

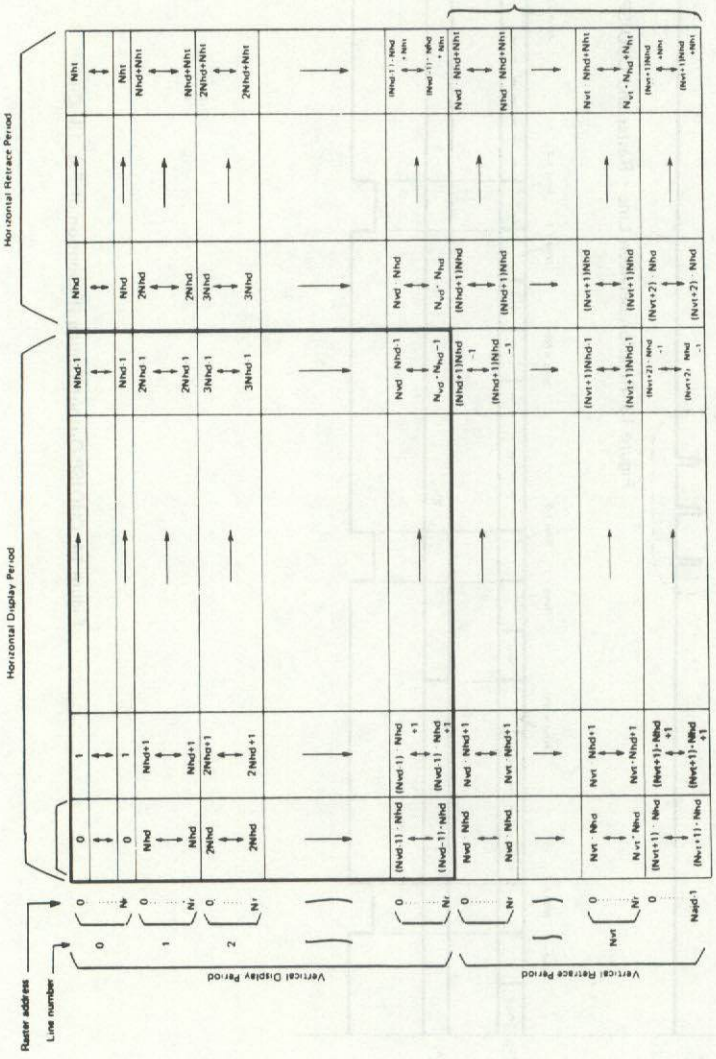


Figure 15 Refresh Memory Address (MA_0~MA_{13})

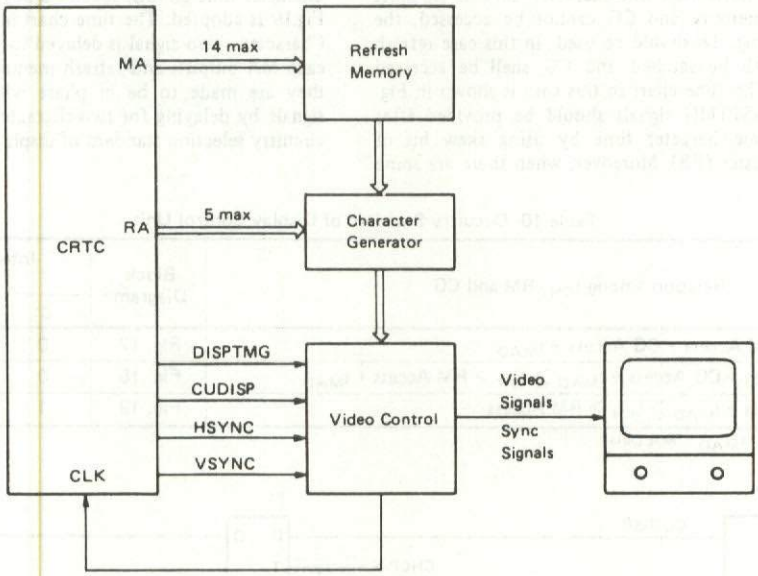


Figure 16 Interface to Display Control Unit

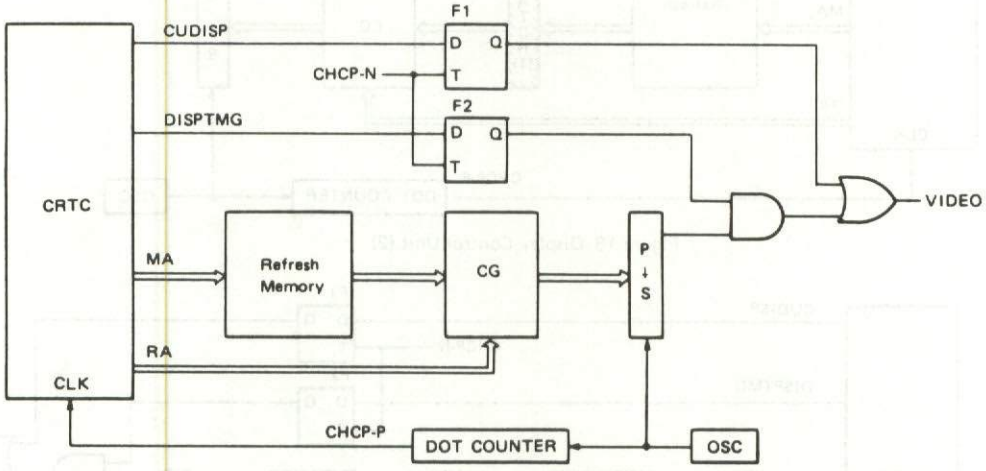


Figure 17 Display Control Unit (1)

When many characters are displayed in horizontal direction on the screen, and horizontal one-character time is so short that both refresh memory and CG cannot be accessed, the circuitry shown in Fig. 18 should be used. In this case refresh memory output shall be latched and CG shall be accessed at the next cycle. The time chart in this case is shown in Fig. 21. CUDISP and DISPTMG signals should be provided after being delayed by one-character time by using skew bit of interlace & skew register (R8). Moreover, when there are some troubles about delay time of MA during horizontal one-character time on high-speed display operation, system shown in Fig.19 is adopted. The time chart in this case is shown in Fig.22. Character video signal is delayed for two-character time because each MA outputs and refresh memory outputs are latched, and they are made to be in phase with CUDISP and DISPTMG signals by delaying for two-character time. Table 10 shows the circuitry selection standard of display units.

Table 10 Circuitry Standard of Display Control Unit

Case	Relation among t_{CH}, RM and CG	Block Diagram	Interlace & Skew Register Bit Programming			
			C1	C0	D1	D0
1	$t_{CH} >$ RM Access + CG Access + t_{MAD}	Fig. 17	0	0	0	0
2	RM Access + CG Access + $t_{MAD} \geqq t_{CH} >$ RM Access + t_{MAD}	Fig. 18	0	1	0	1
3	RM Access + $t_{MAD} \geqq t_{CH} >$ RM Access	Fig. 19	1	0	1	0

t_{CH} : CHCP Period; t_{MAD} : MA Delay

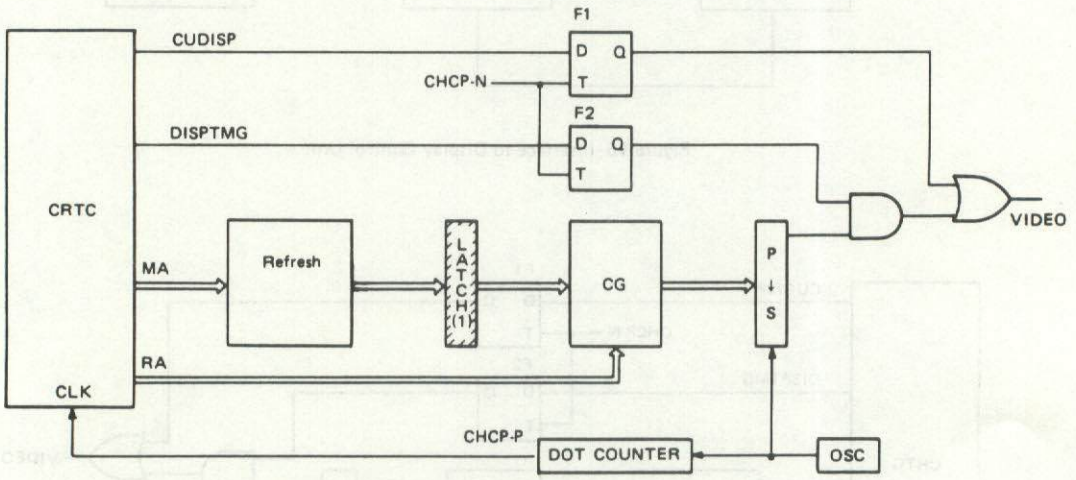


Figure 18 Display Control Unit (2)

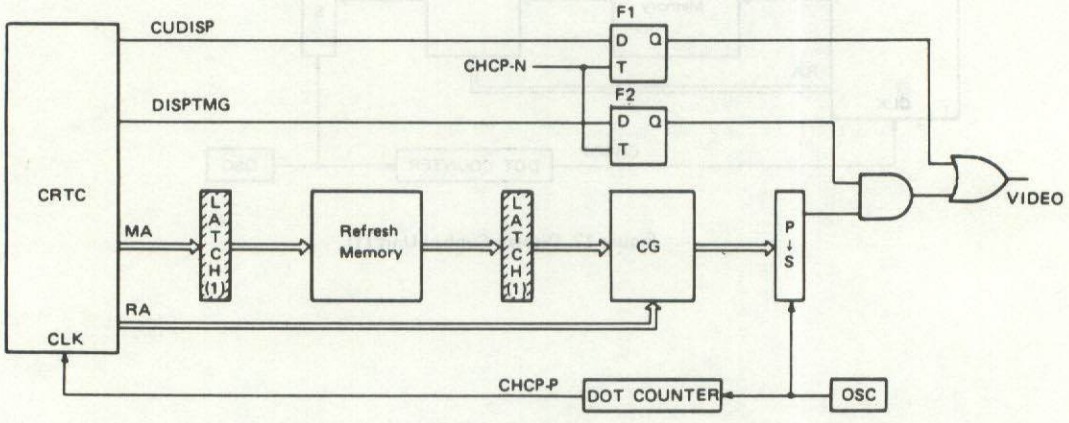


Figure 19 Display Control Unit (For high-speed display operation) (3)

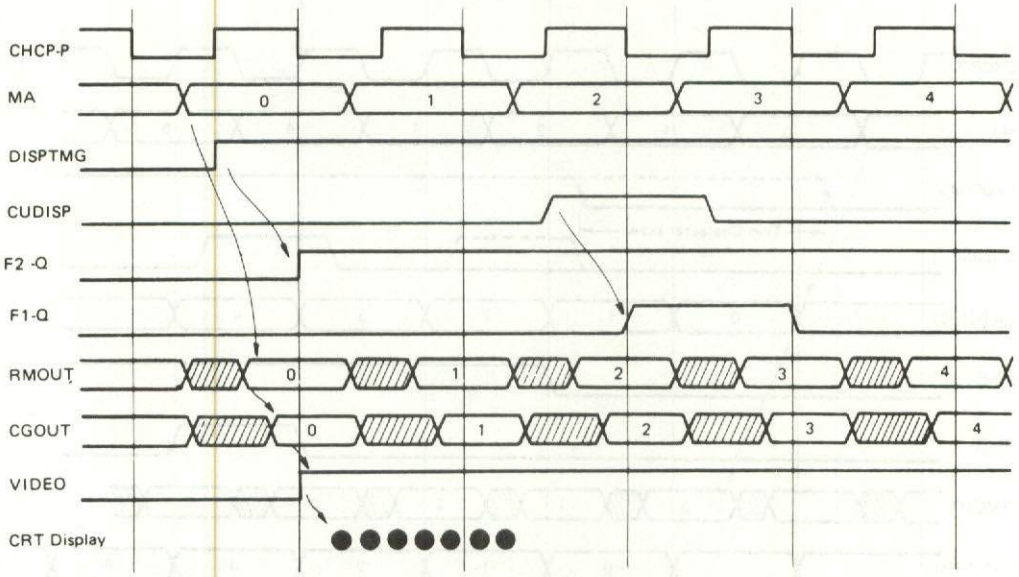


Figure 20 Time Chart of Display Control Unit (1)

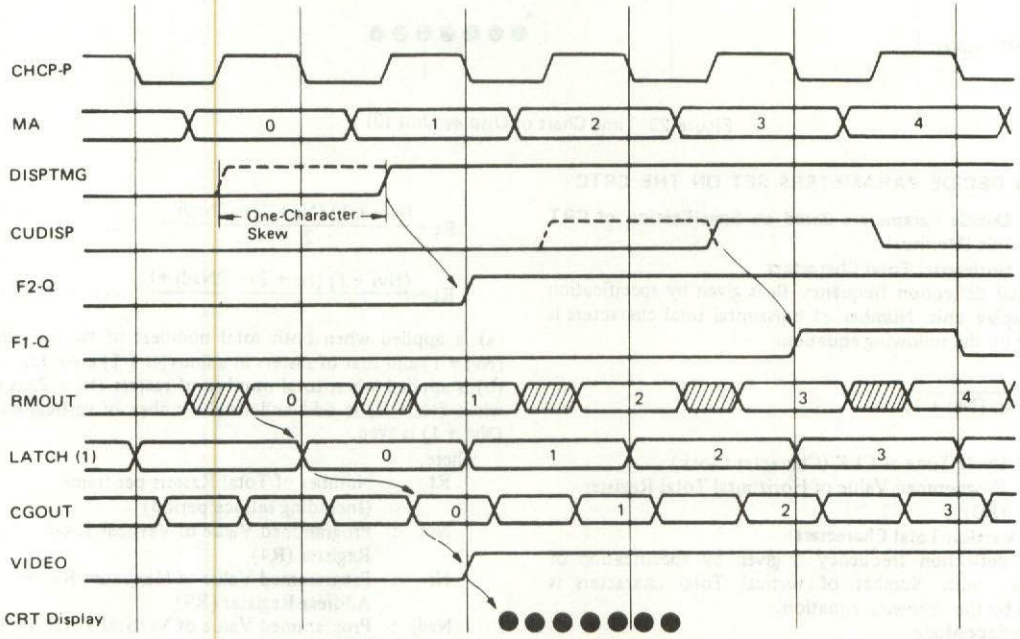


Figure 21 Time Chart of Display Control Unit (2)

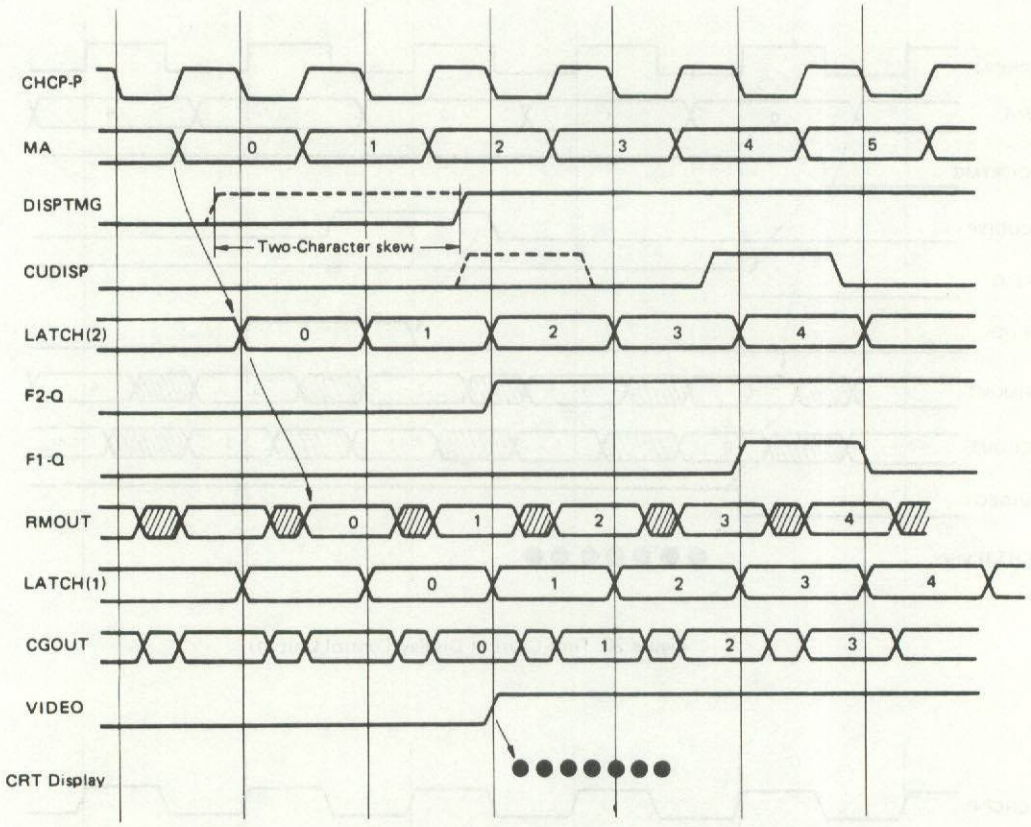


Figure 23 Time Chart of Display Unit (3)

■ HOW TO DECIDE PARAMETERS SET ON THE CRTC

• How to Decide Parameters Based on Specification of CRT Display Unit (Monitor)

Number of Horizontal Total Characters

Horizontal deflection frequency fh is given by specification of CRT display unit. Number of horizontal total characters is determined by the following equation.

$$fh = \frac{1}{t_C\,(Nht + 1)}$$

where,

t_C : Cycle Time of CLK (Character Clock)
Nht : Programmed Value of Horizontal Total Register (R0)

Number of Vertical Total Characters

Vertical deflection frequency is given by specification of CRT display unit. Number of vertical Total characters is determined by the following equation.

1) Non-interlace Mode
   Rt = (Nvt + 1) (Nr + 1) + Nadj
2) Interlace Sync Mode
   Rt = (Nvt + 1) (Nr + 1) + Nadj + 0.5
3) Interlace Sync & Video Mode

$$Rt = \frac{(Nvt + 1)(Nr + 2) + 2Nadj}{2} \quad \ldots\ldots\ldots\ldots \text{(a)}$$

$$Rt = \frac{(Nvt + 1)(Nr + 2) + 2Nadj + 1}{2} \quad \ldots\ldots\ldots\ldots \text{(b)}$$

(a) is applied when both total numbers of vertical characters (Nvt + 1) and that of rasters in a line (Nr + 2) are odd.
(b) is applied when total number of rasters (Nr + 2) is even, or when (Nr + 2) is odd and total number of vertical characters (Nvt + 1) is even.

where,

Rt : Number of Total Rasters per frame (Including retrace period)
Nvt : Programmed Value of Vertical Total Register (R4)
Nr : Programmed Value of Maximum Raster Address Register (R9)
Nadj : Programmed Value of Vertical Total Adjust Register (R5)

Horizontal Sync Pulse Width

Horizontal sync pulse width is programmed to low order 4-bit of horizontal sync width register (R3) in unit of horizontal character time. Programmed value can be selected within from 1 to 15.

Horizontal Sync Position

As shown in Fig. 24, horizontal sync position is normally selected to be in the middle of horizontal blank period. But there are some cases where its optimum sync position is not located in the middle of horizontal blank period according to specification of CRT. Therefore, horizontal sync position should be determined by specification of CRT. Horizontal sync pulse position is programmed in unit of horizontal character time.

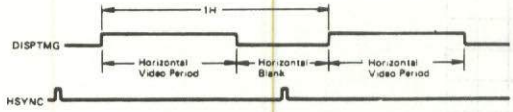


Figure 24 Time Chart of HSYNC

Vertical Sync Pulse Width

Vertical Sync Pulse Width is programmed to high order 4-bit of vertical sync pulse width register (R3) in unit of raster period. Programmed value can be selected within from 1 to 16.

Vertical Sync Position

As shown in Fig. 25, vertical sync position is normally selected to be in the middle of vertical blank period. But there are some cases where its optimum sync position is not located in the middle of vertical blank period according to specification of CRT. Therefore, vertical sync position should be determined by specification of CRT. Vertical sync pulse position is programmed to vertical sync position register (R7) in unit of line period.

- **How to Decide Parameters Based on Screen Format**

Dot Number of Characters (Horizontal)

Dot number of characters (horizontal) is determined by character font and character space. An example is shown in Fig. 26. More strictly, dot number of characters (horizontal) N is determined by external N-counter. Character space is set by means shown in Fig. 27.

Dot Number of Characters (Vertical)

Dot number of characters (vertical) is determined by characters font and line space. An example is shown in Fig. 26. Dot number of characters (vertical) is programmed to maximum raster address (register R9) of CRTC. When Nr is programmed

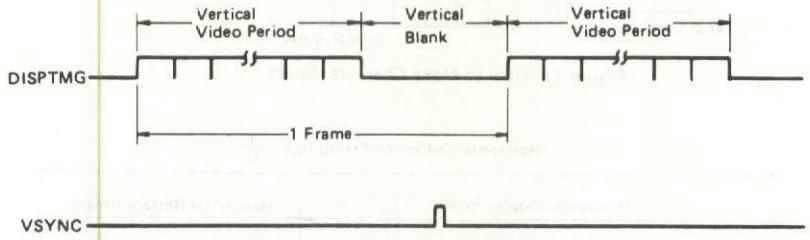


Figure 25 Time Chart of VSYNC

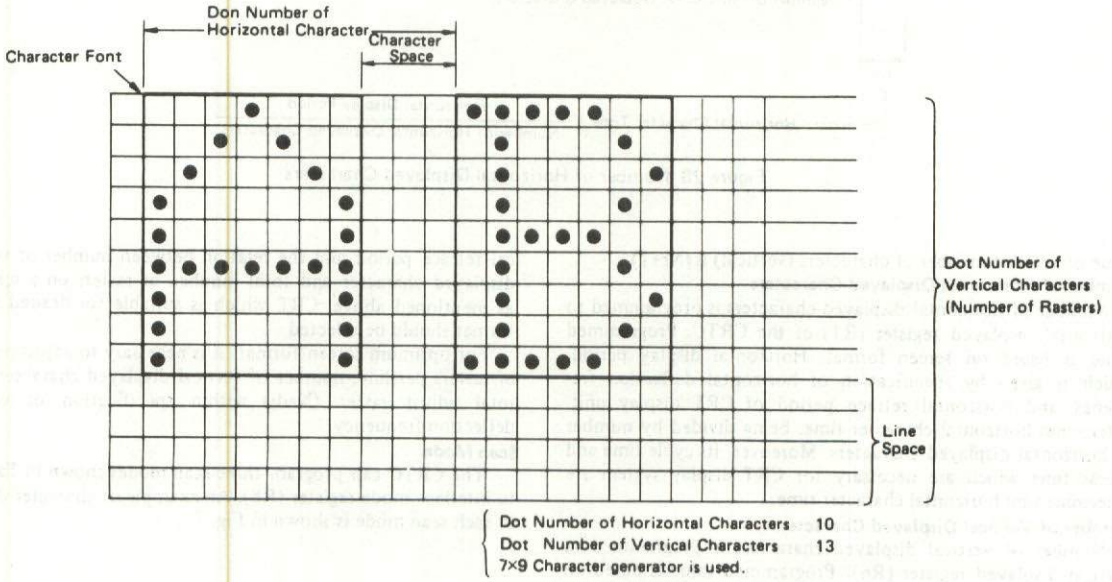


Figure 26 Dot Number of Horizontal and Vertical Characters

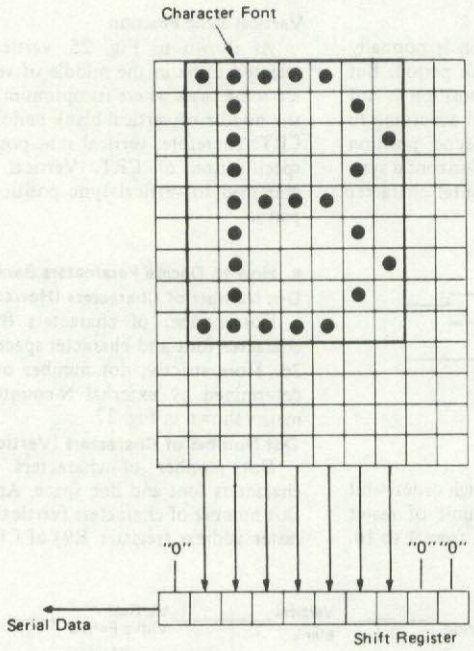


Figure 27 How to Make Character Space

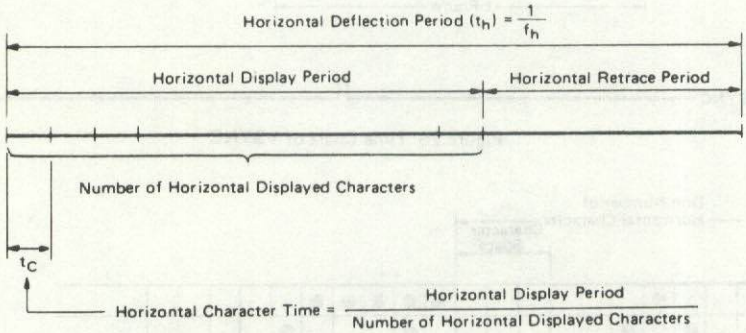


Figure 28 Number of Horizontal Displayed Characters

value of R9, dot number of characters (vertical) is (Nr+1).

Number of Horizontal Displayed Characters

Number of horizontal displayed characters is programmed to horizontal displayed register (R1) of the CRTC. Programmed value is based on screen format. Horizontal display period, which is given by specification of horizontal deflection frequency and horizontal retrace period of CRT display unit, determines horizontal character time, being divided by number of horizontal displayed characters. Moreover, its cycle time and access time which are necessary for CRT display system are determined by horizontal character time.

Number of Vertical Displayed Characters

Number of vertical displayed characters is programmed to vertical displayed register (R6). Programmed value is based on screen format. As specification of vertical deflection frequency of CRT determines number of total rasters (Rt) including vertical retrace period and the relation between number of vertical displayed character and total number of rasters on a screen is as mentioned above, CRT which is suitable for desired screen format should be selected.

For optimum screen format, it is necessary to adjust number of rasters per line, number of vertical displayed characters, and total adjust raster (Nadj) within specification of vertical deflection frequency.

Scan Mode

The CRTC can program three-scan modes shown in Table 11 to interlace mode register (R8). An example of character display in each scan mode is shown in Fig. 7.

Table 11 Program of Scan Mode

2^1	2^0	Scan Mode	Main Usage
0	0	Non-interlace	Normal Display of Characters & Figures
1	0		
0	1	Interlace Sync	Fine Display of Characters & Figures
1	1	Interlace Sync & Video	Display of Many Characters & Figures Without Using High-resolution CRT

[NOTE] In the interlace mode, the number of times per sec. in raster scanning on one spot on the screen is half as many as that in non-interlace mode. Therefore, when persistence of luminescence is short, flickering may happen. It is necessary to select optimum scan mode for the system, taking characteristics of CRT, raster scan speed, and number of displayed characters and figures into account.

Cursor Display Method

Cursor start raster register and cursor end raster register (R10, R11) enable programming the display modes shown in Table 7 and display patterns shown in Fig. 8. Therefore, it is possible to change the method of cursor display dynamically according to the system conditions as well as to realize the cursor display that meets the system requirements.

Start Address

Start address resisters (R12, R13) give an offset to the address of refresh memory to read out. This enables paging and scrolling easily.

Cursor Register

Cursor registers (R14, R15) enable programming the cursor display position on the screen. As for cursor address, it is not X, Y address but linear address that is programmed.

■ EXAMPLES OF APPLIED CIRCUIT OF THE CRTC

Fig. 30 shows an example of application of the CRTC to monochrome character display. Its specification is shown in Table 12. Moreover, specification of CRT display unit is shown in Table 13 and initializing values for the CRTC are shown in Table 14.

Table 12 Specification of Applied Circuit

Item	Specification															
Character Format	5 × 7 Dot															
Character Space	Horizontal : 3 Dot Vertical : 5 Dot															
One Character Time	1 μs															
Number of Displayed Characters	40 characters × 16 lines = 640 characters															
Access Method to Refresh Memory	Snychronous Method (DISPTMG Read)															
Refresh Memory	1 kB															
Address Map		2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	Refresh Memory	0	0	0	0	0	0	*	*	*	*	*	*	*	*	*	*
	CRTC Address Register	0	0	0	1	0	0	×	×	×	×	×	×	×	×	×	0
	CRTC Control Register	0	0	0	1	0	0	×	×	×	×	×	×	×	×	×	1
	× · · · don't care, * · · · 0 or 1																
Synchronization Method	HVSYNC Method															

Table 13 Specification of Character Display

Item	Specification
Scan Mode	Non-interlace
Horizontal Deflection Frequency	15.625 kHz
Vertical Deflection Frequency	60.1 Hz
Dot Frequency	8 MHz
Character Dot (Horizontal × Vertical)	8 × 12 (Character Font 5 × 9)
Number of Displayed Characters (Row × Line)	40 × 16
HSYNC Width	4 μs
VSYNC Width	3 H
Cursor Display	Raster 9 ~ 10, Blink 16 Field Period
Paging, Scrolling	Not used

Table 14 Initializing Values for Character Display

Register	Name	Symbol	Initializing Value Hex (Decimal)
R0	Horizontal Total	Nht	3F (63)
R1	Horizontal Displayed	Nhd	28 (40)
R2	Horizontal Sync Position	Nhsp	34 (52)
R3	Sync Width	Nvsw, Nhsw	34
R4	Vertical Total	Nvt	14 (20)
R5	Vertical Total Adjust	Nadj	08 (8)
R6	Vertical Displayed	Nvd	10 (16)
R7	Vertical Sync Position	Nvsp	13 (19)
R8	Interlace & Skew		00
R9	Maximum Raster Address	Nr	0B (11)
R10	Cursor Start Raster	B, P, NCSTART	49
R11	Cursor End Raster	NCEND	0A (10)
R12	Start Address (H)		00 (0)
R13	Start Address (L)		00 (0)
R14	Cursor (H)		00 (0)
R15	Cursor (L)		00 (0)

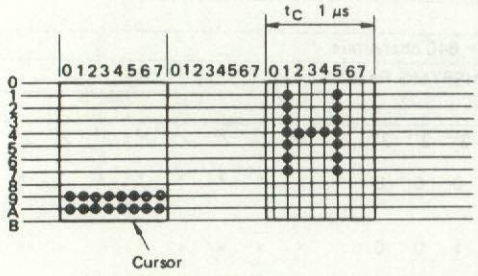


Figure 29 Non-interlace Display (Example)

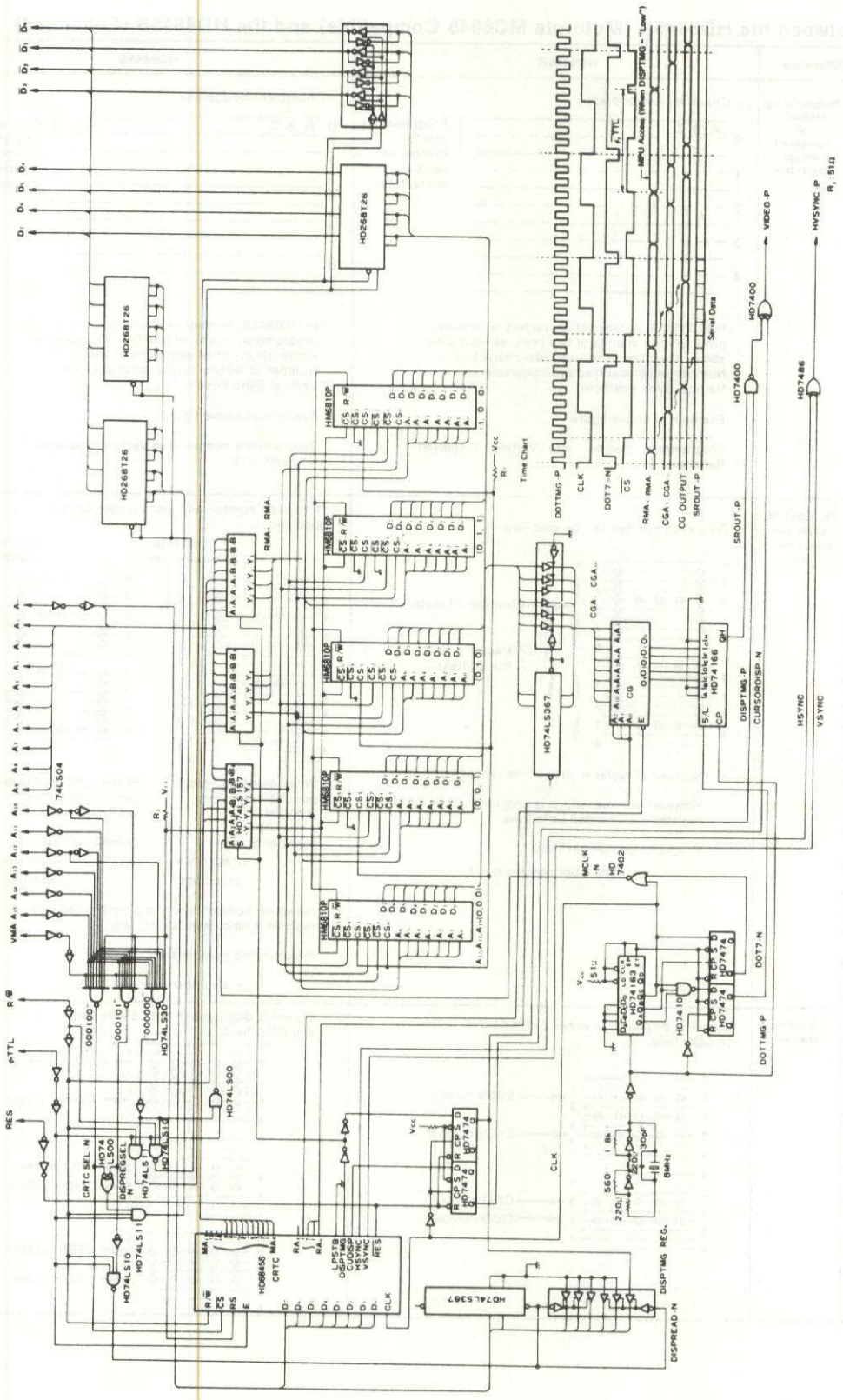
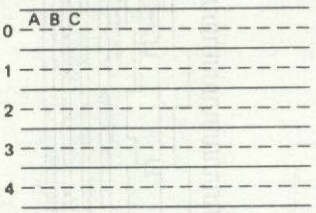
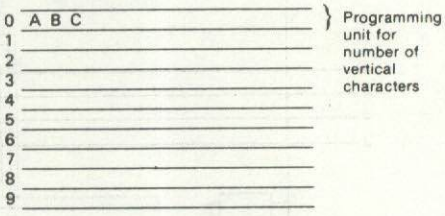
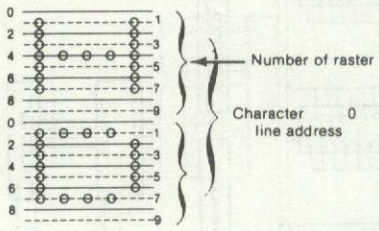
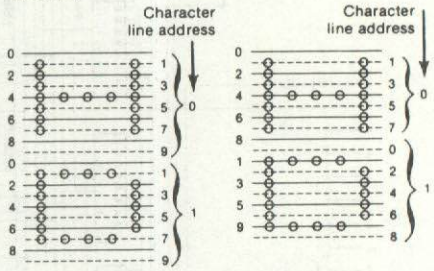
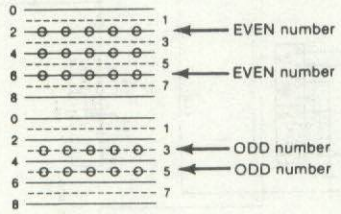
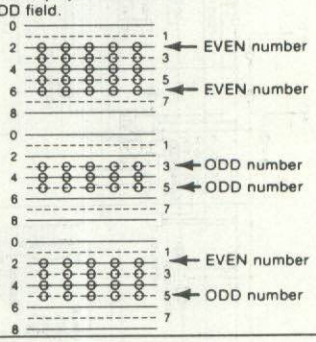
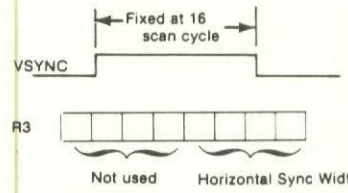
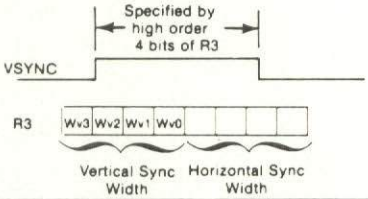
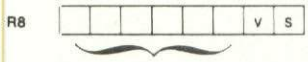
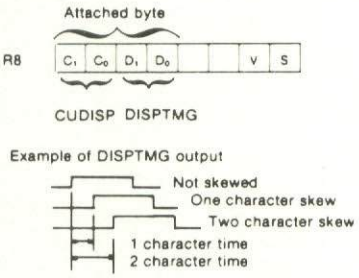


Figure 30 Example of Applied Circuit of the CRTC (Monochrome Character Display)

Differences between the HD6845R (Motorola MC6845 Compatible) and the HD6845S (Enhanced)

No.	Functional Difference		HD6845R	HD6845S
1	Interlace Sync & Video Mode Display	Programming Method of number of vertical characters	Character line address  In HD6845R, number of characters is vertically programmed in units of two lines, as illustrated above. (Number of vertical total characters, Number of vertical displayed characters, Vertical Sync Position) Example of above figure . . . Programmed number into Vertical Displayed Register = 5	Character line address  In HD6845S, number of characters is vertically programmed in unit of one line, as illustrated above. (Number of vertical total characters, Number of vertical displayed characters, Vertical Sync Position) Example of above figure . . . Programmed number into Vertical Displayed Register = 10
		Number of raster per character line	Only even number can be specified.  Number of raster = 10 scanline (specified) However, number which is programmed into register is calculated as follows. Programmed number (Nr) = (Number specified) − 1	Both even number and odd number can be specified.  When number of raster per character line is EVEN Number of raster = 10 scan line (specified) When number of raster per character line is ODD. Number of raster = 9 scan line (specified) However, number which is programmed into register is calculated as follows. Programmed number (NR) = (Number specified) − 2
		Cursor Display	Cursor is displayed in either EVEN field or ODD field. 	Cursor is displayed in both EVEN field and ODD field. 

No.	Functional Difference	HD6845R	HD6845S
2	Vertical Sync Pulse Width (VSYNC output)	Fixed at 16 raster scan cycle (16H) 	Programmable (1 - 16 raster scan cycle) 
3	SKEW Function	Not included 	SKEW capability is included in DISPTMG, CUDISP signals. 
4	Start Address Register	Write Only	Read or Write
5	RESET Signal (RES)	$MA_0 \sim M_{13}$ Output, $RA_0 \sim RA_4$ Output } -----Synchronous reset Other Outputs --------Asynchronous reset Output signals of $MA_0 \sim MA_{13}$, $RA_0 \sim RA_4$, synchronized with CLK "LOW" level, go to "LOW" level, after RES has gone to "LOW." Other outputs go to "LOW" immediately after RES has gone to "LOW" level.	$MA^\circ \sim MA_{13}$ Output, $RA_0 \sim RA_4$ Output, Other Outputs } ---- Asynchronous reset Output signals of $MA_0 \sim MA_{13}$, $RA_0 \sim RA_4$ and others go to "LOW" level immediately after RES has gone to "LOW" level.

AC Characteristic Differences between HD6845R (Motorola MC6845 Compatible) and HD6845S (Enhanced)

No.	Characteristic Difference	Symbol	HD46505R			HD46505S			Unit
			min.	typ.	max.	min.	typ.	max.	
1	Clock Cycle Time	$tcycc$	330	—	—	270	—	—	ns
2	Clock Pulse Width "High"	PW_{CH}	150	—	—	130	—	—	ns
3	Clock Pulse Width "Low"	PW_{CL}	150	—	—	130	—	—	ns
4	Rise and Fall Time for Clock Input	T_{CR}, T_{CF}	—	—	15	—	—	20	ns
5	Horizontal Sync Delay Time	T_{HSD}	—	—	250	—	—	200	ns
6	Light Pan Strobe Pulse Width	PW_{LPH}	80	—	—	60	—	—	ns
7	Light Pan Strobe, Uncertain Time of Acceptance	T_{LPD1}	—	—	80	—	—	70	ns
		T_{LPD2}	—	—	10	—	—	0	ns

SERVICE MODULE

Video Deflection/Driver Boards

Z-160 Personal Portable Computer

585-71-01

860-46

ZENITH data systems

The purpose of this page is to make sure that all service bulletins are entered in this manual. When a service bulletin is received, annotate the manual and list the information in the record below.

Record of Field Service Bulletins

SERVICE BULLETIN NUMBER	DATE OF ISSUE	CHANGED PAGE(S)	PURPOSE OF SERVICE BULLETIN	INITIALS

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Chapter 1

Introduction and Specifications

Introduction

This service module is designed to help the service technician troubleshoot and repair the video deflection and driver boards in the computer. A basic theory of operation and detailed circuit descriptions are given to assist in understanding the proper operation of the units. With knowledge of the normal operating characteristics of the boards, the technician should be able to successfully repair the board(s) in a minimum amount of time.

The video deflection and video driver boards produce the vertical and horizontal deflection voltages, the video output signal, and the high voltage required to produce a display on the cathode-ray tube (CRT) of the Z-160 Personal Portable Computer.

Specifications

Video	
Bandwidth:	18 MHz
Rise time:	20 ns maximum
Fall time:	23 ns maximum
Delay time:	25 ns maximum
Horizontal frequency:	15.697 KHz
Vertical frequency:	59.91 Hz
Input signal:	TTL compatible
Cathode-Ray Tube (CRT)	9″, amber phosphor
Nominal High Voltage	12 KVDC
Power Requirements	+12 VDC, 1.2 amps maximum

Chapter 2

Basic Theory of Operation

Refer to Figure 2.1 while reading the following.

NOTE: The following circuits are located on the video deflection board.

Vertical Circuitry Operation

The vertical oscillator (Q301 and Q302) is synchronized to the video information coming from the video logic card by the vertical sync signal from that same card. The oscillator output is then fed to a differential amplifier (Q303), which drives the base of the vertical driver (Q304). The vertical driver output is fed to a pair of complementary symmetry amplifiers (Q306 and Q307), which supply the necessary current to drive the vertical deflection yoke. The remaining transistor (Q308) is used to develop a fast vertical retrace signal needed to rapidly bring the electron beam back to the left side of the CRT for the beginning of the next vertical sweep cycle.

Horizontal Circuitry Operation

The horizontal oscillator (Q101, Q104, Q106, and Q107) is synchronized to the video information coming from the video logic card by the horizontal sync signal from that same card. The horizontal oscillator's output is then fed through an inverter (Q108), which drives the base of horizontal driver (Q102). The horizontal driver's output is then coupled through transformer TX101 to the base of the horizontal output transistor (Q103). Q103 develops the ramp voltage for the horizontal yoke through flyback transformer TX102. The display on the CRT is centered by the phase control (R103), and its width is adjusted by the width coil (LX101).

DC Power Supplies

The horizontal output stage, in conjunction with the flyback transformer, functions as an electronic switching power supply to develop the voltages for the anode, focus grid, and acceleration grid of the CRT. This is accomplished with low-voltage windings on the flyback, which are connected to rectifier and filter circuits. These circuits change the pulsed outputs of the flyback to DC voltages, which are used by other parts of the video circuitry.

Video Driver Circuitry

NOTE: The following circuit is contained on the video driver board.

The video signal coming from the video logic card is amplified to a level necessary to drive the cathode of the CRT by the video driver (Q402) and video output (Q401) stages.

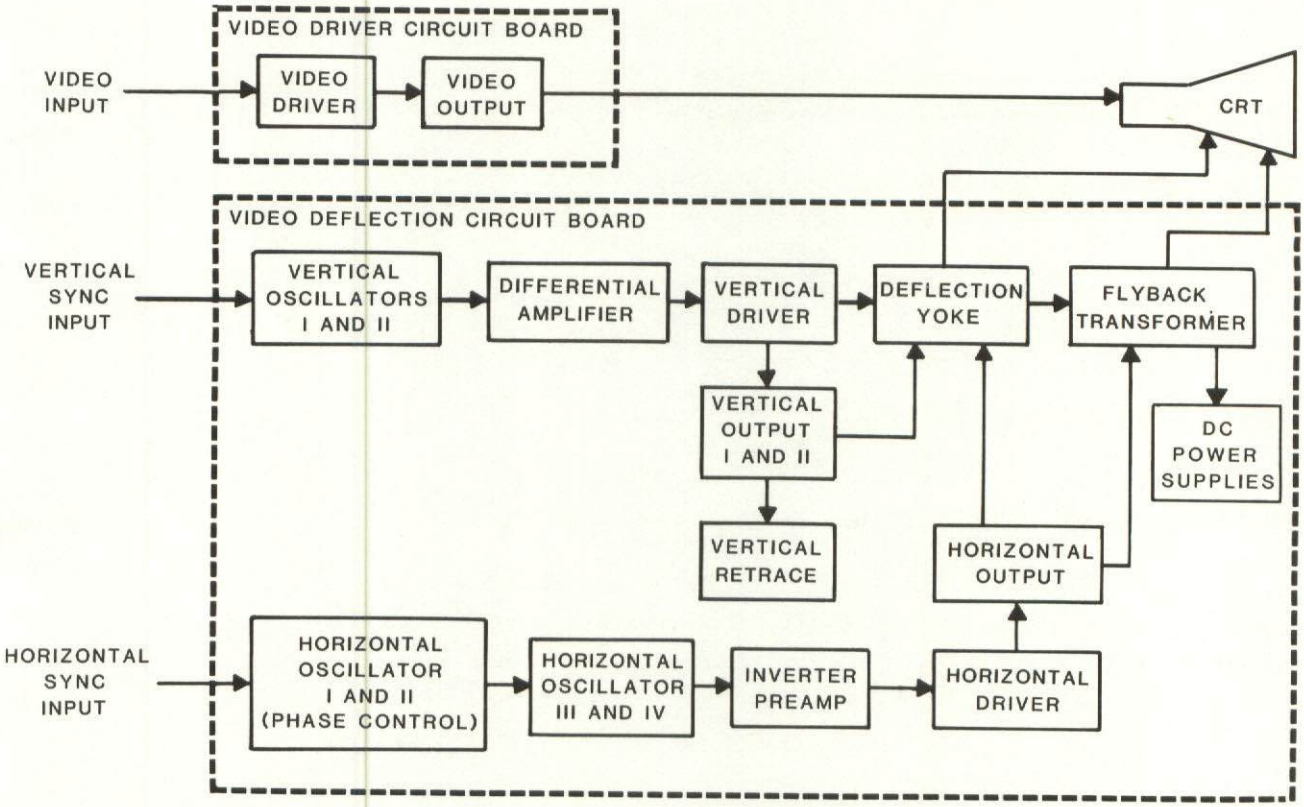


Figure 2.1. Overall Block Diagram

Chapter 3

Detailed Circuit Description

Introduction

This chapter provides detailed circuit descriptions of the video deflection and video driver boards. Before proceeding, read the "Basic Theory of Operation," Chapter 2, for an overall view of the video driver and video deflection circuits' operation.

Refer to the video deflection and video driver schematic for each of the following circuit descriptions.

Vertical Circuits

Capacitor C301 couples the vertical sync signal from the video logic board to synchronize vertical oscillator I and II (Q301 and Q302). Capacitor C303 shapes the 60 Hz output at the emitter of Q301 to help produce a linear sweep.

The shaped 60 Hz oscillator signal is applied to differential amplifier Q303, where the base is the inverting input and the emitter the non-inverting input. Feedback from the collector to the emitter is provided by resistor R319, providing good linearity.

The output of Q303 drives the vertical driver Q304, which in turn drives the complementary vertical amplifier I and II (Q306 and Q307).This stage develops the sweep current through the deflection yoke TX202A. Diodes CR302 and CR303 prevent crossover distortion. The RC network composed of R312, R313, R314, R316, R317, C308, and C309 sets the gain and frequency of the vertical amplifier.

The vertical retrace transistor Q308 generates a fast vertical retrace of 850 μs maximum for the vertical sweep. This occurs during the retrace period of the vertical scan.

Horizontal Circuits

Capacitor C101 couples the positive horizontal sync pulse from the video logic card to the base of Q101. Resistor R102 and capacitor C102 form an impedance matching network. Diode CR101 serves as a blocking diode, allowing only the positive signal to the base of Q101. Horizontal oscillator II (Q104) normally is conducting, biasing Q101 to an off state. The positive horizontal sync pulse turns Q101 on, cutting off Q104 at a point on the slope of the pulse determined by the phase shift network composed of R103, R104, and C103.

When Q104 cuts off, horizontal oscillator I (Q101) is cut off, turning Q104 on. This action produces an amplified sync pulse across capacitor C106 and blocking diode CR103 to the horizontal oscillator III and IV (Q106 and Q107). The horizontal oscillator outputs a 15.697 KHz horizontal frequency to inverter Q108. Diodes CR113 and CR114, and resistors R113, R114, R116, and R119 are discharge diodes and resistors. The output of Q108 is fed to the horizontal driver Q102. Resistor R123 and capacitor C114 form a wave shaping network. Driver output transformer TX101 couples the signal from the horizontal driver to the horizontal output transistor Q103. Resistor R128 prevents transformer ringing.

Horizontal Scan and Power Supplies

Transistor Q103 is used as an electronic switch which is on for approximately 60 to 70 percent of the horizontal scan period. Capacitor CX117 functions as a pseudo B+ for the horizontal deflection yoke TX202B. When Q103 is on, current flows out of CX117, through TX202B, LX102, LX101, and Q103 to ground. This action produces the right side of the scan. Inductor LX102 is a magnetically biased saturable reactor which provides left to right linearity. Inductor LX101 sets the horizontal scan width. The value of CX117 determines the parabolic waveform on the pseudo B+ which controls the center to edge linearity. The network composed of RX129, CR112, R131, and C118 provides suppression of spurious ringing which would cause black vertical lines at the left side of the raster.

When Q103 turns off, the resonant circuit of CX116 and LX101, LX102, and TX202B rings for one-half of a sine wave for a period of time equal to the LC time constant of the resonant circuit CX116 and LX101. This is the retrace pulse which moves the scanning beam from the left to the right side of the CRT, and also provides a high amplitude pulse for the auxiliary power supplies. Flyback transformer TX102 steps up the pulse to develop 12 KV of high voltage, and also steps down and inverts the pulse. The inverted pulse is rectified by CR111 to provide the video B+, clamped by C119 and CR107 to provide a negative voltage supply for the CRT, and rectified by CR106 to provide grid 2 bias for the CRT.

At the end of the retrace the sine wave goes negative, biasing the damper diode CR104 on. Current flowing through the yoke circuit into the damper diode provides the left side of the raster scan. The above scanning cycle then is repeated.

The 12 volts for the horizontal scan is fed through diode CR109 into a tap on TX102, where transformer action increases the voltage to 20 volts for the pseudo B+ necessary for the horizontal deflection.

The positive pulse from Q103 saturates the flyback transformer TX102 and charges CX117 through width coil LX101, linearity coil LX102, and horizontal deflection yoke TX202B. When Q103 turns off, the magnetic field of TX102 collapses, generating the acceleration voltage to the CRT through an internal rectifier diode. Diode CR106 rectifies the focus voltage, charging C129 to a static level. Diode CR107 is the charge path for C126, which develops the brightness voltage for the CRT. Diode CR104 and CX116 form a damper network to eliminate the ringing effect of flyback transformer TX102. Width coil LX101 and linearity coil LX102 modify the sawtooth waveform generated by TX102, to provide a linear horizontal display.

Resistors RX129 and R131, diode CR112, and capacitor C118 form an arc suppression network for the horizontal yoke winding. This network protects the horizontal driving circuits from the inductive spike which is generated when the magnetic field in the yoke assembly collapses. Diode CR111, capacitor C122, and resistor R132 rectify and filter the output of the flyback transformer's secondary winding to generate the +45 VDC supply voltage. Resistor RX130 is a current limiting resistor for the secondary circuit.

Video Amplifier

Video driver Q402 and video output Q401 transistors are connected in cascade to form the video amplifier. This circuit provides high gain, low noise, and low input and output capacitance. The video signal from the video logic card is applied to the base of Q402. This causes transistors Q401 and Q402 to conduct, driving the CRT cathode more negative, thereby producing the white information for the video display. Resistor R412 determines the overall stage gain, while capacitor C403 and resistor R413 determine the frequency response.

Chapter 4

Service and Troubleshooting

Introduction

This chapter contains information on servicing the video deflection and video driver boards of the Z-160 Personal Portable Computer. The technician should verify that a problem has been isolated to the video deflection and video driver boards before attempting to service them.

Test Equipment

The following is a listing of recommended test equipment for this unit.

- **Oscilloscope** — DC to 5 MHz, triggered sweep. Heath Model IO-4105 or equivalent.
- **Voltmeter** — High input impedance, 0 to 1000 volts, 0 to 1 megohm. Heath Model IM-2215 or equivalent.
- **Low-Capacitance 10X Oscilloscope Probe** — 10 megohm input impedance. Heath Model PK-1 or equivalent.
- **High Voltage Probe** — 0 to 30 KV. Heath Model IMA-100-10 or equivalent.

Adjustments

In many instances, a simple adjustment may be all that is necessary to correct a problem with a circuit. Before you begin to troubleshoot a circuit, try to correct the problem by performing the service adjustments.

Video Deflection Board Adjustments

Refer to Figure 4.1 and perform the following adjustments:

NOTE: The adjustment procedures assume that the video deflection board and video driver board are installed in the computer and are functioning properly.

Horizontal Phase Control

Adjust the horizontal PHASE control (R103) to bring the video information into the center of the display.

Brightness Control

Adjust the BRITE control (R139) to a level where the raster is barely visible.

Vertical Size Control

Adjust the VERT SIZE control (R312) as required to provide normal screen height.

Horizontal Width Control

Adjust the HORIZ WIDTH control (LX101) as required to provide normal screen width.

Focus Control

Adjust the FOCUS control (R148) until the video has maximum clarity of detail.

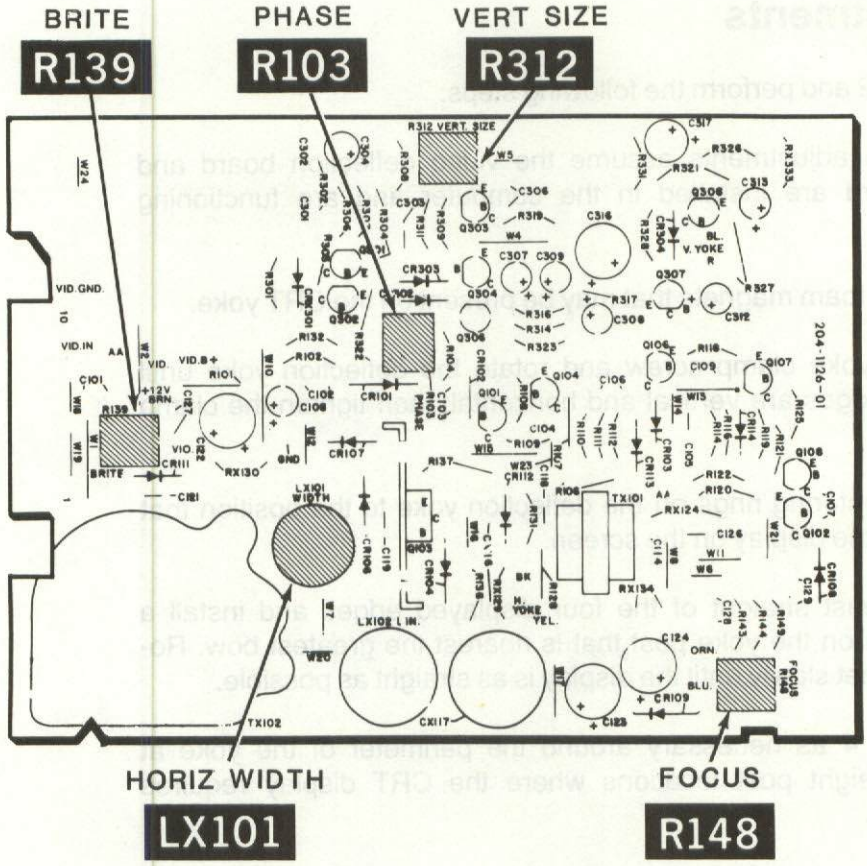


Figure 4.1. Service Adjustments

Yoke Adjustments

Refer to Figure 4.2 and perform the following steps:

NOTE: The yoke adjustments assume the video deflection board and video driver board are installed in the computer and are functioning properly.

1. Remove any foam magnets that may be present on the CRT yoke.

2. Loosen the yoke clamp screw and rotate the deflection yoke until the display edges are vertical and horizontal; then tighten the clamp screw.

3. Adjust the centering rings on the deflection yoke to the position that best centers the display on the screen.

4. Select the least straight of the four displayed edges and install a foam magnet on the yoke post that is nearest the greatest bow. Rotate the magnet slowly until the display is as straight as possible.

5. Repeat step 4 as necessary around the perimeter of the yoke at any of the eight post locations where the CRT display requires straightening.

NOTE: If only a small effect is desired, reduce the size of the foam magnets by cutting off a corner with diagonal cutters.

6. After making all adjustments, note that the display is a uniform rectangular shape.

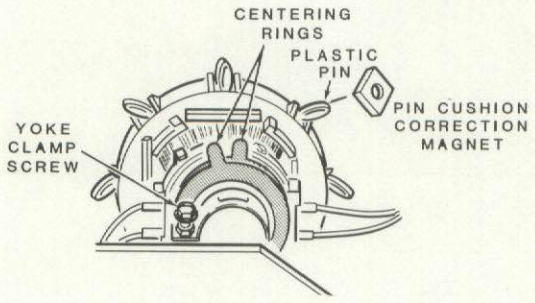


Figure 4.2. CRT Yoke Adjustments

Testing and Troubleshooting

The testing and troubleshooting contained in this chapter consists of general procedures, and specific procedures for the video deflection board, and the video driver board.

General Troubleshooting

Refer to Table 4.1 for general troubleshooting.

Table 4.1. General Troubleshooting

PROBLEM	POSSIBLE CAUSE
No video or raster on CRT screen	Power supply module
No video data on CRT screen	Q401, Q402
No vertical deflection	Q304, Q306, Q307
No vertical sync	Q301, Q302
No horizontal deflection	Q102, Q103, TX102
No horizontal sync	Q101, Q104
Horizontal phasing out	Q101, Q104
No high voltage CRT anode	TXl02, TX202
Narrow raster on screen	Q106, Q107, Q108, Q103
Only top and bottom of vertical raster present	Q304, Q306, Q307, TX202A
Vertical retrace lines visible	Q308

Video Deflection Board Troubleshooting

Refer to Tables 4.2 and 4.3, and the waveforms in Figures 4.3 through 4.5 for video deflection board troubleshooting.

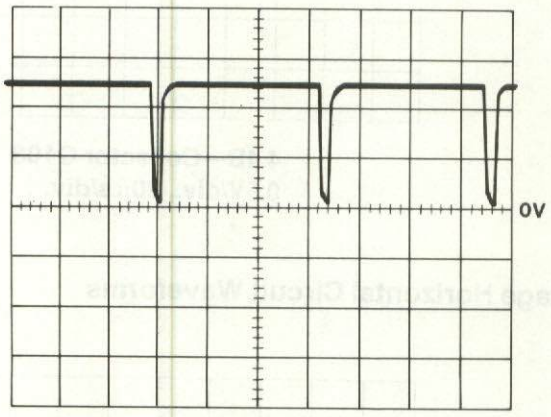
Table 4.2. Video Deflection Board Troubleshooting

PROBLEM	POSSIBLE CAUSE
No raster	1. Check high voltage at anode of CRT 2. Check Q1O2, Q1O3, CR1O4, TX2O2A, TX202B, R128, Q3O1, Q3O2
Raster present on CRT (no video)	1. Q4O1, Q4O2, VX1O1, CR4O1 2. CR111, CRT socket
No vertical deflection	1. R139, Q3O1, Q3O2, Q3O6, Q3O7
Vertical oscillator off frequency	1. Q3O1, Q3O2, C3O3
No vertical sync	1. C3O2, CRX3O1, C3O1, R3O1
Horizontal oscillator off frequency	1. Q1O6, Q107, Q1O8
No horizontal sync	1. Q1O1, R1O1, C1O1, R1O2, CR1O1
Horizontal phasing incorrect	1. Q1O1, Q1O4, C1O3, R1O4, R1O5 2. R1O7, R1O3
Poor horizontal linearity or foldover	1. TX1O1, LX1O1, LX1O2 2. CR1O4, TX2O2B, Q1O6, Q1O7 3. Q1O8, Q1O3, Q1O2
Narrow raster on screen	1. Q1O6, Q1O7, Q1O8, Q1O3 2. CR1O4, LX1O1, CR111

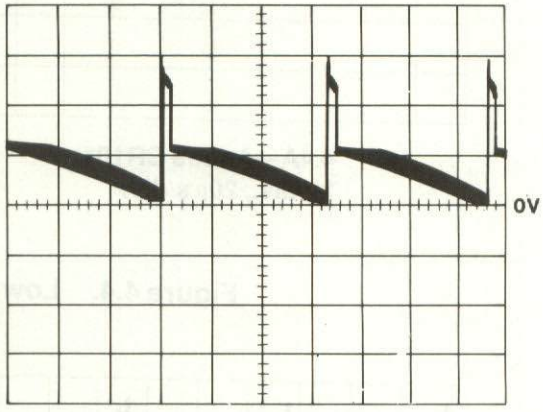
Video Deflection Board Waveforms

Use the color bar display available from the MFM-150 menu to obtain the following waveforms. To generate the color bars, turn on the computer, then simultaneously press the **Ctrl**, **Alt**, and **Del** keys. When the MFM-150 sign-on message appears, press **C** then **RETURN**.

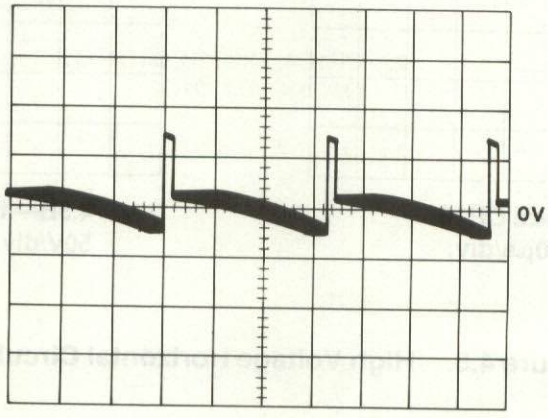
The waveforms are taken with the oscilloscope triggered at the beginning of the vertical sync pulse for vertical measurements, and the beginning of the horizontal sync pulse for horizontal measurements. The vertical channel should be set at DC coupling with the base line set at the center of the graticule.



4.3A—Junction R301 and C301
Scope set at 2V/div., 5ms/div.

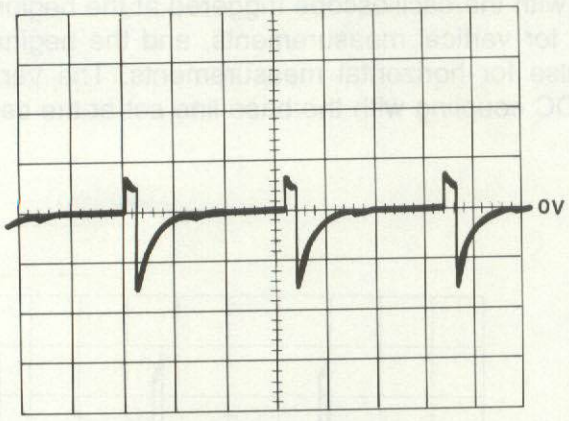


4.3B—Emitter Q307
Scope set at 10V/div., 5ms/div.

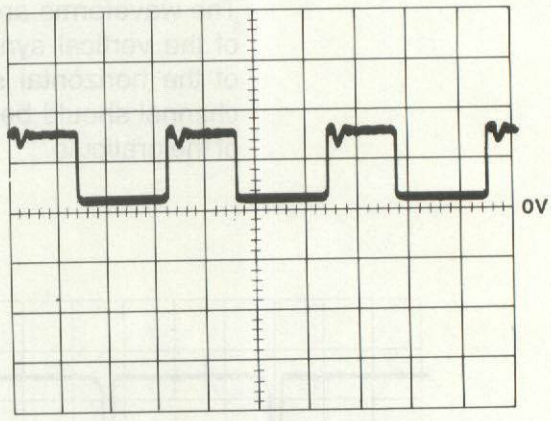


4.3C—Base Q308
10V/div., 5ms/div.

Figure 4.3. Vertical Circuit Waveforms

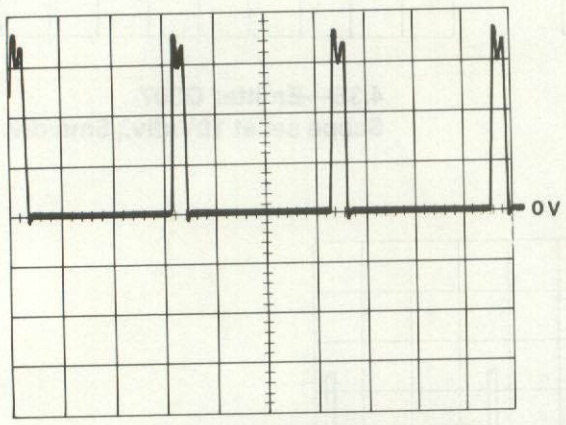


4.4A—Anode CR101
2V/div., 20μs/div.

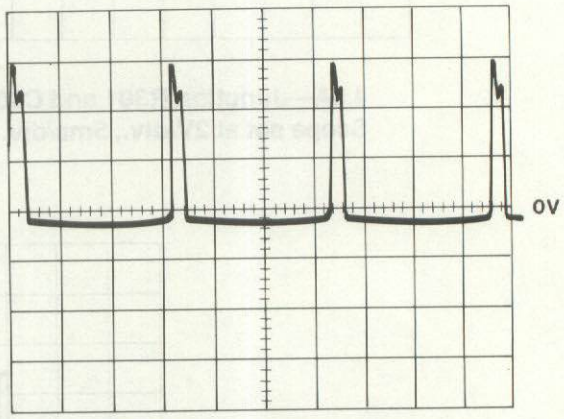


4.4B—Collector Q108
0.5V/div., 20μs/div.

Figure 4.4. Low Voltage Horizontal Circuit Waveforms



4.5A—Anode CR106
50V/div., 20μs/div.



4.5B—Yoke, pin #2 (yellow wire)
50V/div., 20μs/div.

Figure 4.5. High Voltage Horizontal Circuit Waveforms

Transistor Voltage Measurements

Refer to Table 4.3 for transistor voltage measurements on the video deflection board.

Table 4.3. Transistor Voltage Measurements (Video Deflection)

TRANSISTOR	EMITTER	BASE	COLLECTOR
Q101	0	0.7 V	3.0 V
Q102	0	0.8 V	9.0 V
Q103	0	0.7 V	15.0 V
Q104	0	0.7 V	3.0 V
Q106	0	0.7 V	3.0 V
Q107	0	0.7 V	3.0 V
Q301	7.26 V	7.0 V	8.35 V
Q302	8.78 V	8.62 V	6.99 V
Q303	7.72 V	7.3 V	0.32 V
Q304	0	0.31 V	9.0 V
Q306	9.44 V	9.0 V	0
Q307	10.24 V	10.64 V	0
Q308	6.0 V	6.84 V	17.15 V

NOTE: Reference for measurements: video deflection board ground.

Video Driver Board Troubleshooting

Refer to Tables 4.4 and 4.5 for video driver board troubleshooting.

Transistor Voltage Measurements

Table 4.4 lists the transistor voltage measurements on the video driver board.

Table 4.4. Transistor Voltage Measurements (Video Driver)

TRANSISTOR	EMITTER	BASE	COLLECTOR
Q401	.03 V	0	6.5 V
Q402	6.50 V	7.20 V	50.0 V

NOTE: Reference for measurements: video driver board ground.

CRT Voltage Measurements

Refer to Table 4.5 for CRT voltage measurements on the video driver board.

Table 4.5. CRT Voltage Measurements (Video Driver)

PIN	VOLTAGE
1	−50 to +12 V
2	50 V
3	12 V
4	0
5	−50 to +12 V
6	+500 V
7	−50 to +400 V

NOTE: Measure 12.5 KV at CRT anode, using high voltage probe.

Chapter 5

Parts List

Introduction

This portion of the service module contains component views of the video deflection board, video driver board, and related parts lists. Refer to Figures 5.1 and 5.2 for location of parts and components.

Video Deflection Board Parts List

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
Capacitors		
C101	HE 21-789	330 pF ceramic
C102	HE 21-750	56 pF ceramic
C103	HE 234-512	.001 µF polyester
C104	HE 21-750	56 pF ceramic
C105	HE 234-512	.001 µF polyester
C106	HE 234-405	560 pF ceramic
C107	HE 234-406	.022 µF ceramic
C108	HE 25-898	33 µF electrolytic
C109	HE 234-512	.001 µF polyester
C110	Not used	
C111	Not used	
C112	Not used	
C113	Not used	
C114	HE 21-47	.01 µF ceramic
C115	Not used	
C116	Not used	
C117	Not used	
C118	HE 234-406	.022 µF ceramic
C119	HE 21-43	.001 µF ceramic, 1 KV
C120	Not used	
C121	HE 21-43	.001 µF ceramic, 1 KV
C122	HE 25-882	22 µF electrolytic
C123	HE 25-942	220 µF electrolytic
C124	HE 25-942	220 µF electrolytic
C125	Not used	
C126	HE 27-74	.01 µF polyester
C127	Not used	
C128	Not used	
C129	HE 21-43	.001 µF ceramic, 1 KV
C316	HE 25-905	470 µF electrolytic
C317	HE 25-942	220 µF electrolytic
CX116	HE 234-513	.022 µF polypropylene
CX117	HE 234-514	10 µF non-polarized

Parts List

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
Connector		
P101	HE 234-519	10-pin plug
Diodes		
CR101	HE 234-299	103-142
CR102	Not used	
CR103	HE 234-299	103-142
CR104	HE 234-264	103-298
CR105	Not used	
CR106	HE 234-526	103-323
CR107	HE 234-353	103-295
CR108	HE 6-104	100 KΩ resistor, 1/2 watt
CR109	HE 234-521	103-339
CR110	Not used	
CR111	HE 234-526	103-323
CR112	HE 234-267	103-254
CR113	HE 234-299	103-142
CR114	HE 234-299	103-142
CR301	Not used	
CR302	HE 234-299	103-142
CR303	HE 234-299	103-142
CR304	HE 234-267	103-254
CRX301	HE 234-266	103-279
Inductors/Transformers		
LX101	HE 234-510	Width coil
LX102	HE 234-509	Linearity coil
TX101	HE 234-350	Horizontal driver
TX102	HE 234-262	Sweep transformer
TX202	HE 234-520	Deflection yoke

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
Resistors		
NOTE: All resistors are 1/4 watt unless otherwise specified.		
R101	HE 6-153-12	15 KΩ
R102	HE 6-561-12	560 Ω
R103	HE 234-515	2.5 KΩ (PHASE control)
R104	HE 6-223-12	22 KΩ
R105	Not used	
R106	HE 6-102-12	1 KΩ
R107	HE 6-683-12	68 KΩ
R108	HE 6-103-12	10 KΩ
R109	HE 6-223-12	22 KΩ
R110	HE 6-102-12	1 KΩ
R111	HE 6-103-12	10 KΩ
R112	HE 6-102-12	1 KΩ
R113	Not used	
R114	HE 6-4322-12	43.2 KΩ
R115	Not used	
R116	HE 6-4752-12	47.5 KΩ
R117	Not used	
R118	HE 6-101-12	100 Ω
R119	HE 6-102-12	1 KΩ
R120	HE 6-122-12	1.2 KΩ
R121	HE 6-183-12	18 KΩ
R122	HE 6-361-12	360 Ω
R123	Not used	
R124	Not used	
R125	HE 6-103-12	10 KΩ
R126	Not used	
R127	Not used	
R128	HE 6-820-12	82 Ω
R129	Not used	
R130	Not used	

Parts List

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
Resistors (continued)		
R131	HE 6-681-12	680 Ω
R132	HE 6-153-12	15 KΩ
R133	Not used	
R134	Not used	
R135	Not used	
R136	Not used	
R137	HE 6-223-12	22 KΩ
R138	HE 6-104-12	100 KΩ
R139	HE 234-516	100 KΩ (BRITE control)
R140	Not used	
R141	Not used	
R143	Not used	
R144	HE 6-105-12	1 MΩ
R145	Not used	
R146	Not used	
R147	Not used	
R148	HE 234-518	2 MΩ (FOCUS control)
R149	Not used	
R150	Not used	
R301	HE 6-103-12	10 KΩ
R302	HE 6-223-12	22 KΩ
R303	HE 6-204-12	200 KΩ
R304	HE 6-470-12	47 Ω
R305	Not used	
R306	HE 6-223-12	22 KΩ
R307	HE 6-622-12	6.2 KΩ
R308	HE 6-273-12	27 KΩ
R309	HE 6-225-12	2.2 MΩ
R310	Not used	
R311	HE 6-155-12	1.5 MΩ
R312	HE 234-517	250 KΩ (VERT SIZE control)
R313	Not used	
R314	HE 6-223-12	
R315	Not used	
R316	HE 6-273-12	27 KΩ
R317	HE 6-222-12	2.2 KΩ
R318	Not used	
R319	HE 6-473-12	47 KΩ
R320	Not used	
R321	HE 6-221	220 Ω, 1/2 watt
R322	HE 6-153-12	15 KΩ
R323	Not used	
R324	Not used	
R325	Not used	
R326	HE 6-750-12	75 Ω
R327	HE 6-332-12	3.3 KΩ
R328	HE 6-472-12	4.7 KΩ
R331	HE 6-279-12	2.7 Ω
RX124	HE 6-339-12	3.3 Ω
RX129	HE 6-101-12	100 Ω
RX130	HE 6-220-12	22 Ω
RX323	HE 6-339-12	3.3 Ω
RX333	HE 6-220-12	22 Ω
Transistors		
Q101	HE 234-275	Silicon, NPN
Q102	HE 234-522	Silicon, NPN
Q103	HE 234-276	Silicon, NPN
Q104	HE 234-275	Silicon, NPN
Q105	Not used	
Q106	HE 234-275	Silicon, NPN
Q107	HE 234-275	Silicon, NPN
Q108	HE 234-523	Silicon, NPN
Q301	HE 234-275	Silicon, NPN
Q302	HE 234-274	Silicon, PNP
Q303	HE 234-274	Silicon, PNP
Q304	HE 234-522	Silicon, NPN
Q305	Not used	
Q306	HE 234-272	Silicon, PNP
Q307	HE 234-271	Silicon, NPN
Q308	HE 234-522	Silicon, NPN
Miscellaneous		
Foam magnet	HE 234-268	
Heat sink	HE 234-525	

Parts List

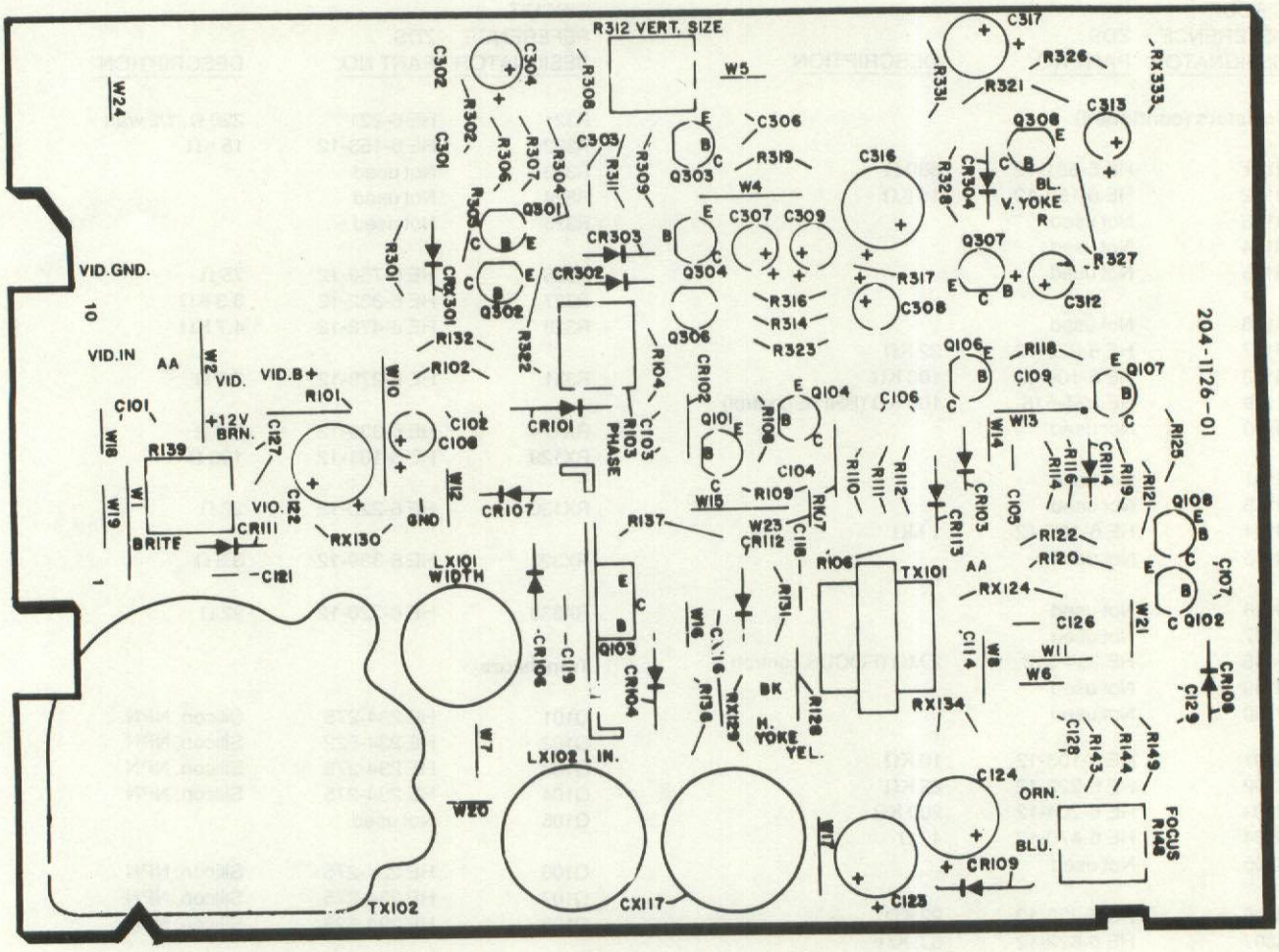


Figure 5.1. Video Deflection Board Parts Locations

Video Driver Board Parts List

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
Capacitors		
C127	HE 27-74	.01 μF polyester
C128	HE 21-90	.001 μF ceramic, 3 KV
C401	HE 25-882	22 μF electrolytic
C402	HE 25-917	10 μF electrolytic
C403	Not used	
C404	Not used	
C405	Not used	
C406	Not used	
C407	Not used	
C408	HE 21-43	.001 μF ceramic, 1 KV
Diode		
CR401	HE 234-267	103-254

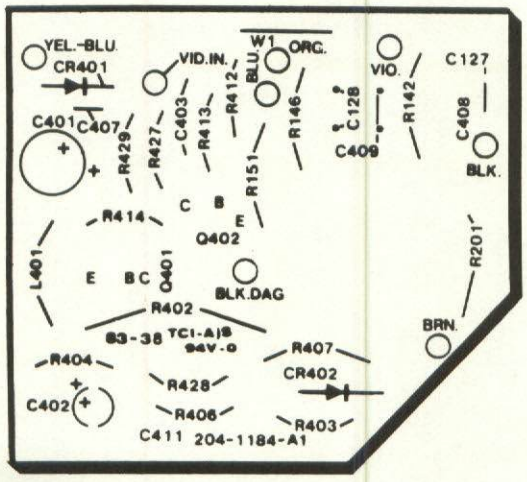


Figure 5.2. Video Driver Board Parts Locations

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
Inductor		
L401	HE 234-258	RF choke, 6.8 μH
Resistors		
NOTE: All resistors are 1/4 watt unless otherwise specified.		
R142	HE 6-222	2.2 KΩ, 1/2 watt
R146	HE 6-222	2.2 KΩ, 1/2 watt
R151	HE 6-473	47 KΩ, 1/2 watt
R201	HE 6-339	3.3 Ω, 1/2 watt
R401	Not used	
R402	HE 234-578	820 Ω, 2 watt
R403	HE 6-102-12	1 KΩ
R404	HE 6-102-12	1 KΩ
R405	Not used	
R406	HE 6-470-12	47 Ω
R407	HE 6-331	330 Ω, 1/2 watt
R408	Not used	
R409	Not used	
R410	Not used	
R411	Not used	
R412	HE 6-470-12	47 Ω
R413	Not used	
R414	HE 6-153-12	15 KΩ
R427	HE 6-470-12	47 Ω
Transistors		
Q401	HE 234-273	Silicon, NPN
Q402	HE 234-290	Silicon, NPN
Miscellaneous		
Socket, CRT	HE 234-337	7-pin socket

Major Assembly Parts List

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION
Video Tube		
VX201	HE 234-530	9-inch CRT, green phosphor
	or	
	HE 234-532	9-inch CRT, amber phosphor
Video Deflection/Driver Boards		
	A-12764	Assembled boards

SERVICE MODULE

Memory Cards

Z-100 PC Series Computers

585-66-02

860-45

ZENITH data systems

The purpose of this page is to make sure that all service bulletins are entered in this manual. When a service bulletin is received, annotate the manual and list the information in the record below.

Record of Service Bulletins

SERVICE BULLETIN NUMBER	DATE OF ISSUE	CHANGED PAGE(S)	PURPOSE OF SERVICE BULLETIN	INITIALS

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Abbreviations

AEN	Address Enable
CPU	Central Processing Unit
DIP	Dual Inline Pack
DMA	Direct Memory Access
I/O	Input/Output
IC	Integrated Circuit
LSB	Least-Significant Bit
MSB	Most-Significant Bit
ns	nanosecond
PAL	Programmable Array Logic
PC	Personal Computer
RAM	Random Access Memory
ROM	Read-Only Memory
TTL	Transistor-Transistor Logic

Chapter 1

Introduction and Specifications

Introduction

The information contained in this service module covers two different but similar memory cards used in the Z-100 PC Computer System. One of the cards is included in all systems and contains the memory and support circuitry, as well as parallel device interfacing circuitry. The second card, Model Z-305, is an add-on which enables system memory to be expanded when the first card is filled with RAM chips. The second card contains only memory chips, access circuitry, and the means to implement parity check and generation disables. The "Component Parts List," Chapter 6, reflects the parts complement for each board.

The memory cards in this computer contain the main dynamic user-accessible random access memory (RAM) and associated timing and multiplexing circuitry. Also contained on the initial card included in the system is the output connector for operating devices requiring information in a parallel data format and its supporting interface and control circuitry. The memory cards interface with the system through one of the parallel input/output (I/O) connectors located on the I/O backplane board. Connection with this board is implemented through a 64-pin edge connector which is an integral part of the memory cards. Three configuration jumpers on the initial card enable up to two blocks (cards) of memory to be designated, and allow one of two parallel port I/O addresses to be assigned to an external parallel device. Only the card-select jumper is installed on the add-on card.

Specifications

The computer comes with a minimum of 128K-bytes of RAM, but may contain up to 640K-bytes if you have installed additional banks and a second memory card. As presently configured, memory may be added in increments of 64K-bytes (8 RAM chips plus one parity chip per bank), thus enabling up to 320K-bytes to reside on one memory card and an additional 320K-bytes on a second card. Should 256K RAM integrated circuits (ICs) become economically viable, it will be possible to have the entire 640K-bytes on one memory card. The system will accept this configuration without further modification, although IC U455 will need to be replaced to provide the program address logic required by the denser chips.

The memory configuration is an 8-bit data structure, with odd parity generation and error detection to detect even-numbered bit-producing errors. The RAM ICs feature on-chip refresh, which is initiated when a given address is read. The direct memory access (DMA) controller provides the necessary refresh at required intervals, thereby eliminating contentions between refresh cycles and memory access cycles.

The memory access circuitry and the parallel interface are designed to be compatible with the IBM® Personal Computer (PC) and related software and firmware.

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Chapter 2

Configuration

CPU DIP Switch Settings

Switches SW101 and SW102 on the Central Processing Unit (CPU) card may need to be reconfigured should memory be increased or decreased. SW101 sections 2 and 3 are both set to OFF to represent a base memory size of 64K-bytes (the minimum configurable RAM in the computer), and probably will not require change. However, SW102 sections 0 through 4 will need to be reconfigured to reflect any changes made in memory size. The switch sections represent existing 32K-bytes amounts of memory in excess of the 64K-byte base size, according to the examples in Table 2.1. The table also shows the binary weights associated with each switch section. Note that OFF is equivalent to a logical 1 (one). To arrive at the memory size, in K-bytes, for a given system add the binary weights, multiply by 32, and add 64. Note also, since memory must be added in 64K-byte increments, some switch combinations will not be used.

Table 2.1. CPU Card DIP Switch Settings

	SW102 SECTION					
	0	1	2	3	4	MEMORY SIZE
BINARY WEIGHT	1	2	4	8	16	(K-BYTES)
	ON	OFF	ON	ON	ON	128
	ON	ON	OFF	ON	ON	192
	ON	OFF	OFF	ON	ON	256
	ON	ON	ON	OFF	ON	320
	ON	OFF	ON	OFF	ON	384
	ON	ON	OFF	OFF	ON	448
	ON	OFF	OFF	OFF	ON	512
	ON	ON	ON	ON	OFF	576
	ON	OFF	ON	ON	OFF	640

NOTE: OFF = logic one, ON = logic zero

Configuration Jumpers

J401, J402, and J403 are configuration jumpers located on the memory card. J401 is used as a card-select jumper. If only one memory card is used, J401 should be positioned to the left (away from the edge connector), marked "1st". If the system has two memory cards, position the jumper on the card to be designated as the first block of 320K-byte memory to "1st", and the jumper on the card containing the second block to the right, marked "2nd". If 256K RAM chips, as opposed to 64K, are used, only one card is used and J401 should be positioned to "1st".

J402 and J403 on the initial card are used to assign the parallel output port to a desired I/O port address according to Table 2.2.

Table 2.2. Parallel Port Address Selection

J403	J402	CONFIGURATION	PORT
0	0	Parallel Printer	*3BC
0	1	Parallel Printer	378
1	0	Port Disabled	N/A
1	1	Port Disabled	N/A

*This port corresponds to the monochrome display port on the IBM PC.

Chapter 3

Theory of Operation

Refer to the memory access block diagram, Figure 3.1, for the following general functional description of the memory card.

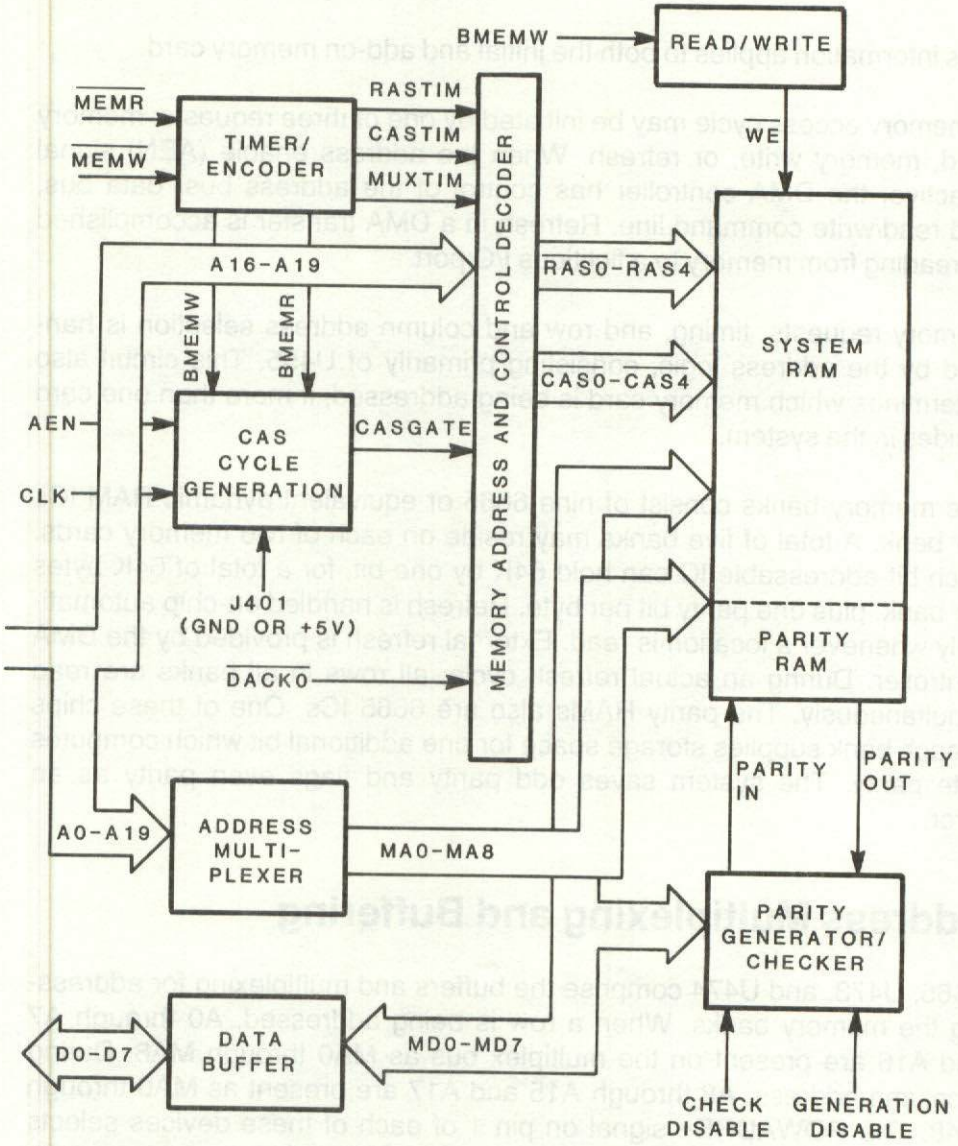


Figure 3.1. Memory Access Block Diagram

Memory Access Operations

This information applies to both the initial and add-on memory card.

A memory access cycle may be initiated by one of three requests: memory read, memory write, or refresh. When the address enable (AEN) signal is active, the DMA controller has control of the address bus, data bus, and read/write command line. Refresh in a DMA transfer is accomplished by reading from memory to a fictitious I/O port.

Memory requests, timing, and row and column address selection is handled by the address logic, consisting primarily of U455. This circuit also determines which memory card is being addressed, if more than one card resides in the system.

The memory banks consist of nine 6665 or equivalent dynamic RAM ICs per bank. A total of five banks may reside on each of two memory cards. Each bit-addressable IC can hold 64K by one-bit, for a total of 64K-bytes per bank, plus one parity bit per byte. Refresh is handled on-chip automatically whenever a location is read. External refresh is provided by the DMA controller. During an actual refresh cycle, all rows in all banks are read simultaneously. The parity RAMs also are 6665 ICs. One of these chips in each bank supplies storage space for one additional bit which computes byte parity. The system saves odd parity and flags even parity as an error.

Address Multiplexing and Buffering

U465, U473, and U474 comprise the buffers and multiplexing for addressing the memory banks. When a row is being addressed, A0 through A7 and A16 are present on the multiplex bus as MA0 through MA8. During a column address, A8 through A15 and A17 are present as MA0 through MA8. The ROWADRS* signal on pin 1 of each of these devices selects between a logical one and a logical zero to alternately place one group of bits or the other on the multiplex bus. The memory banks first latch off the low-order group of bits, then the high-order group, and combine them to form an 18-bit address word. (MA8 connects to pin 1 of the RAM sockets. Since pin 1 has no internal connection on the 6665 ICs, MA8 is not used when 64K-bit chips are used.)

Chapter 4

Detailed Circuit Description

Dynamic Memory

This information applies to both the initial and add-on memory cards.

Refer to the memory card schematic for the following descriptions.

Power Distribution

Operating power for the TTL devices which comprise the main memory and its access and parity circuitry is +5 VDC and 0 volts (ground).

+5 VDC enters the card on edge connector pins B3 and B29. Ground enters on pins B1, B10, and B31.

Ground is supplied on pin 10 of U455, U470, and U469; pin 7 of U467, U456, U468, and U451; pin 8 of U465, U473, U474, and U454; and to pin 16 of U401 through U409, U411 through U419, U421 through U429, U431 through U439, and U441 through U449.

+5 VDC is supplied on pin 20 of U455, U470, and U469; pin 14 of U467, U456, U468, and U451; pin 16 of U465, U473, U474, and U454; and to pin 8 of U401 through U409, U411 through U419, U421 through U429, U431 through U439, and U441 through U449.

Timing and Encoding

The cycle initiation and timing for memory access is controlled by U467, U469, and U456. An active-low from I/O bus MEMR* on pin 2, or MEMW* on pin 4 of U469, is inverted and ORed by U467. The resulting high at pin 3 of U467 becomes the RASTIM signal which is applied to pin 3 of U455, the memory access controller, and pin 1 of U456, a 100-nanosecond tapped delay line. U456 delays the row address strobe timing (RASTIM) signal 40 nanoseconds, and applies the resultant multiplex-timing (MUXTIM) signal at pin 4 to pin 1 of U455. 60 nanoseconds later the column address strobe timing (CASTIM) signal appears at pin 8 of U456, and is applied to pin 2 of U455. These three signals, RASTIM, MUXTIM, and CASTIM, set up the necessary timing relationships to properly access the selected memory address.

Main Memory Banks

The following description applies to systems containing 64K-bit RAM ICs (6665), with embellishment for 256K-bit systems added where clarification is needed.

The heart of the memory card is the memory itself. The supporting circuitry serves to time and control access to a given memory address, direct the transfer of data, and enable the parity generation and check circuitry on the card containing the memory block being accessed. The main user RAM and parity RAM are arranged in five banks of 64K bit-addressable RAM ICs, with nine chips in each bank. The chips are all 6665 NMOS ICs. Bank 0 consists of U401 to U409, bank 1 of U411 to U419, bank 2 of U421 to U429, bank 3 of U431 to U439, and bank 4 of U441 to U449. Eight chips in each bank (e.g., U402 to U409 in bank 0) are the actual RAM addresses, and the 9th chip in each bank (U401 in bank 0) is parity RAM. If your computer has the minimum amount of base user RAM, only banks 0 and 1 will be filled. Banks 2 through 4 will consist of empty sockets. You may add RAM in whole bank increments, that is, nine chips at a time. The appropriate dual inline pack (DIP) switch sections on the CPU card must be positioned to reflect the amount of RAM installed. See Table 4.1 for the location of user RAM in the system memory scheme.

When an individual memory address is accessed, every chip in the bank in which that address resides is affected. For instance, if access to the contents of an address in bank 3 were desired, one bit from each of chips U432 through U439 would contribute either a logical one or a logical zero to form the 8-bit information byte; and, if the address were to be read from, U431 would contribute a parity bit as an error check of that location. The bit from U439 would be the least-significant information bit (LSB), and the one from U432 the most-significant bit (MSB).

Table 4.1. System Memory Map

TYPE	HEX ADDRESS	DECIMAL ADDRESS
1st RAM Card	00000-4FFFF	0000000-0327679
2nd RAM Card	50000-9FFFF	0327680-0655359
Reserved	A0000-AFFFF	0655360-0720895
Monochrome Graphics	B0000-B3FFF	0720896-0737279
Reserved	B4000-B7FFF	0737280-0753663
Color Graphics	B8000-BBFFF	0753664-0770047
Reserved	BC000-BFFFF	0770048-0786431
Reserved for Z-319 Video Interface	C0000-EFFFF	0786432-0983039
MFM-150 Monitor	F0000-F3FFF	0983040-0999423
Scratchpad RAM		
Winchester Drive Buffer	F4000F7FFF	0999424-1015807
System ROM	F8000-FFFFF	1015808-1048575

64K RAM ICs

The 6665 RAM chips have a tendency to develop a signal undershoot condition when a fast negative-going pulse is applied. RP402, RP404, and RP405 are DIP resistor packs containing 33-ohm resistors which act to damper the signals from the address and timing circuits and provide a buffer to the RAM ICs.

To understand how memory is accessed, you must first understand how the memory chip itself is structured. Refer to Figure 4.1 for the following description.

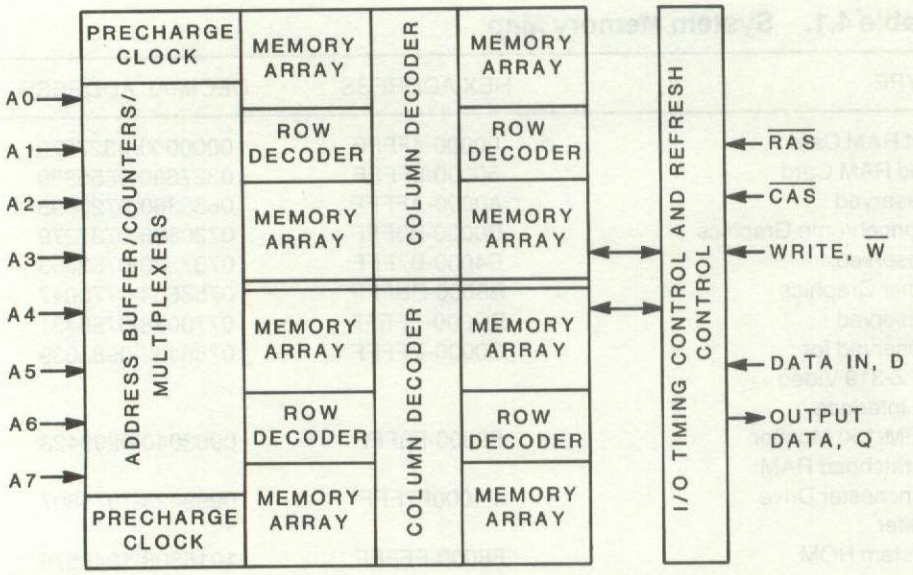


Figure 4.1. 6665 Dynamic RAM IC Architecture

Memory Access Timing

The 6665 dynamic RAM IC is capable of storing 65,536 (64K) one-bit words. In order to address 64K-bits with only eight address lines, it is necessary to multiplex the RAS* and CAS* (row address and column address strobe signals) enables. First the RAS* signal is applied which allows the RAM to latch the eight least-significant bits off the I/O address bus. Then, 100 nanoseconds later, the CAS* signal is applied and the eight most-significant bits are retrieved, to obtain the full 16-bit (or 18-bit for 256K chips) address word. The low-order bits also would include A16, and the high order bits, A17, if 256K chips are installed. The MUXTIM signal, which is derived from the RASTIM signal and delayed 40 nanoseconds, enables the toggling between the high- and low-order bytes through the address multiplexing to accomplish this. The 60-nanosecond time-delay between MUXTIM and CASTIM introduced by the delay line, U456, provides a settling-out time to ensure that the signals on the address lines are stable before the CAS* signal arrives. Figure 4.2 is a timing chart which illustrates the relationship between the timing signals.

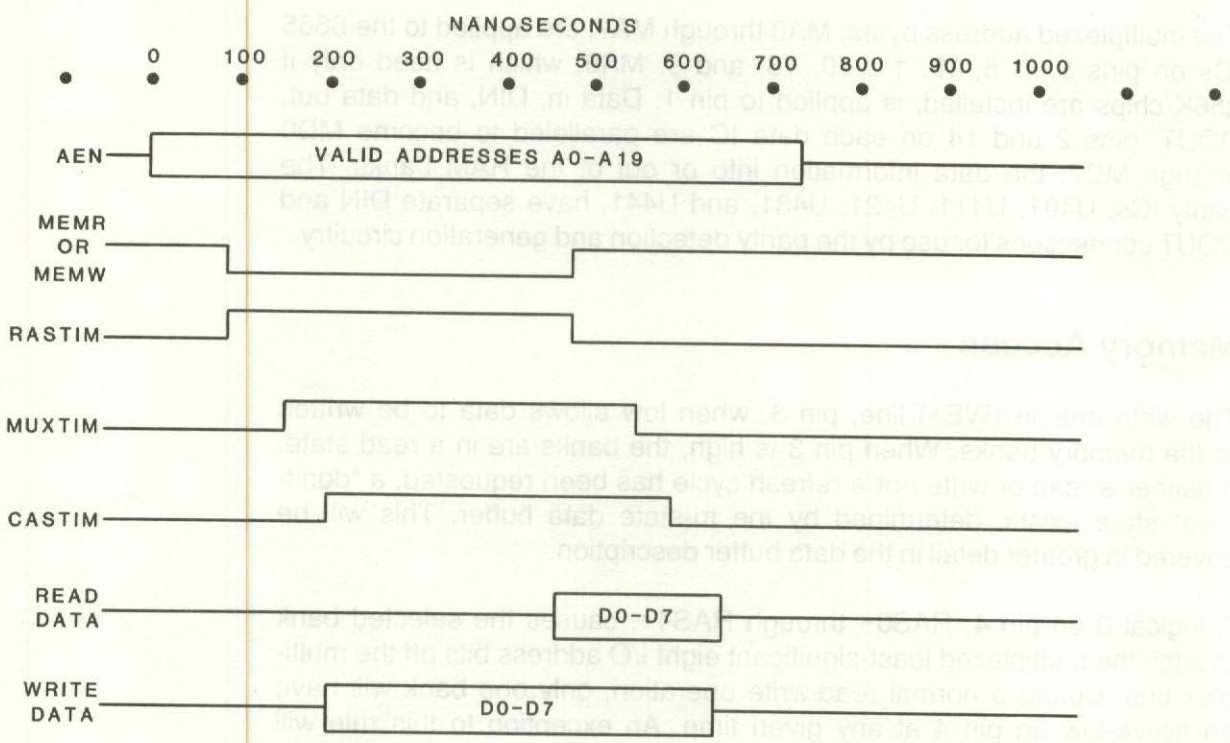


Figure 4.2. Multiplex Timing Chart

From a functional standpoint, each memory chip can be considered a 256-by-256 bit matrix, with the address byte gated by the RAS* signal selecting the row, and the address byte gated by the CAS* signal selecting the column. When all the bits from the same rows and columns of the eight data chips in a bank are combined, one data byte is formed.

Row Addressing

U455, the address decoder, uses I/O address bits A16 through A19 to determine which RAS* line to enable. During a normal read/write operation, only one of the lines, RAS0* through RAS4*, will be low and the memory bank associated with that line will be the only one enabled. When the CAS* signal arrives, the multiplexed address will be present at all five banks, but will be recognized only by the bank selected with RAS*.

The multiplexed address bytes, MA0 through MA7, are applied to the 6665 ICs on pins 5, 7, 6, 12, 11, 10, 13, and 9. MA8, which is used only if 256K chips are installed, is applied to pin 1. Data in, DIN, and data out, DOUT, pins 2 and 14 on each data IC are paralleled to become MD0 through MD7, the data information into or out of the RAM banks. The parity ICs, U401, U411, U421, U431, and U441, have separate DIN and DOUT connections for use by the parity detection and generation circuitry.

Memory Access

The write enable (WE*) line, pin 3, when low allows data to be written to the memory banks. When pin 3 is high, the banks are in a read state. If neither a read or write nor a refresh cycle has been requested, a "don't-care" state exists, determined by the tri-state data buffer. This will be covered in greater detail in the data buffer description.

A logical 0 on pin 4, RAS0* through RAS4*, causes the selected bank to latch the multiplexed least-significant eight I/O address bits off the multiplex bus. During a normal read/write operation, only one bank will have an active-low on pin 4 at any given time. An exception to this rule will be covered under Refresh Cycle.

Column Addressing

A logical 0 on pin 15, CAS0* through CAS4*, signals the bank selected by the RAS* line to latch the eight most-significant bits off the multiplex address bus. The two 8-bit bytes are then utilized internally to fetch data from or write data to the proper row and column for the selected address. If 256K chips are installed, the MA8 address line also is used to form two 9-bit strings required to address the additional memory locations.

Programmable Array Logic

Memory access and refresh cycling is under control of U455, a PAL16L8 IC. A different PAL chip is required if 256K memory is installed. This device determines the correct memory bank for a given address, and controls the traffic on the address and data busses between the rest of the system and the memory banks. It also selects which block of memory is to be addressed, if more than one card is installed.

RAMSEL* Signal

Data transfer and parity error generation on a given card will take place only if the RAM select signal, RAMSEL*, is low. If RAMSEL* is high, U470, the data buffer, is tri-stated (inactive) and parity error generation output is gated off. RAMSEL* will be low under the signal conditions shown in Table 4.2.

Table 4.2. RAMSEL* Signal Logic

FIRST	DACK0*	A19	A18	A17	A16
1	1	0	0	D/C	D/C
1	1	0	1	0	0
0	1	0	1	0	1
0	1	0	1	1	D/C
0	1	1	0	0	D/C

(D/C = Don't Care)

The FIRST signal, as shown in the table, is set for a given memory card by J401, depending on which card has been selected to be the first bank of 320K-bytes, and which the second. RAMSEL* will always be low on one card when it is high on the other during a normal read or write operation.

Memory Bank Selection

The row address strobe, RAS* (bank select), logic is determined by decoding address bits A16 through A19 on pins 4 through 7, along with FIRST on pin 11 and RASTIM on pin 3 of U455, according to the logic expressed in Table 4.3.

Table 4.3. Memory Bank Select Logic

FIRST BLOCK (CARD ONE)

BANK	FIRST	A19	A18	A17	A16	RASTIM	MEMORY RANGE
0	1	0	0	0	0	1	00000-0FFFF
1	1	0	0	0	1	1	10000-1FFFF
2	1	0	0	1	0	1	20000-2FFFF
3	1	0	0	1	1	1	30000-3FFFF
4	1	0	1	0	0	1	40000-4FFFF

SECOND BLOCK (CARD TWO)

BANK	FIRST	A19	A18	A17	A16	RASTIM	MEMORY RANGE
0	0	0	1	0	1	1	50000-5FFFF
1	0	0	1	1	0	1	60000-6FFFF
2	0	0	1	1	1	1	70000-7FFFF
3	0	1	0	0	0	1	80000-8FFFF
4	0	1	0	0	1	1	90000-9FFFF

As can be seen, J401 sets the logic level of the FIRST signal on each memory card, which determines whether the card is the first or second.

A memory refresh cycle also is initiated by the PAL, by selecting all five banks on both cards at the same time whenever DACK0* goes low. Actually, RAS0* and RAS3* are selected 40 nanoseconds ahead of RAS1*, RAS2*, and RAS4*, to minimize current requirements by the card as determined by the RASTIM and MUXTIM signals, respectively. The banks remain selected until completion of the refresh cycle, which occurs at least once every 2 milliseconds.

ROWADRS* also goes low if DACK0* is low during a refresh cycle. This allows the eight least-significant address bits to pass on to the RAMs as the refresh address.

Column Selection

60 nanoseconds after column selection, CASTIM from pin 8 of U456 is applied to pin 2 of U455. The CAS signal on pin 14 of U455 goes high, and, inverted by five inverter sections of U454, forms the columm address strobe signals, CAS0* through CAS4*. After signal dampering by 33-ohm resistors in resistor packs RP402 and RP404, these active-low signals are applied to pin 15 of the memory bank chips. ROWADRS* is high at this time, gating the eight most-significant address bits onto the multiplex bus. The bank selected by RAS* now latches the high-order bits off the multiplex bus and uses them to select one of the 256 columns of bits in each of its RAM ICs, completing the address selection cycle.

CAS also is high if RASTIM, CASGATE, or RAMSEL are high, or DACK0* is low.

The CASGATE signal is active-high any time a bus memory read (BMEMR) signal is high on pin 12 of U467, the AEN signal is high on pin 13 of U467, or the bus memory write (BMEMW) signal sets the MWTC flip-flop at pin 2 of U468.

Address Multiplexing

U465, U473, and U474 convert I/O bus address bits A0 through A17 to a nine-bit multiplexed address bus comprising MA0 through MA8. MA8, while always present on the bus, is used only if 256K RAM chips are installed. MA0 through MA7 supply all the addressing information required by systems using 64K RAM chips.

A0 through A4 come in on pins 2, 5, 11, and 14 of U465. A5 through A7 come in on the same pins of U473. A16 comes in on pin 2 of U474. When ROWADRS* (row select) is low, these nine bits are gated through these three ICs on pins 4, 7, 9, and 12 of U465 and U473, and pin 4 of U474, to become the row address for the RAM chips.

Addresses A8 through A11 come in on pins 3, 6, 10, and 13 of U465. A12 through A15 come in on the same pins of U473. A17 comes in on pin 3 of U474. When ROWADRS* is high, these nine bits are gated through the multiplexer on pins 4, 7, 9, and 12 of U465 and U473, and pin 4 of U474, to become the column address for the RAM chips.

33-ohm resistors, part of RP404 and RP405, provide the damping required to minimize undershoot on the multiplexed address signals before applying them to the RAM.

Tri-State Data Buffer

U470, the input/output data buffer, interfaces the memory banks with the I/O data bus for the system. As implied by its name, it has three discrete states.

- Active write: gates data from the I/O bus to RAM;
- Active read: gates data from RAM to the I/O bus;
- Inactive: blocks data flow in either direction.

When the buffer is inactive, it is said to be tri-stated (or in its high impedance state).

The 4.7K-ohm resistors, RP401, connected between +5 volts and pins 11 through 18 of U470, act as pull-up resistors for the memory side input/output lines.

The buffer transfers data according to the logic represented by Table 4.4.

Table 4.4. Tri-State Data Buffer Logic

	GBA*	GAB
Memory to I/O	0	0
Dual-Enabled (Not Allowed)	0	1
Inactive (Tri-Stated)	1	0
I/O to Memory	1	1

GAB, on pin 1 of the buffer, connects to the bus memory write (BMEMW) signal line. Bus memory read (BMEMR) uses pins 8 and 12 of U469 to invert and emerge as BMEMR*, which is applied to pin 19 (GBA*) of U470. I/O data lines D0 through D7 come in on pins 2 through 9 of U470. Pins 4, 5, and 6 of U467 are the inputs and output of an OR gate used as a negative-logic AND gate; i.e. both inputs must be low for the output to be low.

When BMEMR is active-high, BMEMR* is active-low. BMEMW also is low (inactive) at this time, so if RAMSEL* is low, logical conditions are correct to transfer (read) data from the memory data bus to the I/O bus.

When BMEMW goes active-high, BMEMR* is high and the negative logic AND gate output is high. Logical conditions are now correct for data transfer from the I/O bus to memory (write).

Data transfer can be effectively stopped in one of two ways:

- By holding RAMSEL* high when BMEMW is low. This has the effect of placing the buffer in an isolate state.
- By placing both BMEMW and BMEMR high at the same time. This dual-enables the buffer by placing a high on pin 1 while BMEMR* and RAMSEL* together force a low on pin 19. The effect of a dual-enable is to place the corresponding bits of each bus at the same logic levels.

Dynamic RAM Refresh Cycle

As mentioned previously, a RAM refresh takes place when a given location is read or written. This is handled by circuitry on the RAM ICs. For more details on how the chip does this, refer to the data sheet for the 6665 ICs in Chapter 8.

External refresh of all the RAM takes place as follows:

Every 16.4 microseconds a refresh cycle takes place (2 milliseconds to refresh all 128 rows). If a read or write operation is in progress or is requested simultaneously with a refresh request, the read/write request is serviced first, then refresh is initiated. When the DACK0* line to the program address logic goes active-low, as the result of a DMA request on channel 0 (refresh request), all the memory banks are selected at once. That is, RAS0* through RAS4* all go low.

DACK0* presents the least-significant eight address bits to the RAMs and pulls all RAS* signals down at the same time. DMA0 passes through memory, one row at a time. It takes approximately 780 nanoseconds to read each row.

Parity Generation and Error Checking

The parity generation and error checking circuitry consists of U451, U457, U469, U468, and U464. The parity memory consists of U401 for bank 0, U411 for bank 1, U421 for bank 2, U431 for bank 3, and U441 for bank 4. Parity bits enter the parity RAM on pin 2 of each chip and exit on pin 14. Pin 2 and 14 are electrically separated on the parity RAM chips, not tied together as they are on the data memory chips.

The circuitry is configured to generate and check for odd parity. The error check will trap any data mutilation which causes an even number of logical ones in the nine-bit word comprised of MD0 through MD7 and parity bit MD8 from pin 14 of the parity RAM ICs.

Parity Generation

The data word, consisting of bits MD0 through MD7, is applied from the memory data bus to pins 8, 9, 10, 11, 12, 13, 1, and 2 of the parity generator U451. During a write operation, the RAM outputs are inactive, causing all the parity RAM pin 14 lines to be pulled up to +5 volts. This places a logical one on pin 4 of U451. U451 checks to see how many logical ones are in the string of nine bits. If there are an even number, the parity generator outputs a logical one to pin 5. If there are an odd number of bits, a logical 0 is output on pin 5. U457 accepts this logic state on pin 4 and inverts it to pin 6, which is routed to all parity RAM pin 2 data input lines. When BMEMW goes high and gates the data buffer into the I/O-to-memory transfer state, the selected memory address not only stores the eight bits off the data bus, but also picks off the bit on pin 2 of the parity RAM ICs and stores it along with the data word.

As an example, assume that the I/O data word has logical ones in positions A6, A5, A3, and A1:

A7	A6	A5	A4	A3	A2	A1	A0
0	1	1	0	1	0	1	0

There are four logical ones presented to the parity checker, plus an additional one on pin 4,

A7	A6	A5	A4	A3	A2	A1	A0	Parity Bit
0	1	1	0	1	0	1	0	1

for a total of five. U451 counts five high-level bits and generates a low on pin 5 (EVEN*). U457 inverts this to a high and presents it to the parity RAM data-in bus, pin 2. When the data is stored, there will be five logical ones in the nine-bit string, maintaining odd parity.

Conversely, had the data string contained an odd number of ones, a logical 0 would have been stored in parity RAM.

Parity Error Trapping

When data is read out of a bank, all nine bits are presented to U451: MD0 through MD7 off the bus, and the parity bit from pin 14 of parity RAM. If an error condition has caused the nine-bit string to contain an even number of logical ones, U451 places a logical one on pin 5 (EVEN). U457 pin 1 senses this and resets U468, a D-type flip-flop. The Q* output goes high, is inverted by U464 and applied to the I/O channel check line as an active-low parity error (IOCHCK*).

For instance, if we assume a noise spike on the data bus has inserted an additional logical one at A0 in our previous example:

A7	A6	A5	A4	A3	A2	A1	A0	Parity Bit
0	1	1	0	1	0	1	1	1

U451 counts the bits, sees six and generates a high on pin 5 to signify an even parity error. If the noise had caused the number of ones to be odd, no error would be detected and pin 5 would be low.

Either parity generation and/or parity checking may be disabled by software means. The disable parity check (DISPCHK*) signal, when active-low, holds the D-type flip-flop in a preset condition, causing it to ignore changes on its D input at pin 12. Similarly, if the disable parity generation (DISPGEN*) signal is made active-low, it gates NAND-gate U457 off, preventing any state change at the parity RAM data inputs.

Parallel I/O Port

This information, except parity disable descriptions, applies only to the initial memory card included in the system.

Refer to Figure 3.2, the parallel interface block diagram, and to the memory card schematic, sheet 2, for the following description.

In addition to the memory access functions, the memory card also provides an interface for transfer of parallel data from the computer to an external parallel device, and status signals from the device to the computer. One printer per memory card may be assigned a port address by proper positioning of jumpers J402 and J403. Connection to the outside world is by means of a 25-pin D-type connector physically mounted at the rear of the card. This connector extends through the rear of the computer cabinet for ease of attachment to the external device.

Supporting circuitry includes a PAL chip acting as an address decoder; a tri-state buffer for data-direction control; data output latches; diagnostic error checking devices; and associated gates, pull-up resistors, and decoupling capacitors. All of the logic devices are TTL types.

Three ports are supported by circuitry on this card. Ports A and C are read and write ports. Port A is the parallel data port and port C the device command port. Port B is a read-only port to drive status signal data from the parallel device onto the parallel data bus. The read ports associated with A and C are used to perform a diagnostic check of the data sent out to the parallel device, to ensure, for example, that false data is not present on the data lines as a result of malfunctions in the device.

Supply Voltage

Operating power for the TTL devices is distributed on two supply busses: +5 VDC and 0 volts (ground).

Ground (0 volts) is routed to pin 10 on U471, U453, and U452; pin 8 on U472, U463, U462, and U458; pin 7 on U464, U461, and U457; and to pin 12 on U459.

+5 VDC connects to pin 20 on U471, U453, and U452; pin 16 on U472, U463, U462, and U458; pin 14 on U464, U461, and U457; and to pin 24 on U459.

Signal Names

Table 4.5 defines the signals present on the parallel interface 25-pin connector, P401. The flow column indicates direction of signal travel with respect to the attached parallel device.

Table 4.5. Interface Connector Signal Names

PIN NUMBER	SIGNAL NAME	DESCRIPTION	FLOW
2-9	PDATA0-PDATA7	Parallel data bits 0 through 7. Active-high.	In
1	STROBE*	Gates data in from external device. Active-low.	In
14	AUTO FD XT*	When low, automatically line feeds printer paper at the end of a line.	In
31	INIT*	Resets printer controller to its initial conditions and clears its data buffer.	In
17	SLCT IN*	When low, allows data to be placed in the printer's data buffer.	In
18-25	GND	Signal return (ground) lines.	—
15	ERROR*	Goes low when printer is in an error status, as when out of paper or off line.	Out

Table 4.5 (Continued). Interface Connector Signal Names

PIN NUMBER	SIGNAL NAME	DESCRIPTION	FLOW
13	SLCT	This active-high signal indicates printer acknowledgement of selected operating state.	Out
12	PE	When high, printer is out of paper.	Out
10	ACK*	Printer acknowledgement of receipt of data and ready to accept additional data. Active-low.	Out
11	BUSY	Prevents transmission of further data to printer when high, during data transfer, printing, off line, or in error state.	Out

Table 4.6 defines the signals used by the parallel interface which appear on the system I/O bus.

Table 4.6. I/O Bus Signal Names

SIGNAL NAME	DESCRIPTION
A0-A9	Address lines 0 through 9. Used by PAL for address decoding.
D0-D7	The eight I/O data lines. Used to transfer information between the bidirectional data buffer and the microprocessor or memory.
RESET DRV	Reset driver. Used to reset the port C data latch and the parity control data latch.
AEN	Disables parallel port during DMA transfers.
IOR*	I/O bus read request. When low, causes data from the parallel interface to be driven onto the I/O bus. Address decoding determines bus driver involved.
IOW*	I/O bus write request. When low, causes data to be latched off the I/O bus. Address decoding determines latch involved.
IRQ7	Interrupt request 7. This is the parallel printer interrupt request signal. It is derived from the printer acknowledge (ACK*) and port B interrupt enable (INTRENB) signals.

DISPCHK* and DISPGEN* are signals generated by the parity control data latch for use by the parity generation and error check circuitry. When the proper data value appears on the bus, and I/O port address 100 (hex) is selected, one or the other (or both) parity disable signal(s) is (are) formed.

Program Decoder

U459 is a PAL14L8 IC configured to act as an address decoder for the parallel interface logic devices. It uses I/O address lines A0, A1, and A3 through A9 on pins 1 through 9; AEN on pin 10; IOR* on pin 11; IOW* on pin 13; and logic signals from jumpers J2 and J3 on pins 14 and 23 to determine logic device selection.

With the exception of the write parity control signal, WPCNTRL*, only two possible A3-A9/J2/J3 bit-pattern combinations will be recognized by the decoder logic:

J2	J3	A9	A8	A7	A6	A5	A4	A3
0	0	1	1	1	0	1	1	1

and:

J2	J3	A9	A8	A7	A6	A5	A4	A3
1	0	1	1	0	1	1	1	1

Bits A0 and A1 determine which of the three ports—A, B, or C—is selected:

A1	A0	Port
0	0	A
0	1	B
1	0	C

IOW* and IOR* determine whether a read or write operation is to be initiated. AEN must be low for any program selection. The configuration jumpers, J402 on pin 14, and J403 on pin 23 of U459, determine which of two port addresses are assigned to ports A, B, or C, according to the logic of Table 4.7.

The last two conditions disable the parallel interface, except for parity disable functions.

Table 4.7. Printer Configuration Jumpers

J403	J402	PORT A	PORT B	PORT C
0	0	3BC	3BD	3BE
0	1	378	379	37A
1	0	——Disabled——		
1	1	——Disabled——		

Data Transfer

The direction in/out signal, DIROUT*, from pin 15 of U459 to pin 1 of U471, determines the direction data travels through U471, the bidirectional data buffer. When a logical 0 is present on this line, data on the B side of U471 is gated to the bus on the A side, or in this case, from the device side to the system I/O bus. When DIROUT* is at a logical one, data flows from the A side of U471 to the B side, or from the bus to the device.

In order for data to be read onto the I/O bus, IOR* must be active-low. If it is not, the data buffer is in its direction-in (DIROUT* is high) state, routing data off the I/O bus to the parallel interface bus.

Writing To Port A

The WPA* signal controls the write-port A function. It must be low to allow the transfer of information off the data bus to U453, the port A data latch. In order for WPA* to be low, J2 and J3 must be positioned to select one of the two valid port addresses; a valid port A address (378 or 3BC) must be on the address bus; AEN must be low; bits A0 and A1 must be low; and IOW* must be active-low. WPA* connects from pin 16 on U459 to pin 11, which is the CLK signal for U453, the port A data latch. WPA* goes low at the beginning of the I/O write cycle, stabilizing the data. At the end of the write cycle WPA* goes high, latching data into the port and outputting data at that time. The data appears at pins 2, 5, 6, 9, 12, 15, 16, and 19 of U453, and is routed to pins 2 through 9 of the 25-pin D connector to become the parallel device input data. These same lines are routed to U452, the diagnostic read bus driver for port A.

Capacitors C478, C479, C482, and C484 through C488 on the data lines stabilize the output signals and minimize noise.

Reading Port A

The RPA* signal goes active-low if J402 and J403 are not in a disable state; either port address 378 or 3BC is selected; AEN is low; A0 and A1 are low; and IOR* is active-low. RPA* appears at pin 17 of U459 and is applied to U452, pins 1 and 19. This gates the PDATA outputs at pins 2, 4, 6, 8, 11, 13, 15, and 17 back onto the interface data bus from pins 18, 16, 14, 12, 9, 7, 5, and 3 of U452. DIROUT* is also low at this time, which drives the data onto the I/O bus. Diagnostics on the CPU card compare this data with the signals sent out and, if different, signify an error condition.

Writing to Port C

The WPC* signal goes active-low if J402 and J403 are not in a disable state; either port address 37A or 3BE is selected; AEN is low; A0 is low and A1 is high; and IOW* is active-low. WPC* appears at pin 18 of U459 and is applied to the CLK line, pin 9 of U472. WPA* goes low at the beginning of the I/O write cycle, stabilizing the data. At the end of the write cycle WPA* goes high, latching data into the port and outputting data at that time. These states appear at the Q outputs on pins 2, 5, 7, 10, and 12. The output on pin 15 is not used.

BD0 through BD3 are inverted and applied to pins 1, 14, 16, and 17 of the parallel connector to become the STROBE*, AUTO FD XT*, INIT*, and SLCT IN* signals for a parallel printer. BD4 on pin 12 of U472 becomes the port B interrupt enable signal, INTRENB*. 4.7K-ohm resistors, part of resistor pack RP403, are pull-up resistors for the open collector inverters of U464. 330 pF capacitors C76, C77, C81, and C83 are used for noise suppression.

The inverter outputs and INTRENB* also are applied to the input of U463, the port C diagnostic bus driver.

Reading Port C

RPC* on pin 20 of U459 goes active-low if J402 and J403 are not in a disable state; port address 37A or 3BE is selected; AEN is low; A0 is low and A1 is high; and IOR* is active-low. When RPC* is asserted and applied to pins 1 and 15 of U463, STROBE*, AUTO FD XT*, INIT*, and SLCT IN* on pins 2, 4, 6, and 10, INTRENB on pin 12, and DISPGEN* on pin 14, are accepted and inverted, then driven onto the interface bus lines as bits BD0 through BD5. Diagnostics on the CPU card check the logic levels of these signals, compare them to the data sent out and, if different, output an error condition. The 4.7K-ohm resistor, part of RP403, pulls the output of the open collector inverter at pins 12 and 13 of U464 up to +5 volts when a logical 0 is present on INTRENB.

Reading Port B

RPB* at pin 19 of U459 goes low if J402 and J403 are not in a disable state; port address 379 or 3BD is selected; AEN is low; A0 is high and A1 is low; and IOR* is active-low. RPB* is applied to pins 1 and 15 of device status read port U462. The status of ERROR*, SLCT, PE, ACK*, and BUSY, from pins 15, 13, 12, 10, and 11 of the device connector, is accepted at pins 4, 6, 10, 12, and 14 of U462, and driven onto the interface data bus to emerge as BD3 through BD7 at pins 5, 7, 9, 11, and 13. The status of DISPCHK* on pin 2 also is sampled to become BD2 at pin 3. BUSY is inverted by the buffer at pins 8 and 9 of U461 before application to U462.

Parity Disable Circuitry

WPCNTRL* at pin 21 of U459 goes active-low if port address 100 hex is selected, AEN is active-high, and IOW* is active-low. WPCNTRL* is applied to pin 9, the CLK line of U458, latching up the logic states at BD0, pin 3, and BD1, pin 4. BD0 controls the state of the disable parity check (DISPCHK*) signal at pin 2, and BD1 the state of the disable parity generator (DISPGEN*) signal at pin 5. DISPCHK*, when low, disables the parity check flip-flop, U468, and DISPGEN* turns off the parity generation gate, U457, for diagnostic system checks, when the proper data is present on BD0 and/or BD1. DISPCHK* also is presented to the read device status port, U462, and DISPGEN* to U463, port C read.

U472 and U458 Reset

The reset driver (RESET DRIVER) signal off the I/O bus is inverted by the buffer at pins 1 and 2 of U461, and applied as RESET* to clear the C write port, U472, and the parity control port, U458. RESET* is applied to pin 1, the CLR* line, on both of these ICs.

Parallel Interface Interrupt Request

The interrupt request for the parallel port is IRQ7. Interrupt enable, INTRENB, from write port C is applied to U457, pin 10. The acknowledge (ACK*) signal from the parallel device connector pin 10 is inverted by U461, pins 11 and 10, and applied to pin 9 of U457. If INTRENB is active-high and ACK* is active-low, the resulting low at pin 8 of U457 is inverted by U461 and emerges as an active-high IRQ7. This causes the CPU to recognize and service the request being made by the parallel device.

Chapter 5

Troubleshooting

If you have encountered problems with the computer, and indications point to the memory card as the source of the difficulty, proceed to isolate the fault(s) in the manner described in this section.

NOTE: If you have the Disk-Based Diagnostics package, you may find it easier and more efficient to use the package than the procedures outlined here.

The first and last 64K of RAM chips are checked by the built-in ROM diagnostics. Since faulty RAM chips are pinpointed, RAM fault-isolation will not be duplicated here.

General

If a spare memory card is available, it is best to first substitute it in place of a suspect card to ensure that the malfunction is on the memory card. If replacement of the card eliminates the problem, the removed card was at fault and must be either repaired or replaced.

The following checks and measurements will require the use of an oscilloscope, appropriate leads and probes, and standard hand tools (listed in the Base Units Service Modules). When troubleshooting, use extreme care to avoid damage to the delicate components on the card.

CAUTION: This card contains electrostatic-sensitive devices (ESD). Exercise extreme care when handling these devices to prevent damage.

Troubleshooting procedures are divided into two parts — those concerning the memory access circuits, and those involving the parallel interface circuits.

It is recommended that the ROM-based diagnostics be used to isolate problems of a complicated nature. Refer to the information detailing use of these routines in the Base Units Service Modules.

Memory Access Circuits Fault Isolation

Troubleshooting the memory card access circuits should, for the most part, be fairly straightforward. Many problems which occur on this card should be pinpointed by the automatic checks made when the computer is first powered up. If further fault isolation is deemed necessary, use the procedures outlined here.

Memory Banks

If, at powerup, an error message is displayed indicating a malfunction in the RAM, it should be noted that the automatic checks abort as soon as a bad memory location is detected. This could mean that other deficiencies in the circuitry are being masked, because the checks that would detect them were never performed.

To make sure that a given address and chip appearing in the error message are definitely at fault, turn off the computer and swap the suspected chip with one in a different location. Repeat the ROM diagnostic checks to see if the same chip is again flagged. If it is, chances are good that the chip originally in that location is all right, and that the cause of the difficulty lies elsewhere, for instance, in the memory address logic.

The ROM diagnostics provide an excellent means of further isolation of a problem of this nature, especially the debugging routines. You can use the special debugging commands to send values to questionable memory address locations. The E command, which examines or optionally changes specific memory contents, should be especially useful in the foregoing situation. See the troubleshooting chapter in the Base Units Service Modules for details on the use of this command.

The F command, which fills selected portions of memory with specific data, also may prove useful when dealing with problems affecting large sections of memory.

NOTE: Check DIP switches on the CPU card.

If it appears that the wrong RAM banks are being selected, suspect problems with the program address logic, U455.

If the same address location in each bank is affected, the multiplexing ICs, U465 and U473 (also U474 if 256K RAM chips are installed), should be substituted.

If only the high-order addresses in each bank are deficient, U467, U468, and U469 should be checked. These ICs provide the signals required to generate the column-address (CASGATE) logic.

Data Dropout

If data dropout is occurring but is not flagged by the parity checks, and it is affecting only the user memory, U470, the tri-state data latch should be suspected.

Parity RAM

If the error message indicates a parity malfunction, and you suspect that the problem may not be in the RAM but in the parity generation and error checking circuitry itself, the debugging commands I and O could be used to disable and look at subsequent parity results. I and O are commands which enable you to output values to, or read values from, the various ports. The parity disable port is 100 hex. A value of 1 sent to this port will disable the parity check circuitry, a value of 2 will disable the parity generation circuitry, and a value of 3 will disable both functions. You may then make logical decisions based on the results this action has on the parity error state.

Timing Problems

If many dissimilar problems are occurring with memory access, it is possible that access timing is off. Checks of the RASTIM, CASTIM, and MUXTIM timing relationships with a multi-trace oscilloscope can be made to ascertain proper timing. Refer to Figure 4.2 for the required waveforms. You will need to initiate a memory read or write operation using the debugging E command to properly view these relationships. If the timing appears to be off, the delay line, U456, should be a prime suspect.

Parallel Interface Fault Isolation

(Initial memory cards only)

Troubleshooting the parallel interface portion of the memory card should, in most cases, present no real difficulty. The on-board diagnostic ICs will aid in isolating problems related to device interfacing.

Read and Write Ports

If the microprocessor flags an error on a given parallel read or write port, first disconnect the device to see if the malfunction goes away. If it does, the device itself or its attaching hardware is suspect. Refer to the service material provided with the device.

If the discrepancy still is present, try replacing either the read or write IC associated with the port flagged as the cause of the error. For example, assume that the microprocessor has indicated a data-compare error on port C. U472, U463, U461, and U464 should be replaced one at a time to eliminate the error condition. Also examine the circuit card foil to ensure that no physical damage has occurred in the areas associated with the flagged port. An oscilloscope may be needed to determine the presence or absence of required data at the individual devices.

The mechanical connections between the computer and attached device should always be given close scrutiny in the event of interface malfunction. A large proportion of malfunctions are traced to physical interconnections between devices.

Data Bus

If erroneous data is being written to or read from the parallel interface, and the port ICs themselves have been eliminated as the problem source, suspect the bidirectional data bus IC, U471, especially if no data retrieval problems have been encountered with other devices or the user memory banks. Also check pin 1 of U471 with an oscilloscope. The signal on this line determines whether data is coming from or going to the I/O data bus. It should be low for data going onto the bus from the parallel device, and high when data is being sent to the device.

Address Decoder Problems

Use Tables 5.1 and 5.2 to aid in isolating address decoder problems. Again, the address decoder on the parallel interface circuitry should be suspected only if no addressing problems have been encountered with the memory banks or other devices.

The seven port select signals developed by the PAL IC, U459, must be low to enable a given device, as defined by Table 5.1.

Table 5.1. Address Decoder Outputs

SIGNAL	DESIGNATOR	DEVICE
DIROUT*	U471	Bidirectional Data Bus
WPA*	U453	Write Port A
RPA*	U452	Read Port A
RPB*	U462	Read Port B
WPC*	U472	Write Port C
RPC*	U463	Read Port C
WPCNTRL*	U458	Write Parity Control

Table 5.2 is a truth table defining the logic conditions required on U459 inputs to enable a given data transfer. J403 and J402 must be configured one of two ways, as shown, or the parallel interface will be disabled.

ADDRESS	J403	J402
3BC	0	0
378	0	1

Table 5.2. Program Decoder Logic

FUNCTION	INPUTS											
	IOW*	IOR*	AEN	A9	A8	A7	A6	A5	A4	A3	A1	A0
DIROUT*	1	0	1	1	1	1	0	1	1	1	X	X
	1	0	1	1	1	0	1	1	1	1	X	X
WPA*	0	1	1	1	1	1	0	1	1	1	0	0
	0	1	1	1	1	0	1	1	1	1	0	0
RPA*	1	0	1	1	1	1	0	1	1	1	0	0
	1	0	1	1	1	0	1	1	1	1	0	0
RPB*	1	0	1	1	1	1	0	1	1	1	0	1
	1	0	1	1	1	0	1	1	1	1	0	1
WPC*	0	1	1	1	1	1	0	1	1	1	1	0
	0	1	1	1	1	0	1	1	1	1	1	0
RPC*	1	0	1	1	1	1	0	1	1	1	1	0
	1	0	1	1	1	0	1	1	1	1	1	0
WPCNTRL*	0	1	1	0	1	0	0	0	0	0	X	X
	X = Don't care											

Chapter 6

Component Parts List

Introduction

This chapter of the service module contains a component view of the initial memory card (part numbers HE 181-4648, HE 181-4931-1, or HE 181-5304) and related parts list. Refer to Figure 6.1 for location of parts and components. The parts on the add-on memory card (HE 181-5307) common to both cards are in the same locations.

CAUTION: This card contains electrostatic-sensitive devices (ESD). Exercise extreme care when handling these devices to prevent damage.

Refer to Chapter 7, "Semiconductor Identification," or to the data sheet in Chapter 8 for descriptions of semiconductor devices.

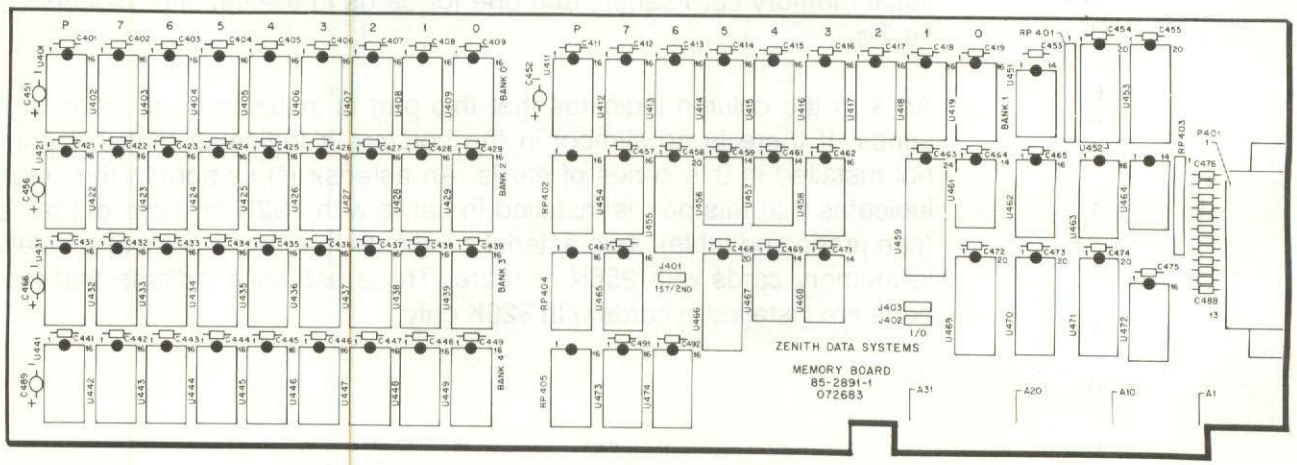


Figure 6.1. Memory Card Component Layout

Component Parts List

There are several cards in the memory card series. The four cards in the initial memory card series are all identical except for the amount of RAM memory chips installed. The second memory card is manufactured using the same bare (no components installed) card, but does not have the ICs used for the communication ports installed. The cards in the second card series differ from each other only in the amount of RAM memory installed. These card part numbers are as follows:

MEMORY SIZE	INITIAL MEMORY CARD PART NO.	SECOND MEMORY CARD PART NO.
128K	HE 181-4648	HE 181-5307
192K	HE 181-4931-1	NONE
256K	HE 181-5304	NONE
320K	HE 181-5324	HE 181-5446

In the following parts list, two columns are shown: one for cards in the initial memory card series, and one for cards in the second memory card series.

An X in the column indicates that this part is installed in all cards in the series. If there is no symbol in the column, it indicates that this part is not installed in this series of cards. An asterisk (*) symbol in the column indicates that this part is installed in cards with 192K or more of memory (see preceding table). Two asterisks indicate that these parts are installed in memory cards with 256K or more. Three asterisks indicate that these parts are installed in cards with 320K only.

Parts List

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION	INITIAL MEMORY CARD	ADD-ON MEMORY CARD
Capacitors				
C401	HE 21-786	.1 μF ceramic	X	X
C402	HE 21-786	.1 μF ceramic	X	X
C403	HE 21-786	.1 μF ceramic	X	X
C404	HE 21-786	.1 μF ceramic	X	X
C405	HE 21-786	.1 μF ceramic	X	X
C406	HE 21-786	.1 μF ceramic	X	X
C407	HE 21-786	.1 μF ceramic	X	X
C408	HE 21-786	.1 μF ceramic	X	X
C409	HE 21-786	.1 μF ceramic	X	X
C410	Not Used			
C411	HE 21-786	.1 μF ceramic	X	X
C412	HE 21-786	.1 μF ceramic	X	X
C413	HE 21-786	.1 μF ceramic	X	X
C414	HE 21-786	.1 μF ceramic	X	X
C415	HE 21-786	.1 μF ceramic	X	X
C416	HE 21-786	.1 μF ceramic	X	X
C417	HE 21-786	.1 μF ceramic	X	X
C418	HE 21-786	.1 μF ceramic	X	X
C419	HE 21-786	.1 μF ceramic	X	X
C420	Not Used			
C421	HE 21-786	.1 μF ceramic	X	X
C422	HE 21-786	.1 μF ceramic	X	X
C423	HE 21-786	.1 μF ceramic	X	X
C424	HE 21-786	.1 μF ceramic	X	X
C425	HE 21-786	.1 μF ceramic	X	X
C426	HE 21-786	.1 μF ceramic	X	X
C427	HE 21-786	.1 μF ceramic	X	X
C428	HE 21-786	.1 μF ceramic	X	X
C429	HE 21-786	.1 μF ceramic	X	X
C430	Not Used			
C431	HE 21-786	.1 μF ceramic	X	X
C432	HE 21-786	.1 μF ceramic	X	X
C433	HE 21-786	.1 μF ceramic	X	X
C434	HE 21-786	.1 μF ceramic	X	X
C435	HE 21-786	.1 μF ceramic	X	X

Component Parts List

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION	INITIAL MEMORY CARD	ADD-ON MEMORY CARD
Capacitors (Continued)				
C436	HE 21-786	.1 μF ceramic	X	X
C437	HE 21-786	.1 μF ceramic	X	X
C438	HE 21-786	.1 μF ceramic	X	X
C439	HE 21-786	.1 μF ceramic	X	X
C440	Not Used			
C441	HE 21-786	.1 μF ceramic	X	X
C442	HE 21-786	.1 μF ceramic	X	X
C443	HE 21-786	.1 μF ceramic	X	X
C444	HE 21-786	.1 μF ceramic	X	X
C445	HE 21-786	.1 μF ceramic	X	X
C446	HE 21-786	.1 μF ceramic	X	X
C447	HE 21-786	.1 μF ceramic	X	X
C448	HE 21-786	.1 μF ceramic	X	X
C449	HE 21-786	.1 μF ceramic	X	X
C450	Not Used			
C451	HE 25-252	15 μF tantalum	X	X
C452	HE 25-252	15 μF tantalum	X	X
C453	HE 21-786	.1 μF ceramic	X	X
C454	HE 21-786	.1 μF ceramic	X	X
C455	HE 21-786	.1 μF ceramic	X	X
C456	HE 25-252	15 μF tantalum	X	X
C457	HE 21-786	.1 μF ceramic	X	X
C458	HE 21-786	.1 μF ceramic	X	X
C459	HE 21-786	.1 μF ceramic	X	X
C460	Not Used			
C461	HE 21-786	.1 μF ceramic	X	X
C462	HE 21-786	.1 μF ceramic	X	X
C463	HE 21-786	.1 μF ceramic	X	X
C464	HE 21-786	.1 μF ceramic	X	X
C465	HE 21-786	.1 μF ceramic	X	X
C466	HE 25-252	15 μF tantalum	X	X
C467	HE 21-786	.1 μF ceramic	X	X
C468	HE 21-786	.1 μF ceramic	X	X
C469	HE 21-786	.1 μF ceramic	X	X
C470	Not Used			
C471	HE 21-786	.1 μF ceramic	X	X
C472	HE 21-786	.1 μF ceramic	X	X
C473	HE 21-786	.1 μF ceramic	X	X
C474	HE 21-786	.1 μF ceramic	X	X
C475	HE 21-786	.1 μF ceramic	X	X

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION	INITIAL MEMORY CARD	ADD-ON MEMORY CARD
Capacitors (Continued)				
C476	HE 21-763	330 pF ceramic	X	
C477	HE 21-763	330 pF ceramic	X	
C478	HE 21-763	330 pF ceramic	X	
C479	HE 21-763	330 pF ceramic	X	
C480	Not Used			
C481	HE 21-763	330 pF ceramic	X	
C482	HE 21-763	330 pF ceramic	X	
C483	HE 21-763	330 pF ceramic	X	
C484	HE 21-763	330 pF ceramic	X	
C485	HE 21-763	330 pF ceramic	X	
C486	HE 21-763	330 pF ceramic	X	
C487	HE 21-763	330 pF ceramic	X	
C488	HE 21-763	330 pF ceramic	X	
C489	HE 25-252	15 μF tantalum	X	X
C490	Not Used			
C491	HE 21-786	.1 μF ceramic	X	X
C491A	HE 21-147	47 pF	X	X
C492	HE 21-786	.1 μF ceramic	X	X
Interfaces and Jumpers				
J401	HE 432-1102	Pin, 3M MOLEX	X	X
	HE 432-1041	Pin, 2F BERG	X	X
J402	HE 432-1102	Pin, 3M MOLEX	X	
	HE 432-1041	Pin, 2F BERG	X	
J403	HE 432-1102	Pin, 3M MOLEX	X	
	HE 432-1041	Pin, 2F BERG	X	
P401	HE 432-1365	Connector, 25F Winchester D-Type	X	
	HE 255-757	Spacer, hex, threaded 4-40 × 4-40	X	
Resistors				
R401	HE 6-332-11	3.3 KΩ resistor		X
RP401	HE 9-133	4.7KΩ resistor pack	X	X
RP402	HE 9-154	47 Ω resistor pack	X	X
	HE 434-299	Socket	X	X
RP403	HE 9-133	4.7KΩ resistor pack	X	
RP404	HE 9-154	47 Ω resistor pack	X	X
	HE 434-299	Socket	X	X
RP405	HE 9-154	47 Ω resistor pack	X	X
	HE 434-299	Socket	X	X

Component Parts List

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION	INITIAL MEMORY CARD	ADD-ON MEMORY CARD
Integrated Circuits				
U401	HE 443-970	RAM 200 ns 64K × 1	X	X
	HE 434-299	Socket	X	X
U402	HE 443-970	RAM 200 ns 64K × 1	X	X
	HE 434-299	Socket	X	X
U403	HE 443-970	RAM 200 ns 64K × 1	X	X
	HE 434-299	Socket	X	X
U404	HE 443-970	RAM 200 ns 64K × 1	X	X
	HE 434-299	Socket	X	X
U405	HE 443-970	RAM 200 ns 64K × 1	X	X
	HE 434-299	Socket	X	X
U406	HE 443-970	RAM 200 ns 64K × 1	X	X
	HE 434-299	Socket	X	X
U407	HE 443-970	RAM 200 ns 64K × 1	X	X
	HE 434-299	Socket	X	X
U408	HE 443-970	RAM 200 ns 64K × 1	X	X
	HE 434-299	Socket	X	X
U409	HE 443-970	RAM 200 ns 64K × 1	X	X
	HE 434-299	Socket	X	X
U410	Not Used			
U411	HE 443-970	RAM 200 ns 64K × 1	X	X
	HE 434-299	Socket	X	X
U412	HE 443-970	RAM 200 ns 64K × 1	X	X
	HE 434-299	Socket	X	X
U413	HE 443-970	RAM 200 ns 64K × 1	X	X
	HE 434-299	Socket	X	X
U414	HE 443-970	RAM 200 ns 64K × 1	X	X
	HE 434-299	Socket	X	X
U415	HE 443-970	RAM 200 ns 64K × 1	X	X
	HE 434-299	Socket	X	X
U416	HE 443-970	RAM 200 ns 64K × 1	X	X
	HE 434-299	Socket	X	X
U417	HE 443-970	RAM 200 ns 64K × 1	X	X
	HE 434-299	Socket	X	X
U418	HE 443-970	RAM 200 ns 64K × 1	X	X
	HE 434-299	Socket	X	X
U419	HE 443-970	RAM 200 ns 64K × 1	X	X
	HE 434-299	Socket	X	X

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION	INITIAL MEMORY CARD	ADD-ON MEMORY CARD
Integrated Circuits (Continued)				
U420	Not Used			
U421	HE 443-970	RAM 200 ns 64K × 1	*	*
	HE 434-299	Socket	X	X
U422	HE 443-970	RAM 200 ns 64K × 1	*	*
	HE 434-299	Socket	X	X
U423	HE 443-970	RAM 200 ns 64K × 1	*	*
	HE 434-299	Socket	X	X
U424	HE 443-970	RAM 200 ns 64K × 1	*	*
	HE 434-299	Socket	X	X
U425	HE 443-970	RAM 200 ns 64K × 1	*	*
	HE 434-299	Socket	X	X
U426	HE 443-970	RAM 200 ns 64K × 1	*	*
	HE 434-299	Socket	X	X
U427	HE 443-970	RAM 200 ns 64K × 1	*	*
	HE 434-299	Socket	X	X
U428	HE 443-970	RAM 200 ns 64K × 1	*	*
	HE 434-299	Socket	X	X
U429	HE 443-970	RAM 200 ns 64K × 1	*	*
	HE 434-299	Socket	X	X
U430	Not Used			
U431	HE 443-970	RAM 200 ns 64K × 1	**	**
	HE 434-299	Socket	X	X
U432	HE 443-970	RAM 200 ns 64K × 1	**	**
	HE 434-299	Socket	X	X
U433	HE 443-970	RAM 200 ns 64K × 1	**	**
	HE 434-299	Socket	X	X
U434	HE 443-970	RAM 200 ns 64K × 1	**	**
	HE 434-299	Socket	X	X
U435	HE 443-970	RAM 200 ns 64K × 1	**	**
	HE 434-299	Socket	X	X
U436	HE 443-970	RAM 200 ns 64K × 1	**	**
	HE 434-299	Socket	X	X
U437	HE 443-970	RAM 200 ns 64K × 1	**	**
	HE 434-299	Socket	X	X

*Installed on all cards in the series.
*Installed on cards with 192K or more. Refer to beginning of this chapter for part number.
**Installed on cards with 256K or more.
***Installed only on 320K cards.

Component Parts List

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION	INITIAL MEMORY CARD	ADD-ON MEMORY CARD
Integrated Circuits (Continued)				
U438	HE 443-970	RAM 200 ns 64K × 1	**	**
	HE 434-299	Socket	X	X
U439	HE 443-970	RAM 200 ns 64K × 1	**	**
	HE 434-299	Socket	X	X
U440	Not Used			
U441	HE 443-970	RAM 200 ns 64K × 1	***	***
	HE 434-299	Socket	X	X
U442	HE 443-970	RAM 200 ns 64K × 1	***	***
	HE 434-299	Socket	X	X
U443	HE 443-970	RAM 200 ns 64K × 1	***	***
	HE 434-299	Socket	X	X
U444	HE 443-970	RAM 200 ns 64K × 1	***	***
	HE 434-299	Socket	X	X
U445	HE 443-970	RAM 200 ns 64K × 1	***	***
	HE 434-299	Socket	X	X
U446	HE 443-970	RAM 200 ns 64K × 1	***	***
	HE 434-299	Socket	X	X
U447	HE 443-970	RAM 200 ns 64K × 1	***	***
	HE 434-299	Socket	X	X
U448	HE 443-970	RAM 200 ns 64K × 1	***	***
	HE 434-299	Socket	X	X
U449	HE 443-970	RAM 200 ns 64K × 1	***	***
	HE 434-299	Socket	X	X
U450	Not Used			
U451	HE 443-1001	Parity checker, odd/even	X	X
	HE 434-298	Socket	X	X
U452	HE 443-791	Buffer/driver, tri-state	X	
	HE 434-311	Socket	X	
U453	HE 443-863	Flip-flop, octal, D, tri-state	X	
	HE 434-311	Socket	X	
U454	HE 443-1024	Inverter, hex, tri-state	X	X
	HE 434-299	Socket	X	X
U455	HE 444-224	Decoder, memory	X	X
	HE 434-311	Socket	X	X

*Installed on all cards in the series.
*Installed on cards with 192K or more. Refer to beginning of this chapter for part number.
**Installed on cards with 256K or more.
***Installed only on 320K cards.

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION	INITIAL MEMORY CARD	ADD-ON MEMORY CARD
Integrated Circuits (Continued)				
U456	HE 41-14	Delay line, 100 ns, tapped	X	X
	HE 434-298	Socket	X	X
U457	HE 443-728	NAND, quad, 2-input	X	X
	or			
	HE 443-1080			
	HE 434-298	Socket	X	X
U458	HE 443-879	Flip-flop, hex, D	X	X
	HE 434-299	Socket	X	X
U459	HE 444-225	Controller, printer	X	X
	HE 434-368	Socket	X	X
U460	Not Used			
U461	HE 443-872	Inverter, hex	X	
	HE 434-298	Socket	X	
U462	HE 443-857	Buffer, hex, tri-state	X	
	HE 434-299	Socket	X	
U463	HE 443-1024	Inverter, hex, tri-state	X	
	HE 434-299	Socket	X	
U464	HE 443-967	Inverter, hex	X	X
	HE 434-298	Socket	X	X
U465	HE 443-1178	Multiplexer, quad	X	X
	or			
	HE 443-1254			
	or			
	HE 443-1120			
	HE 434-299	Socket	X	X
U466	Not Used			
U467	HE 443-875	OR, quad, 2-input	X	X
	or			
	HE 443-1072			
	HE 434-298	Socket	X	X
U468	HE 443-730	Flip-flop, dual, D	X	X
	or			
	HE 443-1051			
	HE 434-298	Socket	X	X
U469	HE 443-754	Buffer, octal, tri-state	X	X
	HE 434-311	Socket	X	X
U470	HE 443-1174	Bus transceiver, octal	X	X
	HE 434-311	Socket	X	X
U471	HE 443-885	Transceiver	X	X
	HE 434-311	Socket	X	X

Component Parts List

CIRCUIT REFERENCE DESIGNATOR	ZDS PART NO.	DESCRIPTION	INITIAL MEMORY CARD	ADD-ON MEMORY CARD
Integrated Circuits (Continued)				
U472	HE 443-879	Flip-flop, hex, D	X	
	HE 434-299	Socket	X	
U473	HE 443-1178 or HE 443-1254 or HE 443-1120	Multiplexer, quad	X	X
	HE 434-299	Socket	X	X
U474	HE 443-1178 or HE 443-1254 or HE 443-1120	Multiplexer, quad	X	X
	HE 434-299	Socket	X	X
Miscellaneous				
	HE 204-2754	Bracket, mounting, PCB	X	
	HE 254-7	Lock washer	X	
	HE 255-757	Studded screw	X	
	HE 250-1411	Screw, pan head, Phillips, 4-40 × .250, 2 each	X	X
	HE 204-2797	Bracket, mounting, PCB		X

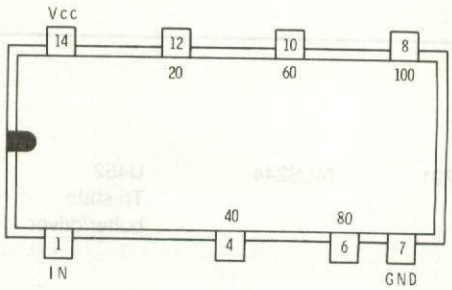
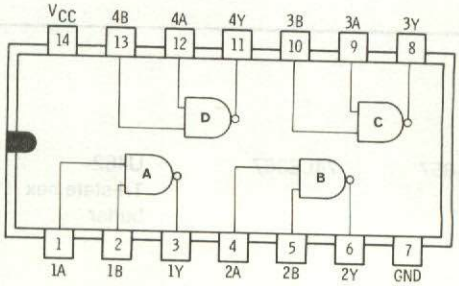
Chapter 7

Semiconductor Identification

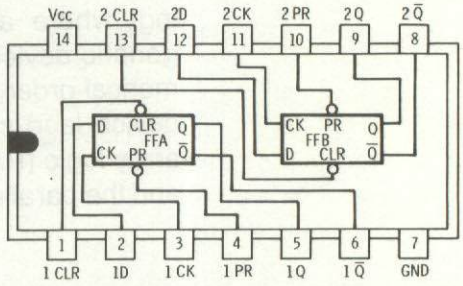
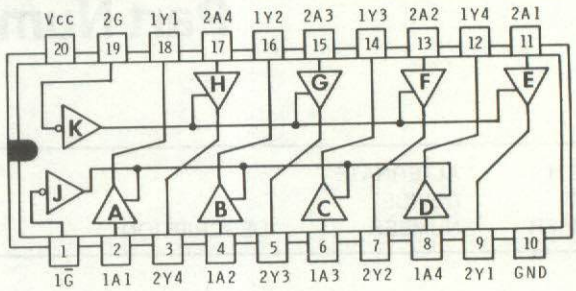
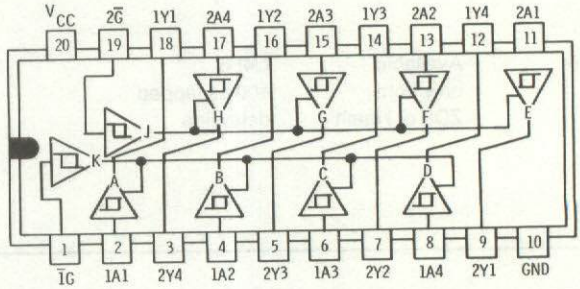
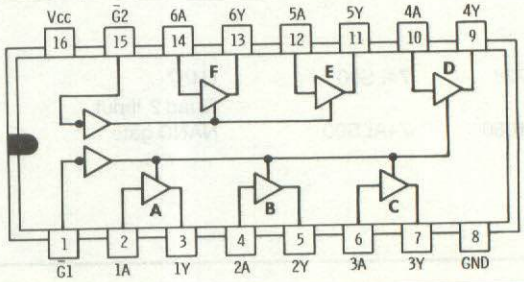
Introduction

This chapter of the service module aids you in identifying the various semiconductor devices (ICs) used on the memory cards by cross-referencing, where applicable, the Zenith/Heath part numbers with alternate/generic device numbers. The IC components are listed in ascending numerical order, along with alternate device number (where applicable), and device lead configuration. This chapter also includes the programmable array logic (PAL) equations for the two decoders used for memory access and the parallel interface.

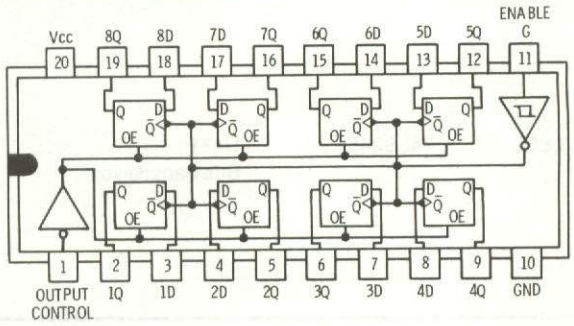
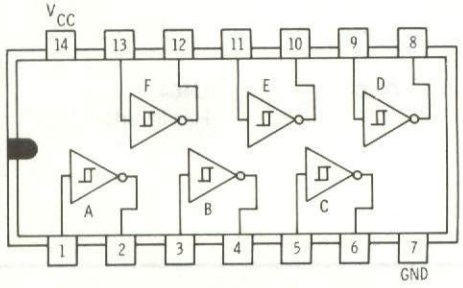
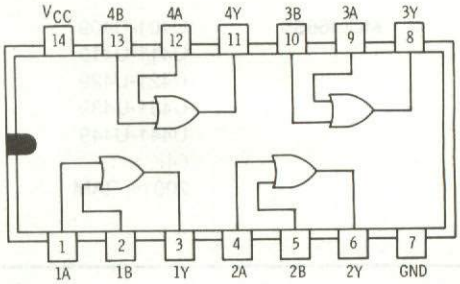
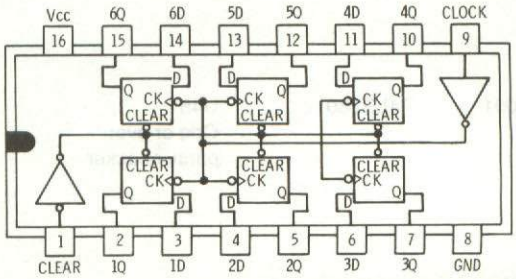
Part Number Index

HEATH PART NUMBER	ALTERNATE DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
41-14	Available only from ZDS or Heath	U456 100 ns tapped delay line	
443-728 or 443-1080	74LS00 74ALS00	U457 Quad 2-input NAND gate	

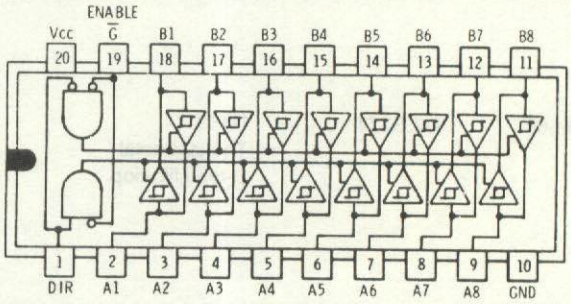
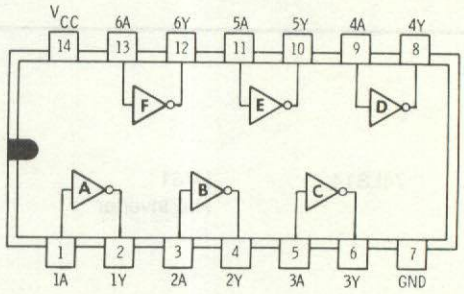
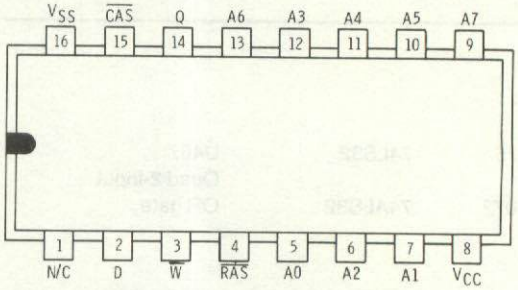
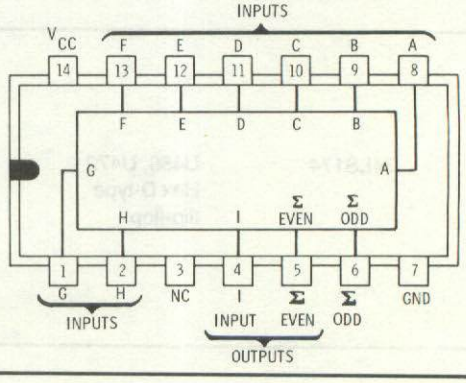
Semiconductor Identification

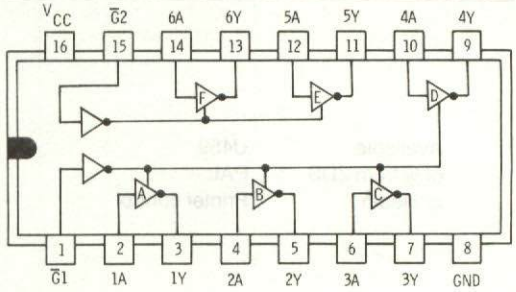
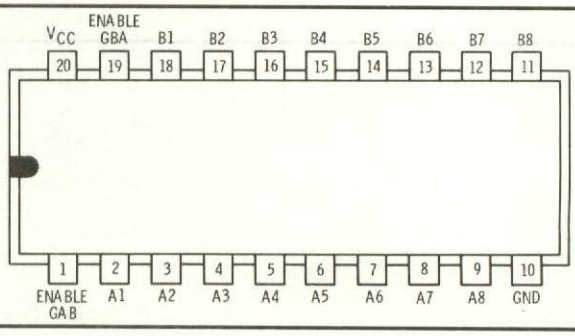
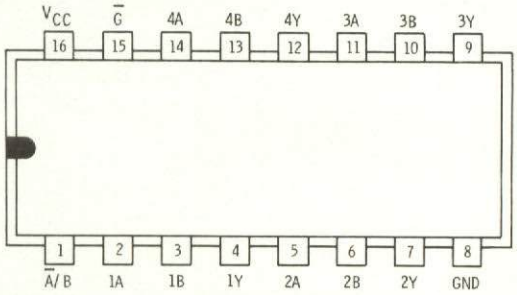
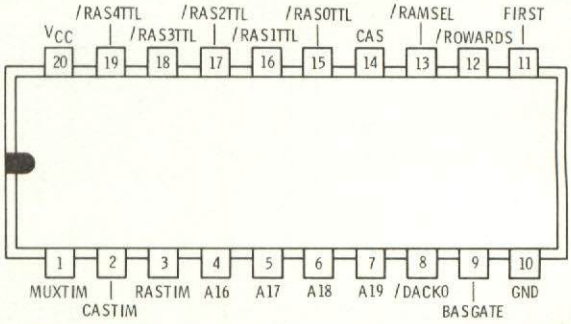
HEATH PART NUMBER	ALTERNATE DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
443-730 or 443-1051	74LS74 74ALS74	U468 Dual D-type flip-flop	
443-754	74LS240	U469 Tri-state octal buffer	
443-791	74LS244	U452 Tri-state buffer/driver	
443-857	74LS367	U462 Tri-state hex buffer	

Semiconductor Identification

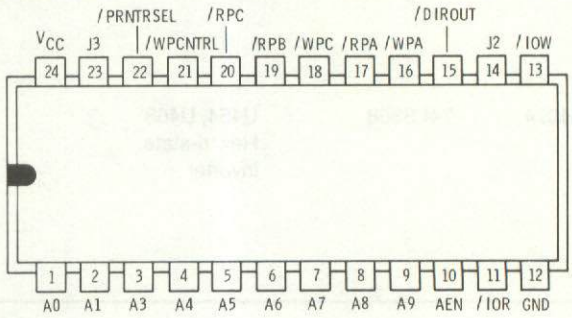
HEATH PART NUMBER	ALTERNATE DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
443-863	74LS374	U453 Tri-state octal D-type flip-flop	
443-872	74LS14	U461 Hex inverter	
443-875 or 443-1072	74LS32 74ALS32	U467 Quad 2-input OR gate	
443-879	74LS174	U458, U472 Hex D-type flip-flop	

Semiconductor Identification

HEATH PART NUMBER	ALTERNATE DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
443-885	74LS245	U471 Bus transceiver	
443-967	7406	U464 Hex inverter	
443-970	MCM6665	U401-U409 U411-U419 U421-U429 U431-U439 U441-U449 64K × 1, 200 ns RAM	
443-1001	74LS280	U451 Odd or even parity checker	

HEATH PART NUMBER	ALTERNATE DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
443-1024	74LS368	U454, U463 Hex tri-state inverter	
443-1174	74LS623	U470 Octal bus transceiver	
443-1178 or 443-1254 or 443-1120	74ALS257 74AS257 74F257	U465, U473, U474 Quad multiplexer	
444-224	Available only from ZDS or Heath	U455 PAL Memory decoder	

Semiconductor Identification

HEATH PART NUMBER	ALTERNATE DEVICE NUMBER	DESCRIPTION	LEAD CONFIGURATION
444-225	Available only from ZDS or Heath	U459 PAL Printer control	

PAL Equations

This section contains the logic equations for the two programmable array logic (PAL) devices resident on the memory cards. Detailed circuit operation for these devices is covered in the dynamic memory access and parallel interface descriptions in Chapter 4.

The 16L8 PAL equations determine specific memory access operations according to the following logic:

```
IF(Vcc)RAS0TTL = FIRST*/A19*/A18*/A17*/A16*RASTIM
                 +/FIRST*/A19*A18*/A17*A16*RASTIM
                 +DACK0*RASTIM

IF(Vcc)RAS1TTL = FIRST*/A19*/A18*/A17*A16*RASTIM
                 +/FIRST*/A19*A18*A17*/A16*RASTIM
                 +DACK0*MUXTIM

IF(Vcc)RAS2TTL = FIRST*/A19*/A18*A17*/A16*RASTIM
                 +/FIRST*/A19*A18*A17*A16*RASTIM
                 +DACK0*MUXTIM

IF(Vcc)RAS3TTL = FIRST*/A19*/A18*A17*A16*RASTIM
                 +/FIRST*A19*/A18*/A17*/A16*RASTIM
                 +DACK0*RASTIM

IF(Vcc)RAS4TTL = FIRST*/A19*A18*/A17*/A16*RASTIM
                 +/FIRST*A19*/A18*/A17*A16*RASTIM
                 +DACK0*MUXTIM

IF(Vcc)/CAS = /CASTIM+/RASTIM+/CASGATE+DACK0+/RAMSEL

IF(Vcc)ROWADRS = /MUXTIM+DACK0

IF(Vcc)RAMSEL = FIRST*/A19*/A18*/DACK0
                +FIRST*/A19*A18*/A17*/A16*/DACK0
                +/FIRST*/A19*A18*/A17*A16*/DACK0
                +/FIRST*/A19*A18*A17*/DACK0
                +/FIRST*A19*/A18*/A17*/DACK0
```

The 14L8 PAL determines parallel port data latch, buffer data transfer, or bus driver selection according to the following logic: (Only the /WPCNTRL function applies to the add-on memory card.)

```
/DIROUT = /J3*/J2*A9*A8*A7*/A6*A5*A4*A3*/AEN*IOR
        + /J3*J2*A9*A8*/A7*A6*A5*A4*A3*/AEN*IOR

/WPA = /J3*/J2*A9*A8*A7*/A6*A5*A4*A3*/AEN*/A1*/A0*IOW
     + /J3*J2*A9*A8*/A7*A6*A5*A4*A3*/AEN*/A1*/A0*IOW

/WPC = /J3*/J2*A9*A8*A7*/A6*A5*A4*A3*/AEN*A1*/A0*IOW
     + /J3*J2*A9*A8*/A7*A6*A5*A4*A3*/AEN*A1*/A0*IOW

/RPA = /J3*/J2*A9*A8*A7*/A6*A5*A4*A3*/AEN*/A1*/A0*IOR
     + /J3*J2*A9*A8*/A7*A6*A5*A4*A3*/AEN*/A1*/A0*IOR

/RPB = /J3*/J2*A9*A8*A7*/A6*A5*A4*A3*/AEN*/A1*A0*IOR
     + /J3*J2*A9*A8*/A7*A6*A5*A4*A3*/AEN*/A1*A0*IOR

/RPC = /J3*/J2*A9*A8*A7*/A6*A5*A4*A3*/AEN*A1*/A0*IOR
     + /J3*J2*A9*A8*/A7*A6*A5*A4*A3*/AEN*A1*/A0*IOR

/WPCNTRL = /A9*A8*/A7*/A6*/A5*/A4*/A3*/A1*/A0*/AEN*IOW
```

where the following functions are represented by the PAL equation symbols:

PAL SYMBOL	LOGIC FUNCTION
/	Complement
*	AND
=	Equals
+	OR

Chapter 8

Data Sheets

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P.O. Box 20924
Phoenix, Arizona 85036

MOTOROLA

MCM6665A

MOS
(N-CHANNEL, SILICON-GATE)

65,536-BIT DYNAMIC RANDOM ACCESS MEMORY

64K BIT DYNAMIC RAM

The MCM6665A is a 65,536 bit, high-speed, dynamic Random-Access Memory. Organized as 65,536 one-bit words and fabricated using HMOS high-performance N-channel silicon-gate technology, this new breed of 5-volt only dynamic RAM combines high performance with low cost and improved reliability.

By multiplexing row- and column-address inputs, the MCM6665A requires only eight address lines and permits packaging in standard 16-pin dual-in-line packages. Complete address decoding is done on chip with address latches incorporated. Data out is controlled by $\overline{CAS}$ allowing for greater system flexibility.

All inputs and outputs, including clocks, are fully TTL compatible. The MCM6665A incorporates a one-transistor cell design and dynamic storage techniques.

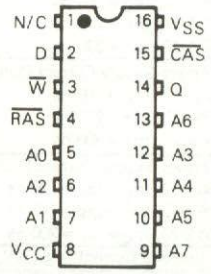
- Organized as 65,536 Words of 1 Bit
- Single +5 V Operation (±10%)
- Full Power Supply Range Capabilities
- Maximum Access Time
  - MCM6665A-12 = 120 ns
  - MCM6665A-15 = 150 ns
  - MCM6665A-20 = 200 ns
- Low Power Dissipation
  - 302.5 mW Maximum (Active) (MCM6665A-15)
  - 22 mW Maximum (Standby)
- Three-State Data Output
- Internal Latches for Address and Data Input
- Early-Write Common I/O Capability
- 16K Compatible 128-Cycle, 2 ms Refresh
- $\overline{RAS}$-only Refresh Mode
- $\overline{CAS}$ Controlled Output
- Upward Pin Compatible from the 16K RAM (MCM4116, MCM4517)
- Fast Page Mode Cycle Time
- Low Soft Error Rate <0.1% per 1000 Hours (See Soft Error Testing)

P SUFFIX
PLASTIC PACKAGE
CASE 648

L SUFFIX
CERAMIC PACKAGE
CASE 690

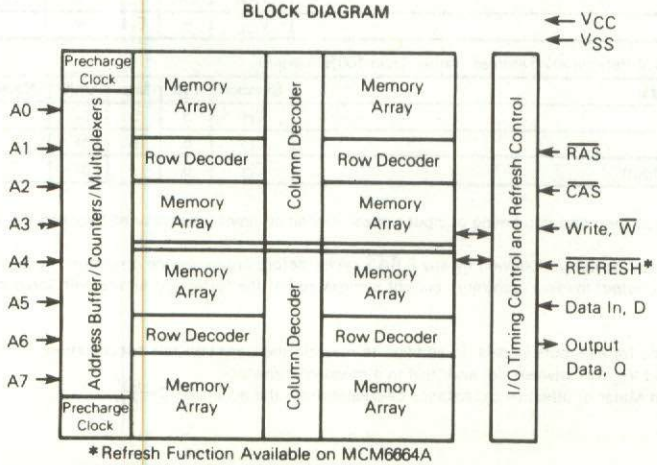
Z SUFFIX, CERAMIC PACKAGE ALSO AVAILABLE — CASE 752A

PIN ASSIGNMENT



PIN NAMES	
A0-A7	Address Input
D	Data In
Q	Data Out
$\overline{W}$	Read/Write Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5 V)
V_{SS}	Ground

BLOCK DIAGRAM



*Refresh Function Available on MCM6664A

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

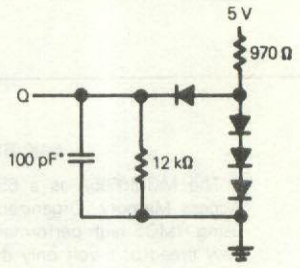
MCM6665A

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{SS} (except V_{CC})	V_{in}, V_{out}	−2 to +7	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	−1 to +7	V
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Power Dissipation	P_D	1.0	W
Data Out Current	I_{out}	50	mA

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

FIGURE 1 — OUTPUT LOAD



*Includes Jig Capacitance

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	MCM6665A-12, -15, -20	V_{CC}	4.5	5.0	5.5	V	1
		V_{SS}	0	0	0	V	1
Logic 1 Voltage, All Inputs		V_{IH}	2.4	–	V_{CC}+1	V	1
Logic 0 Voltage, All Inputs		V_{IL}	−1.0*	–	0.8	V	1

*The device will withstand undershoots to the −2 volt level with a maximum pulse width of 20 ns at the −1.5 volt level. This is periodically sampled rather than 100% tested.

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Units	Notes
V_{CC} Power Supply Current (Standby)	I_{CC2}	–	4.0	mA	5
V_{CC} Power Supply Current					
6665A-12, t_{RC} = 250 ns	I_{CC1}	–	60	mA	4
6665A-15, t_{RC} = 270 ns		–	55		
6665A-20, t_{RC} = 330 ns		–	50		
V_{CC} Power Supply Current During $\overline{RAS}$ only Refresh Cycles					
6665A-12, t_{RC} = 250 ns	I_{CC3}	–	50	mA	4
6665A-15, t_{RC} = 270 ns		–	45		
6665A-20, t_{RC} = 330 ns		–	40		
V_{CC} Power Supply Current During Page Mode Cycle for t_{RAS} = 10 μsec					
6665A-12, t_{PC} = t_{RP} = 120 ns	I_{CC4}	–	45	mA	4
6665A-15, t_{PC} = t_{RP} = 145 ns		–	40		
6665A-20, t_{PC} = t_{RP} = 200 ns		–	35		
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)	$I_{I(L)}$	–	10	μA	–
Output Leakage Current ($\overline{CAS}$ at logic 1, $V_{SS} \le V_{out} \le V_{CC}$)	$I_{O(L)}$	–	10	μA	–
Output Logic 1 Voltage @ I_{out} = −4 mA	V_{OH}	2.4	–	V	–
Output Logic 0 Voltage @ I_{out} = 4 mA	V_{OL}	–	0.4	V	–

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit	Notes
Input Capacitance (A0-A7), D	C_{I1}	3	5	pF	7
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	6	8	pF	7
Output Capacitance (Q), ($\overline{CAS}$ = V_{IH} to disable output)	C_O	5	7	pF	7

NOTES:
1. All voltages referenced to V_{SS}.
2. V_{IH} min and V_{IL} max are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
3. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
4. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
5. $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1.
6. The transition time specification applies for all inputs signals. In addition to meeting the transition rate specification, all input signals must transmit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
7. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I\Delta t}{\Delta V}$

MCM6665A

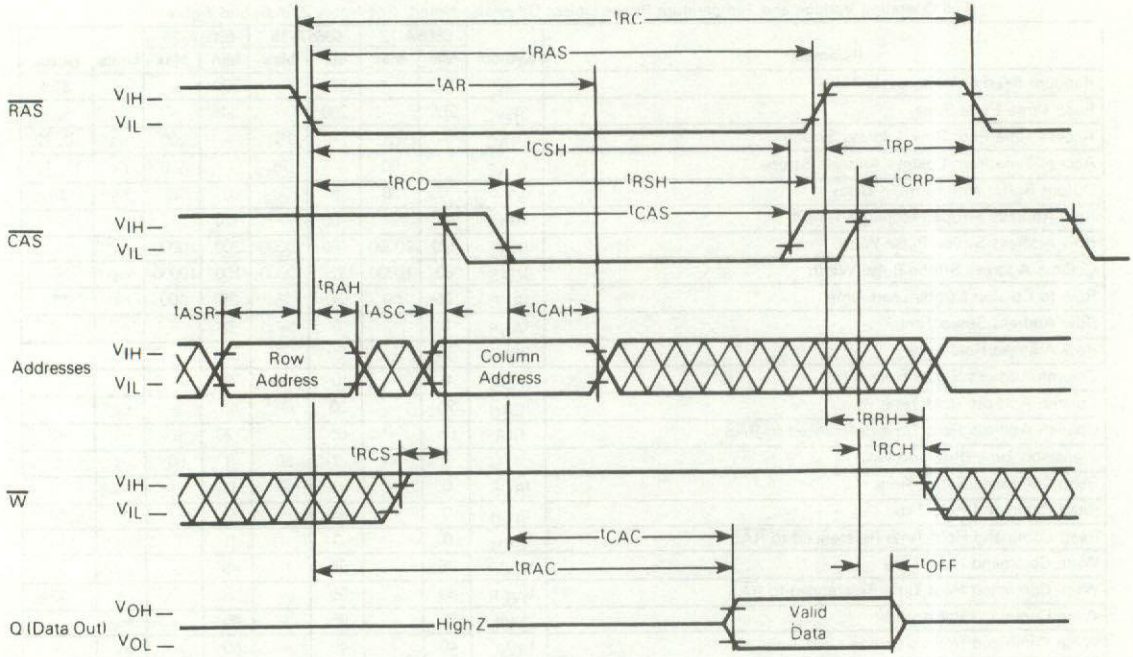
AC OPERATING CONDITIONS AND CHARACTERISTICS (Read, Write, and Read-Modify-Write Cycles)
(Full Operating Voltage and Temperature Range Unless Otherwise Noted; See Notes 2, 3, 6, and Figure 1)

Parameter	Symbol	6665A-12		6665A-15		6665A-20		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	250	–	270	–	330	–	ns	8, 9
Read Write Cycle Time	t_{RWC}	255	–	280	–	345	–	ns	8, 9
Access Time from Row Address Strobe	t_{RAC}	–	120	–	150	–	200	ns	10, 12
Access Time from Column Address Strobe	t_{CAC}	–	60	–	75	–	100	ns	11, 12
Output Buffer and Turn-Off Delay	t_{OFF}	0	30	0	30	0	40	ns	18
Row Address Strobe Precharge Time	t_{RP}	100	–	100	–	120	–	ns	–
Row Address Strobe Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	–
Column Address Strobe Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns	–
Row to Column Strobe Lead Time	t_{RCD}	25	60	30	75	35	100	ns	13
Row Address Setup Time	t_{ASR}	0	–	0	–	0	–	ns	–
Row Address Hold Time	t_{RAH}	15	–	20	–	25	–	ns	–
Column Address Setup Time	t_{ASC}	0	–	0	–	0	–	ns	–
Column Address Hold Time	t_{CAH}	25	–	35	–	45	–	ns	–
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	85	–	95	–	120	–	ns	17
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	ns	–
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	ns	14
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	ns	14
Write Command Hold Time	t_{WCH}	25	–	35	–	45	–	ns	–
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	85	–	95	–	120	–	ns	17
Write Command Pulse Width	t_{WP}	25	–	35	–	45	–	ns	–
Write Command to Row Strobe Lead Time	t_{RWL}	40	–	45	–	55	–	ns	–
Write Command to Column Strobe Lead Time	t_{CWL}	40	–	45	–	55	–	ns	–
Data in Setup Time	t_{DS}	0	–	0	–	0	–	ns	15
Data in Hold Time	t_{DH}	25	–	35	–	45	–	ns	15
Data in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	85	–	95	–	120	–	ns	17
Column to Row Strobe Precharge Time	t_{CRP}	−10	–	−10	–	−10	–	ns	–
$\overline{RAS}$ Hold Time	t_{RSH}	60	–	75	–	100	–	ns	–
Refresh Period	t_{RFSH}	–	2.0	–	2.0	–	2.0	ms	–
$\overline{WRITE}$ Command Setup Time	t_{WCS}	−10	–	−10	–	−10	–	ns	16
$\overline{CAS}$ to $\overline{WRITE}$ Delay	t_{CWD}	40	–	45	–	55	–	ns	16
$\overline{RAS}$ to $\overline{WRITE}$ Delay	t_{RWD}	100	–	120	–	155	–	ns	16
$\overline{CAS}$ Hold Time	t_{CSH}	120	–	150	–	200	–	ns	–
$\overline{CAS}$ Precharge Time (Page Mode Cycle Only)	t_{CP}	50	–	60	–	80	–	ns	–
Page Mode Cycle Time	t_{PC}	120	–	145	–	200	–	ns	–

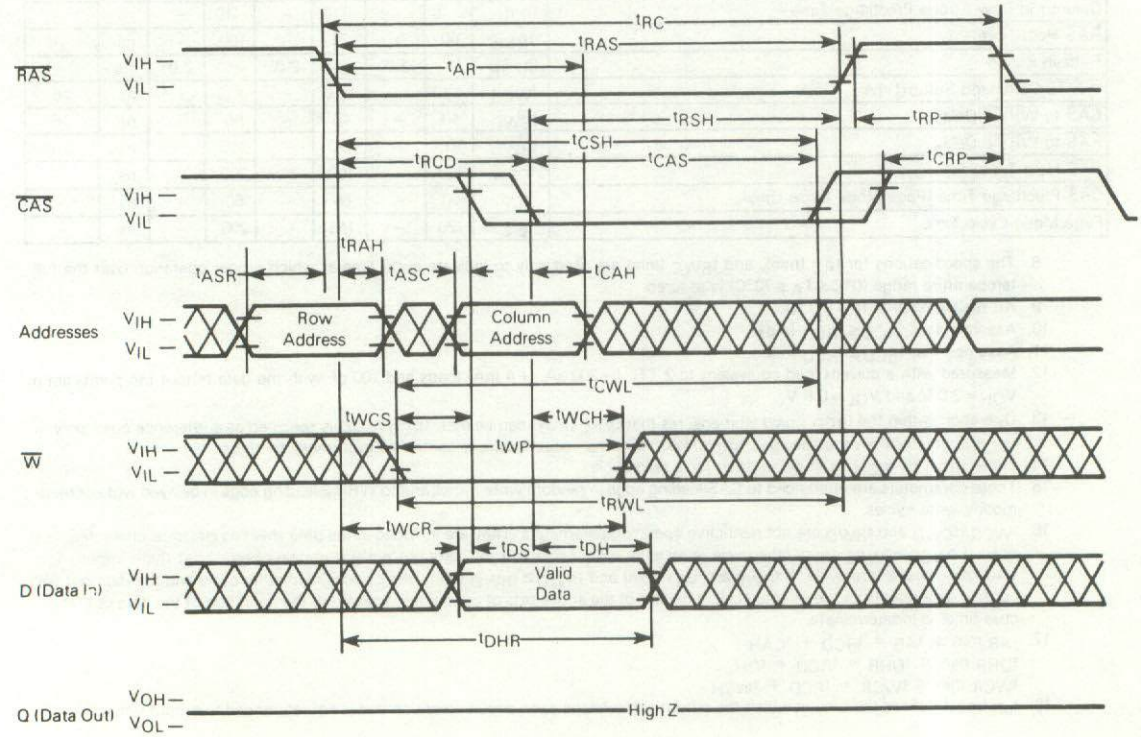
8. The specifications for t_{RC} (min), and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
9. AC measurements $t_T = 5.0$ ns.
10. Assumes that $t_{RCD} \le t_{RCD}$ (max).
11. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
12. Measured with a current load equivalent to 2 TTL (−200 μA, +4 mA) loads and 100 pF with the data output trip points set at $V_{OH} = 2.0$ V and $V_{OL} = 0.8$ V.
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \ge t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \ge t_{CWD}$ (min) and $t_{RWD} \ge t_{RWD}$ (min), the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
17. $t_{AR\ min} \le t_{AR} = t_{RCD} + t_{CAH}$
$t_{DHR\ min} \le t_{DHR} = t_{RCD} + t_{DH}$
$t_{WCR\ min} \le t_{WCR} = t_{RCD} + t_{WCH}$
18. t_{off} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

MCM6665A

READ CYCLE TIMING

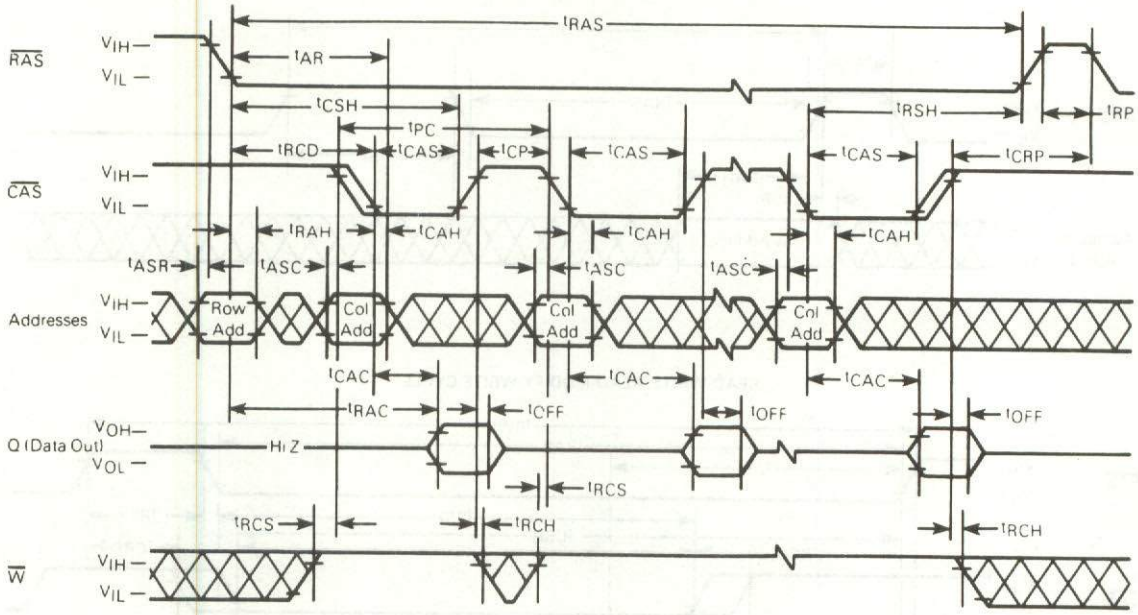


WRITE CYCLE TIMING

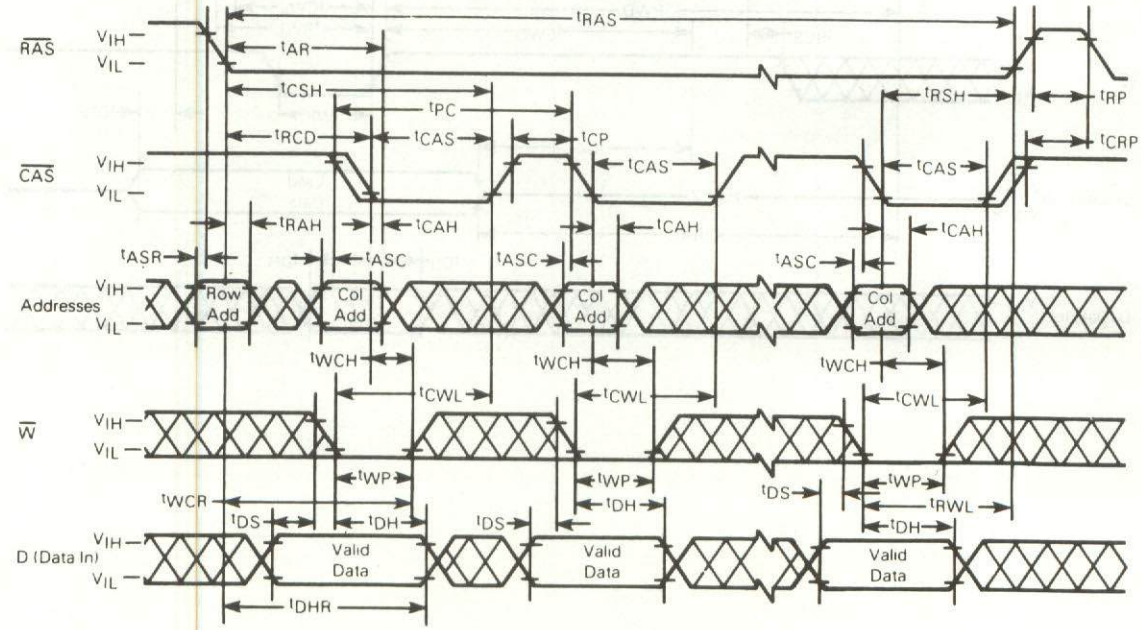


MCM6665A

PAGE MODE READ CYCLE

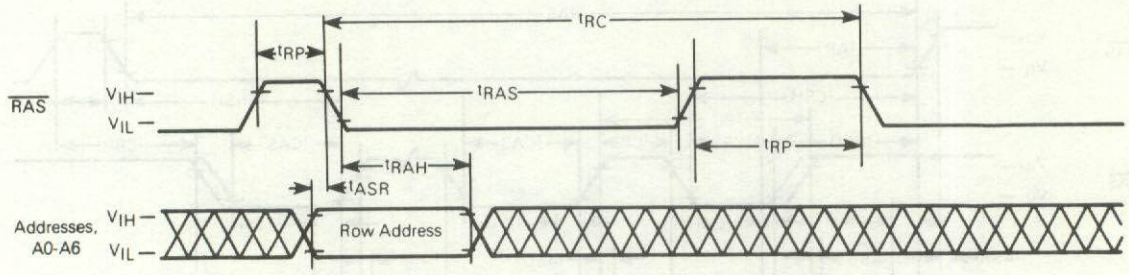


PAGE MODE WRITE CYCLE

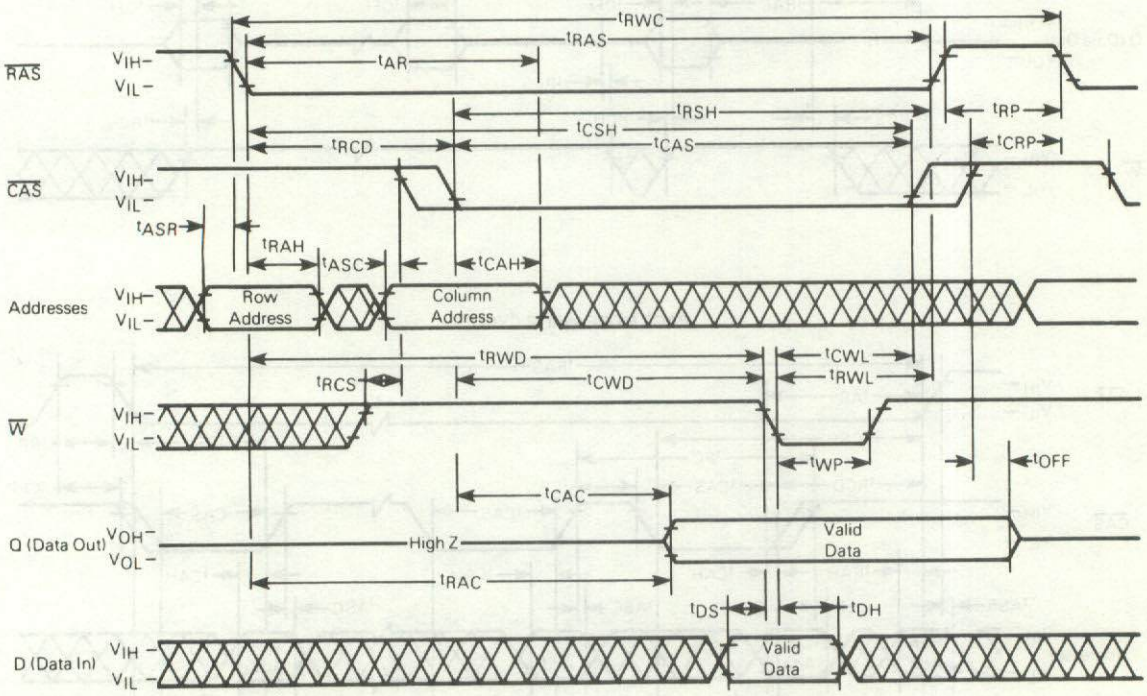


MCM6665A

$\overline{RAS}$-ONLY REFRESH CYCLE
(Data-in and $\overline{Write}$ are Don't Care, $\overline{CAS}$ is HIGH)



READ-WRITE/READ-MODIFY-WRITE CYCLE



TYPICAL CHARACTERISTICS

FIGURE 2 – $\overline{RAS}$ ACCESS TIME versus SUPPLY VOLTAGE

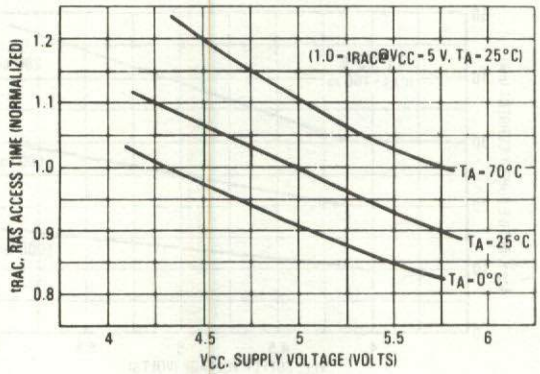


FIGURE 3 – $\overline{CAS}$ ACCESS TIME versus SUPPLY VOLTAGE

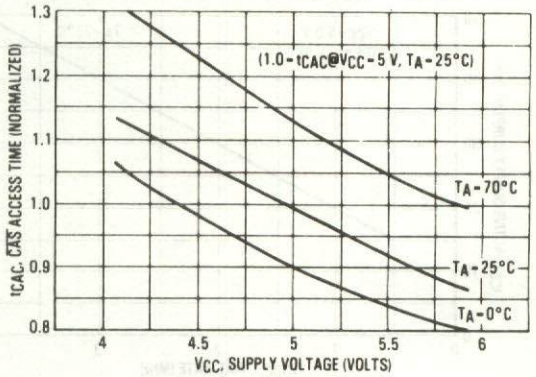


FIGURE 4 – $\overline{RAS}$ ACCESS TIME versus AMBIENT TEMPERATURE

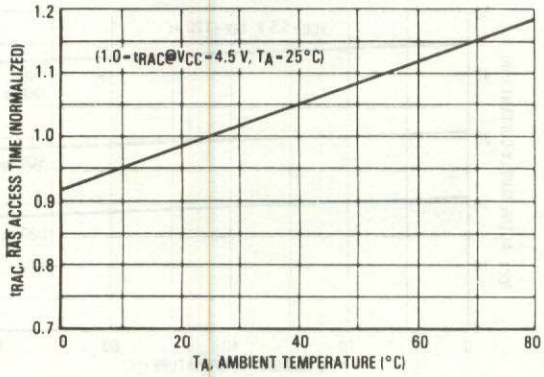


FIGURE 5 – $\overline{CAS}$ ACCESS TIME versus AMBIENT TEMPERATURE

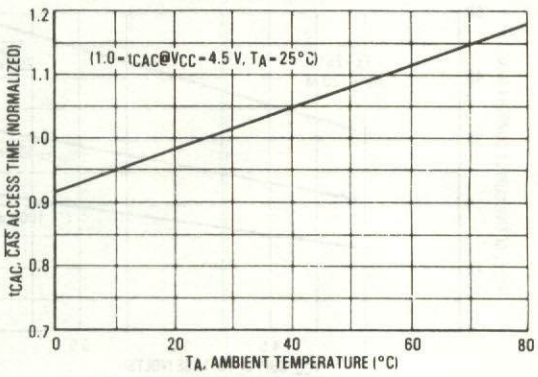


FIGURE 6 – $\overline{RAS}$, $\overline{W}$ INPUT LEVEL versus SUPPLY VOLTAGE

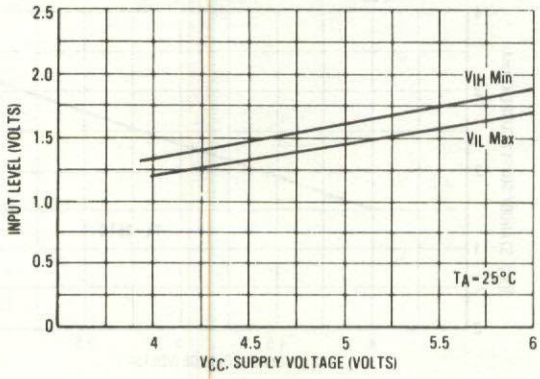
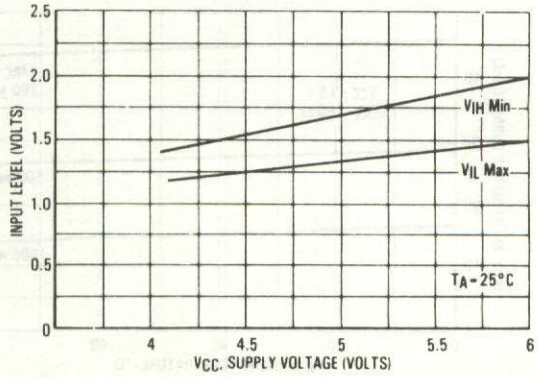


FIGURE 7 – $\overline{CAS}$, $\overline{W}$ INPUT LEVEL versus SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

FIGURE 8 – I_{CC1} SUPPLY CURRENT versus CYCLE RATE

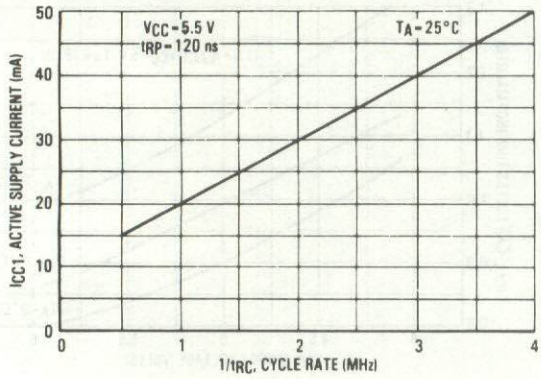


FIGURE 9 – I_{CC1} SUPPLY CURRENT versus SUPPLY VOLTAGE

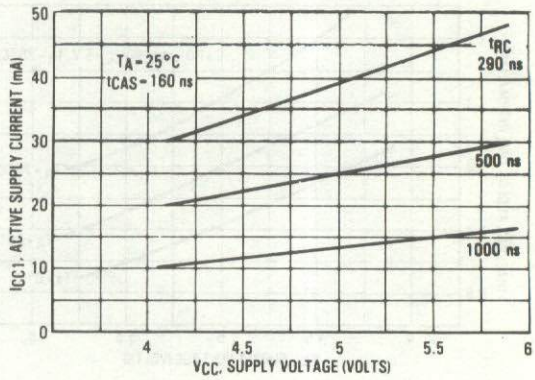


FIGURE 10 – I_{CC1} SUPPLY CURRENT versus SUPPLY VOLTAGE

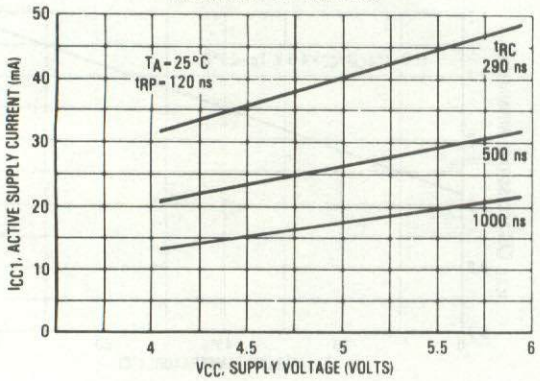


FIGURE 11 – I_{CC1} SUPPLY CURRENT versus AMBIENT TEMPERATURE (min t_{RP})

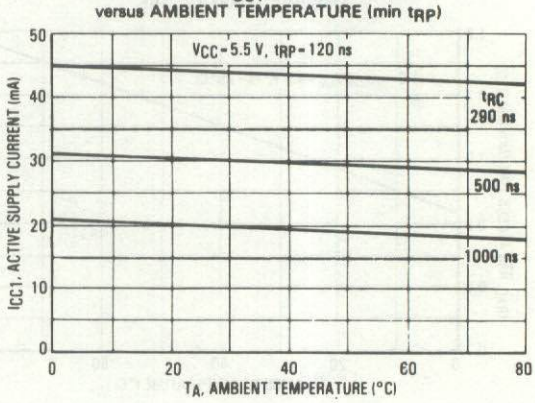


FIGURE 12 – I_{CC1} SUPPLY CURRENT versus AMBIENT TEMPERATURE (min $\overline{RAS}$)

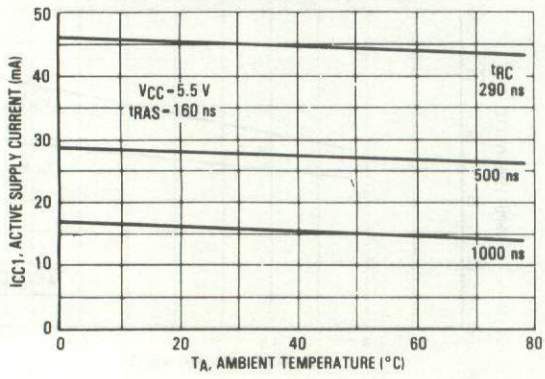
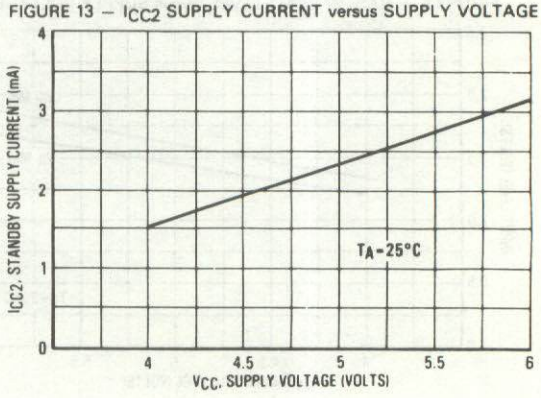


FIGURE 13 – I_{CC2} SUPPLY CURRENT versus SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS (continued)

FIGURE 14 – I_{CC2} STANDBY CURRENT versus AMBIENT TEMPERATURE

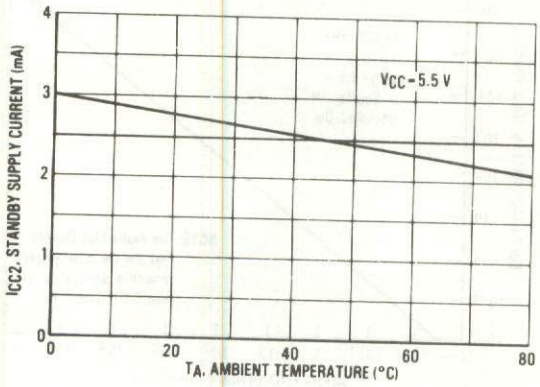


FIGURE 15 – I_{CC3} SUPPLY CURRENT versus CYCLE RATE

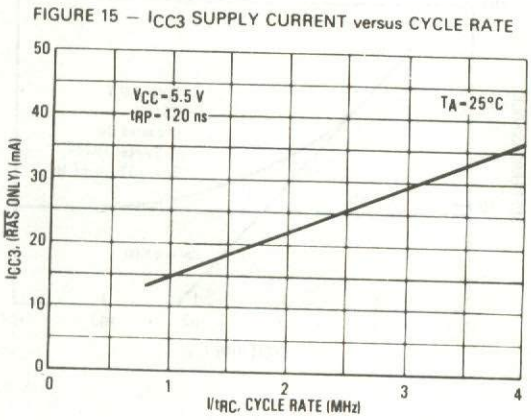


FIGURE 16 – ADDRESS INPUT LEVEL versus SUPPLY VOLTAGE

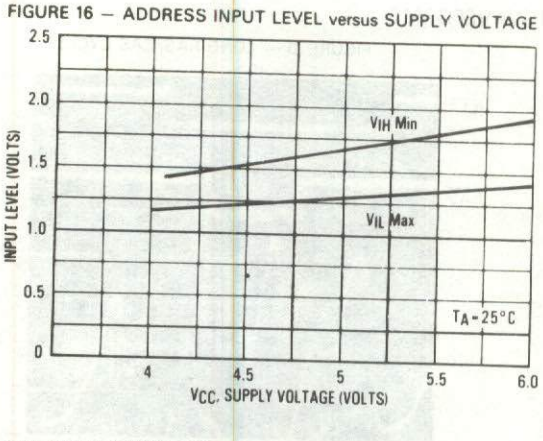
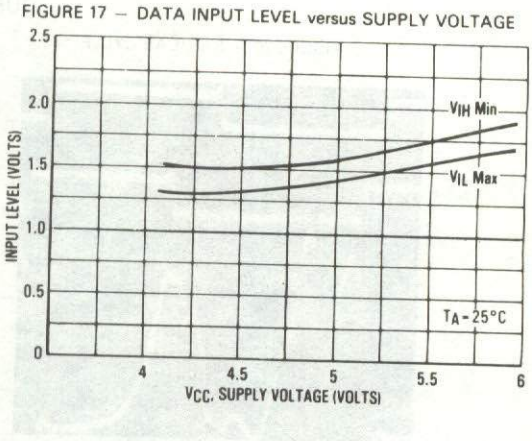


FIGURE 17 – DATA INPUT LEVEL versus SUPPLY VOLTAGE



SOFT ERROR TESTING

The storage cell depletion regions as well as the sense amplifier and its associated bit lines are susceptible to charge collection of electrons from an alpha "hit." However, the susceptibility of these vulnerable regions varies. Depleted storage cells are vulnerable at all times, whereas the sense amplifiers and associated bit lines are susceptible only during the small portion of the memory cycle just prior to sensing. Hence, an increase in the frequency of dynamic RAM access will cause a corresponding increase in the soft error rate.

To take this memory access dependency into account, the total soft error rate profile includes a cycle time component. The soft error rate due to bit line hits at the system's memory cycle rate is added to the soft error rate due to storage cell hits which are not frequency dependent. Figure 18 illustrates the impact that frequency of access has on the MCM6664A/MCM6665A overall soft error rate.

Under normal operating conditions, the die will be exposed to radiation levels of less than 0.01 alpha/cm^2/hr. Accelerated soft error testing data is generated from at least three high-intensity sources having an Alpha Flux Density range of 1×10^5 to 6×10^5 (alpha/cm^{2}hr) placed over uncoated die. Figure 19 shows the soft error rate for a given alpha flux density at a cycle rate of 100 kHz. The accelerated data of Figures 18 and 19 project that the soft error rate for package level radiation will be less than 0.1%/1000 hours.

SYSTEM LIFE OPERATING TEST CONDITIONS

1) Cycle time: 1 microsecond for read, write and refresh cycles
2) Refresh Rate: 1 millisecond
3) Voltage: 5.0 V
4) Temperature: 30° C ± 2° C (ambient temperature inside enclosure)
5) Elevation: Approximately 620 feet above mean sea level
6) Data Patterns: Write the entire memory space sequentially with all "1"s and then perform continuous sequential reads for 6 hours. Next, write the entire memory space with all "0"s sequentially and then perform continuous sequential reads for 6 hours. Next, go back to the all "1"s pattern and repeat the sequences all over again.

FIGURE 18 — ACCELERATED SOFT ERROR versus CYCLE TIME

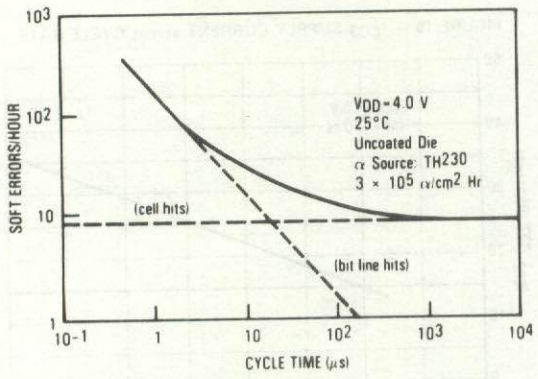
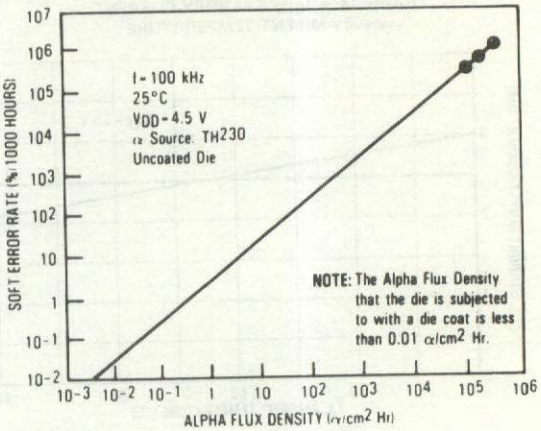


FIGURE 19 — SOFT ERROR RATE versus ALPHA FLUX DENSITY



CURRENT WAVEFORMS

FIGURE 20 — $\overline{RAS}/\overline{CAS}$ CYCLE

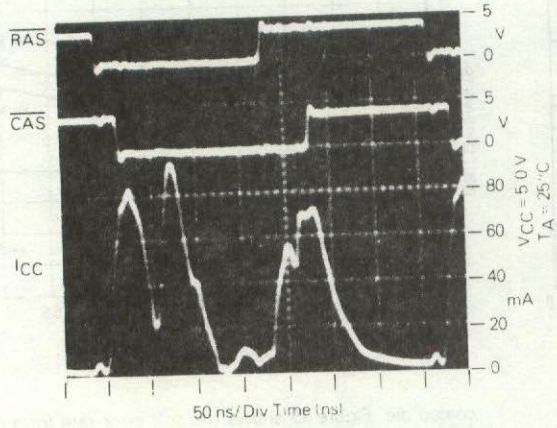


FIGURE 21 — LONG $\overline{RAS}/\overline{CAS}$ CYCLE

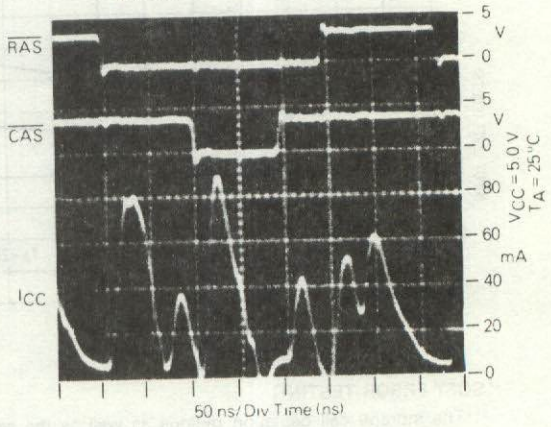


FIGURE 22 — $\overline{RAS}$ ONLY CYCLE

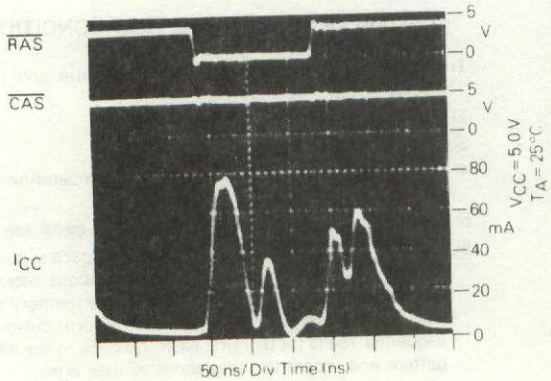
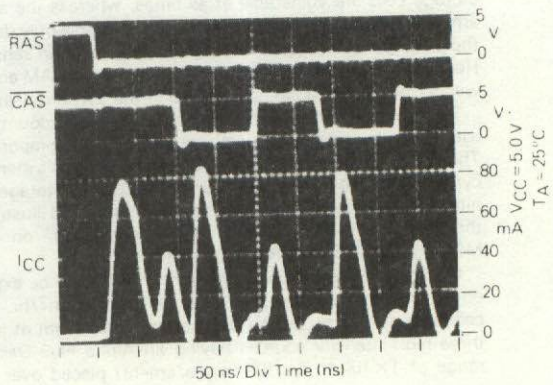


FIGURE 23 — PAGE MODE CYCLE



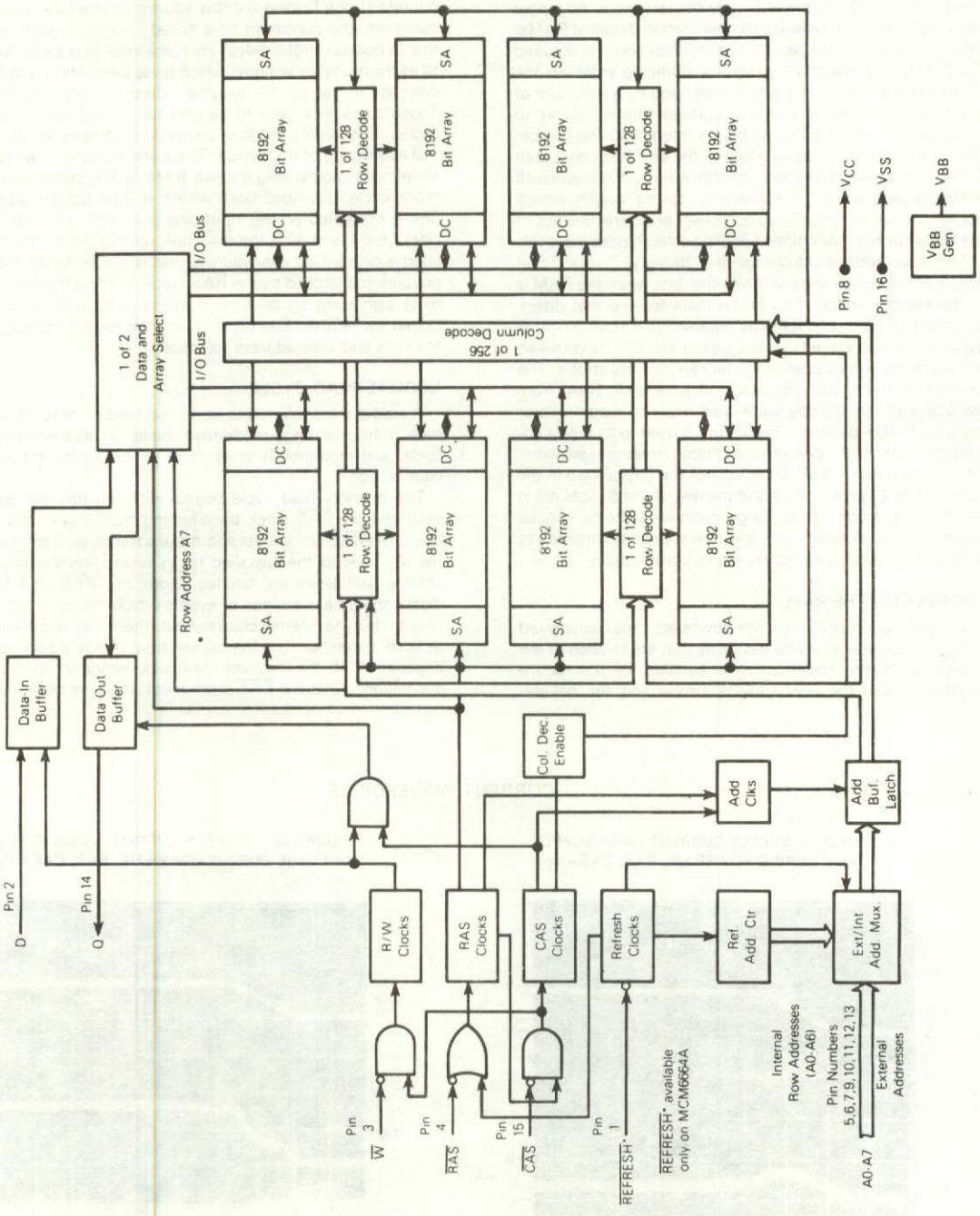


FIGURE 24 — FUNCTIONAL BLOCK DIAGRAM

MCM6665A

DEVICE INITIALIZATION

Since the 64K dynamic RAM is a single supply 5 V only device, the need for power supply sequencing is no longer required as was the case in older generation dynamic RAMs. On power-up an initial pause of 100 microseconds is required for the internal substrate generator pump to establish the correct bias voltage. This is to be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize the various dynamic nodes internal to the device. During an extended inactive state of the device (greater than 2 ms with device powered up) the wake up sequence (8 active cycles) will be necessary to assure proper device operation. See Figures 25, 26 for power on characteristics of the RAM for two conditions (clocks active, clocks inactive).

The row address strobe is the primary "clock" that activates the device and maintains the data when the RAM is in the standby mode. This is the main feature that distinguishes it as a dynamic RAM as opposed to a static RAM. A dynamic RAM is placed in a low power standby mode when the device receives a positive-going row address strobe. The variation in the power dissipation of a dynamic RAM from the active to the standby state is an order of magnitude or more for NMOS devices. This feature is used to its fullest advantage with high density mainframe memory systems, where only a very small percentage of the devices are in the active mode at any one time and the rest of the devices are in the standby mode. Thus, large memory systems can be assembled that dissipate very low power per bit compared to a system where all devices are active continuously.

ADDRESSING THE RAM

The eight address pins on the device are time multiplexed with two separate 8-bit address fields that are strobed at the beginning of the memory cycle by two clocks (active negative) called the row address strobe and the column address strobe. A total of sixteen address bits will decode one of the 65,536 cell locations in the device. The column address strobe follows the row address strobe by a specified minimum and maximum time called "t_{RCD}," which is the row to column strobe delay. This time interval is also referred to as the multiplex window which gives flexibility to a system designer to set up his external addresses into the RAM. These conditions have to be met for normal read or write cycles. This initial portion of the cycle accomplishes the normal addressing of the device. There are, however, two other variations in addressing the 64K RAM: one is called the page mode cycle (described later) where an 8-bit column address field is presented on the input pins and latched by the $\overline{CAS}$ clock, and the other is the $\overline{RAS}$ only refresh cycle (described later) where a 7-bit row address field is presented on the input pins and latched by the $\overline{RAS}$ clock. In the latter case, the most significant bit on Row Address A7 (pin 9) is not required for refresh. See bit address map for the topology of the cells and their address selection.

NORMAL READ CYCLE

A read cycle is referred to as normal read cycle to differentiate if from a page-mode-read cycle, a read-while-write cycle, and read-modify-write cycle which are covered in a later section.

The memory read cycle begins with the row addresses valid and the $\overline{RAS}$ clock transitioning from V_{IH} to the V_{IL} level. The $\overline{CAS}$ clock must also make a transition from V_{IH} to the V_{IL} level at the specified t_{RCD} timing limits when the column addresses are latched. Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. Also, these clocks are linked in such a manner that the access time of the device is independent of the address multiplex window. The only stipulation is that the $\overline{CAS}$ clock must be active before or at

CURRENT WAVEFORMS

FIGURE 25 — SUPPLY CURRENT versus SUPPLY VOLTAGE DURING POWER UP, $\overline{RAS}$, $\overline{CAS}$ = V_{CC}

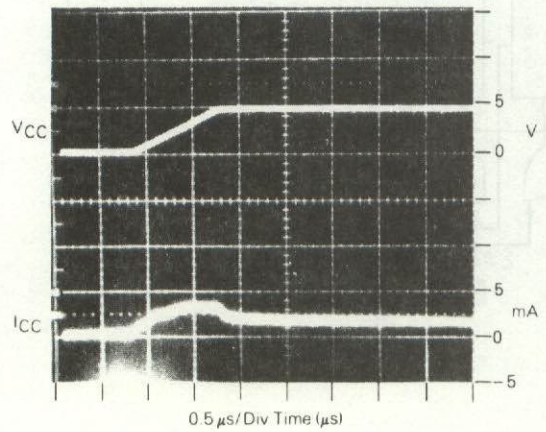
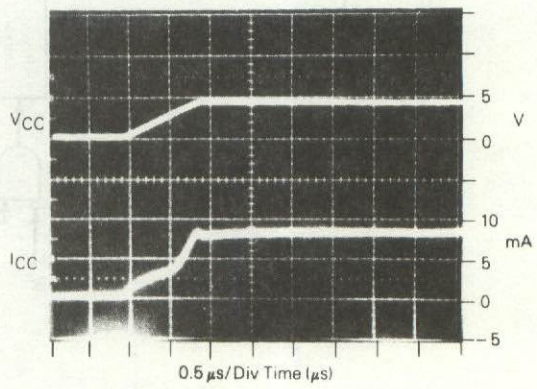


FIGURE 26 — SUPPLY CURRENT versus SUPPLY VOLTAGE DURING POWER UP, $\overline{RAS}$, $\overline{CAS}$ = V_{SS}



the t_{RCD} maximum specification for an access (data valid) from the $\overline{RAS}$ clock edge to be guaranteed (t_{RAC}). If the t_{RCD} maximum condition is not met, the access (t_{CAC}) from the $\overline{CAS}$ clock active transition will determine read access time. The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available, as noted in the functional block diagram, Figure 24. This gating feature on the $\overline{CAS}$ clock will allow the external $\overline{CAS}$ signal to become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the three-state mode when the $\overline{CAS}$ clock goes inactive. The $\overline{CAS}$ clock can remain active for a maximum of 10 ns (t_{CRP}) into the next cycle. To perform a read cycle, the write ($\overline{W}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

WRITE CYCLE

A write cycle is similar to a read cycle except that the Write ($\overline{W}$) clock must go active (V_{IL} level) at or before the $\overline{CAS}$ clock goes active at a minimum t_{WCS} time. If the above condition is met, then the cycle in progress is referred to as a early write cycle. In an early write cycle, the write clock and the data in is referenced to the active transition of the $\overline{CAS}$ clock edge. There are two important parameters with respect to the write cycle: the column strobe to write lead time (t_{CWL}) and the row strobe to write lead time (t_{RWL}). These define the minimum time that $\overline{RAS}$ and $\overline{CAS}$ clocks need to be active after the write operation has started ($\overline{W}$ clock at V_{IL} level).

It is also possible to perform a late write cycle. For this cycle the write clock is activated after the $\overline{CAS}$ goes low which is beyond t_{WCS} minimum time. Thus the parameters t_{CWL} and t_{RWL} must be satisifed before terminating this cycle. The difference between an early write cycle and a late write cycle is that in a late write cycle the write ($\overline{W}$) clock can occur much later in time with respect to the active transition of the $\overline{CAS}$ clock. This time could be as long as 10 microseconds $- [t_{RWL} + t_{RP} + 2T_t]$.

At the start of a write cycle, the data out is in a three-state condition and remains inactive throughout the cycle. The data out remains three-state because the active transition of the write ($\overline{W}$) clock prevents the $\overline{CAS}$ clock from enabling the data-out buffers as noted in Functional Block Diagram. The three-state condition (high impedance) of the Data Out Pin during a write cycle can be effectively utilized in a system that has a common input/output bus. The only stipulation is that the system use only early write mode operations for all write cycles to avoid bus contention.

READ-MODIFY-WRITE AND READ-WHILE-WRITE CYLES

As the name implies, both a read and a write cycle is accomplished at a selected bit during a single access. The read-modify-write cycle is similar to the late write cycle discussed above.

For the read-modify-write cycle a normal read cycle is initiated with the write ($\overline{W}$) clock at the V_{IH} level until the read data occurs at the device access time (t_{RAC}). At this time the write ($\overline{W}$) clock is asserted. The data in is setup and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

Another variation of the read-modify-write cycle is the read-while-write cycle. For this cycle, the following parameters (t_{RWD}, t_{CWD}) play an important role. A read-while-write cycle starts as a normal read cycle with the write ($\overline{W}$) clock being asserted at minimum t_{RWD} or minimum t_{CWD} time, depending upon the application. This results in starting a write operation to the selected cell even before data out occurs. The minimum specification on t_{RWD} and t_{CWD} assures that data out does occur. In this case, the data in is set up with respect to write ($\overline{W}$) clock active edge.

PAGE-MODE CYCLES

Page mode operation allows faster successive data operations at the 256 column locations. Page access (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access (t_{RAC}) on the Motorola 64K dynamic RAM. Page mode operation consists of holding the $\overline{RAS}$ clock active while cycling the $\overline{CAS}$ clock to access the column locations determined by the 8-bit column address field. There are two controlling factors that limit the access to all 256 column locations in one $\overline{RAS}$ clock active operation. These are the refresh interval of the device (2 ms/128 = 15.6 microseconds) and the maximum active time specification for the $\overline{RAS}$ clock (10 microseconds). Since 10 microseconds is the smaller value, the maximum specification of the $\overline{RAS}$ clock on time is the limiting factor of the number of sequential page accesses possible. Ten microseconds will provide approximately (10 microseconds/page mode cycle time) 50 successive page accesses for every row address selected before the $\overline{RAS}$ clock is reset.

The page cycle is always initiated with a row address being provided and latched by the $\overline{RAS}$ clock, followed by the column address and $\overline{CAS}$ clock. From the timing illustrated, the initial cycle is a normal read or write cycle, that has been previously described, followed by the shorter $\overline{CAS}$ cycles (t_{PC}). The $\overline{CAS}$ cycle time (t_{PC}) consists of the $\overline{CAS}$ clock active time (t_{CAS}), and $\overline{CAS}$ clock precharge time (t_{CP}) and two transitions. In addition to read and write cycles, a read-modify-write cycle can also be performed in a page mode operation. For a read-modify-write or read-while-write type cycle, the conditions normal to that mode of operation will apply in the page mode also. The page mode cycles illustrated show a series of sequential reads separated by a series of sequential writes. This is just one mode of operation. In practice, any combination of read, write and read-modify-write cycles can be performed to suit a particular application.

REFRESH CYCLES

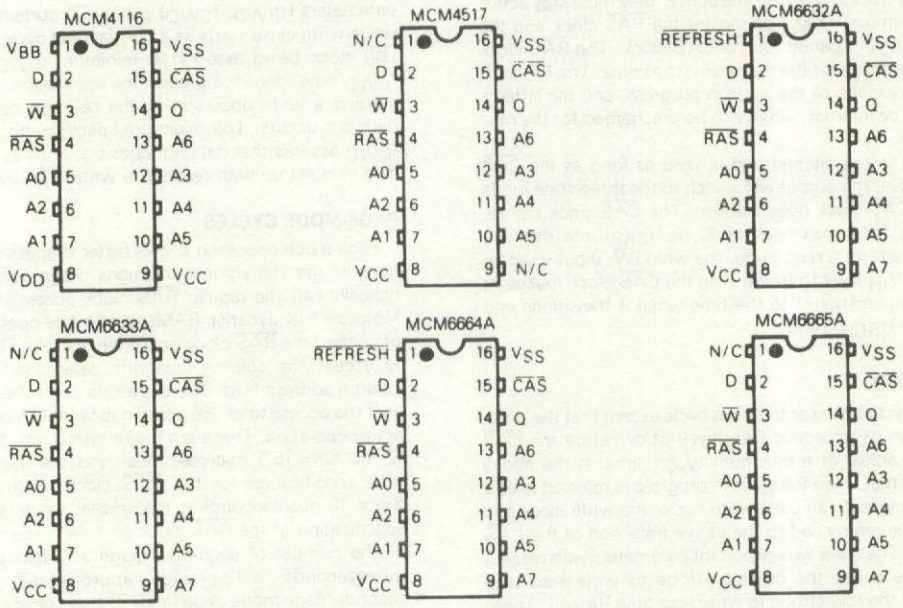
The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to

MCM6665A

degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 2 ms. This is accomplished by sequentially cycling through the 128 row address locations every 2 ms, or at least one row every 15.6 microseconds. A normal read or write operation to the RAM will serve to refresh all the bits (256) associated with that particular row decoded.

$\overline{RAS}$ Only Refresh – When the memory component is in standby the $\overline{RAS}$ only refresh scheme is employed. This refresh method performs a $\overline{RAS}$ only cycle on all 128 row addresses every 2 ms. The row addresses are latched in with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CAS}$ clock is not required and should be inactive or at a V_{IH} level to conserve power.

PIN ASSIGNMENT COMPARISON

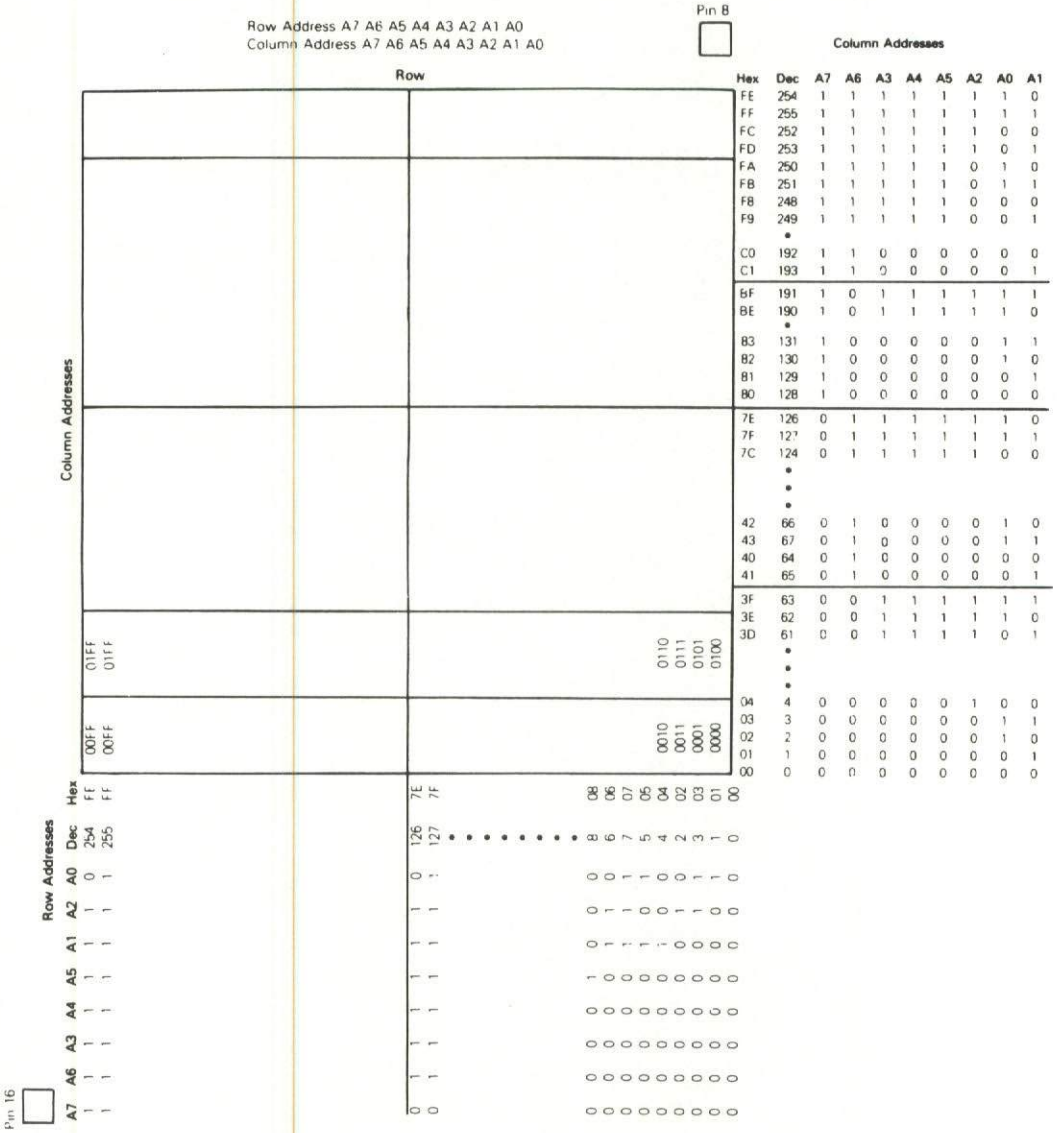


PIN VARIATIONS

PIN NUMBER	MCM4116	MCM4517	MCM6632A	MCM6663A	MCM6664A	MCM6665A
1	V_{BB} (−5 V)	N/C	REFRESH	N/C	REFRESH	N/C
8	V_{DD} (+12 V)	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
9	V_{CC} (+5 V)	N/C	A7	A7	A7	A7

MCM6665A

MCM6665A BIT ADDRESS MAP



Hex	Dec	A7	A6	A3	A4	A5	A2	A0	A1
FE	254	1	1	1	1	1	1	1	0
FF	255	1	1	1	1	1	1	1	1
FC	252	1	1	1	1	1	1	0	0
FD	253	1	1	1	1	1	1	0	1
FA	250	1	1	1	1	1	0	1	0
FB	251	1	1	1	1	1	0	1	1
F8	248	1	1	1	1	1	0	0	0
F9	249	1	1	1	1	1	0	0	1
	•								
C0	192	1	1	0	0	0	0	0	0
C1	193	1	1	0	0	0	0	0	1
BF	191	1	0	1	1	1	1	1	1
BE	190	1	0	1	1	1	1	1	0
	•								
83	131	1	0	0	0	0	0	1	1
82	130	1	0	0	0	0	0	1	0
81	129	1	0	0	0	0	0	0	1
80	128	1	0	0	0	0	0	0	0
7E	126	0	1	1	1	1	1	1	0
7F	127	0	1	1	1	1	1	1	1
7C	124	0	1	1	1	1	1	0	0
	•								
	•								
	•								
42	66	0	1	0	0	0	0	1	0
43	67	0	1	0	0	0	0	1	1
40	64	0	1	0	0	0	0	0	0
41	65	0	1	0	0	0	0	0	1
3F	63	0	0	1	1	1	1	1	1
3E	62	0	0	1	1	1	1	1	0
3D	61	0	0	1	1	1	1	0	1
	•								
	•								
	•								
04	4	0	0	0	0	0	1	0	0
03	3	0	0	0	0	0	0	1	1
02	2	0	0	0	0	0	0	1	0
01	1	0	0	0	0	0	0	0	1
00	0	0	0	0	0	0	0	0	0

Data Stored = $D_{in} \oplus A_{0X} \oplus A_{1Y}$

Column Address A1	Row Address A0	Data Stored
0	0	True
0	1	Inverted
1	0	Inverted
1	1	True

SERVICE MODULE

Floppy Disk Controller Card

Z-100 PC Series Computers

585-63-01

860-45

ZENITH data systems

The purpose of this page is to make sure that all service bulletins are entered in this manual. When a service bulletin is received, annotate the manual and list the information in the record below.

Record of Service Bulletins

SERVICE BULLETIN NUMBER	DATE OF ISSUE	CHANGED PAGE(S)	PURPOSE OF SERVICE BULLETIN	INITIALS

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St. Joseph, Michigan 49085

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Schematic Fold-in

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Abbreviations

ACE	Asynchronous Communication Element
AEN	Address Enable
CD	Carrier Detect
CPU	Central Processing Unit
CTS	Clear to Send
DEMUX	Demultiplexer
DIP	Dual Inline Pack
DMA	Direct Memory Access
DSR	Data Set Ready
DTR	Data Terminal Ready
FDC	Floppy Disk Controller
INT	Interrupt
I/O	Input/Output
MHz	Megahertz
MFM	Modified Frequency Modulation
ms	millisecond
MUX	Multiplexer
ns	nanosecond
PAL	Programmable Array Logic
PLL	Phase-Locked Loop
RD	Read
RI	Ring Indicator
RTS	Request to Send
TP	Test Point
TTL	Transistor-Transistor Logic
VCO	Voltage-Controlled Oscillator
WR	Write

Chapter 1

Introduction

The floppy disk controller card is divided into two sections: the floppy disk controller for the 5.25-inch floppy disk drives, and a pair of serial input/output (I/O) channels for communication. Two schematics are supplied with this service module, one for each section.

Tools and Test Equipment

- Disk-Based Diagnostics Manual, Model CB-5063-13, Part Number 595-3176
- Loop back cables for Input/Output Port Diagnostics, HE 134-1433
- VOM
- Frequency Counter
- Oscilloscope (100 MHz minimum)

Specifications

Serial Input/Output

Number of DTE Channels:	2
Controllers:	Western Digital 8250 ACE (2 — one per channel)
Baud Rates:	50 to 19,200 baud
Communication:	Asynchronous
Word Length:	5, 6, 7, or 8 bits per word
Parity:	Odd, even, or none
Start Bits:	1
Stop Bits:	1 or 2
Control Functions:	CTS, RTS, DSR, DTR, RI, and/or CD
CPU Port Addressing:	COM1 (03F8H-03FFH) COM2 (02D0-02DF)
Full or Half Duplex:	Software programmable

Floppy Disk Controller

Disks Supported:	5.25-inch double-sided double-density
Number:	Up to 4
Controller:	NEC μPD765
CPU Port Addressing:	03F0H-03F7H
Heads:	2
Format:	40 tracks, 8 or 9 sectors/track, 512 bytes/sector, double-density, modified frequency modulation (MFM) encoding
Motor Start Time:	500 ms
Head Load Time:	35 ms
Head Settle Time:	25 ms
Track Stepping:	6 ms track-to-track

Chapter 2

Installation and Configuration

For installation instructions, see the Z-100 PC Series *Base Units Service Modules*.

Configuration

The floppy disk controller card has two jumper blocks, J501 and J502 (see Figure 2.1). Normally, only IR3 of J502 is jumpered; the rest do not have jumpers.

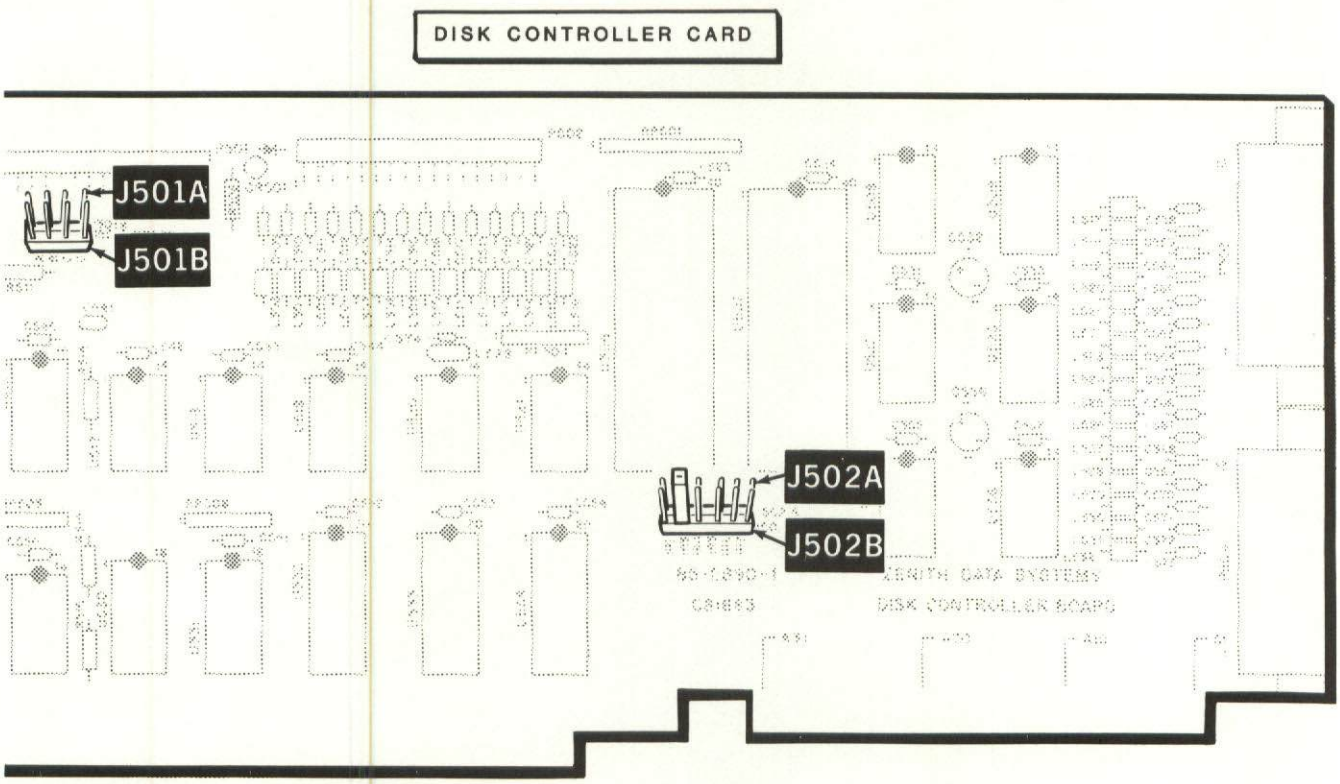


Figure 2.1. Card Jumpers

Chapter 3
Operation

The operation of both the floppy disk controller and serial input/output channels is covered in the "Manufacturer's Data Sheets," Chapter 8. Refer to the disk-based diagnostics (CB-5063-13) for specific tests that can be performed on this card to check its operation.

Serial Interfacing

Table 3.1 and Figures 3.1 and 3.2 provide the pinout and voltage levels for the two RS-232 connectors.

Table 3.1. RS-232 Connector Pinout

PIN	SIGNAL
1	Chassis Ground
2	Transmit Data
3	Receive Data
4	Request to Send (RTS)
5	Clear to Send (CTS)
6	Data Set Ready (DSR)
7	Signal Ground
8	Carrier Detect (CD)
20	Data Terminal Ready (DTR)
22	Ring Indicate (RI)

All other pins are NC (not connected).

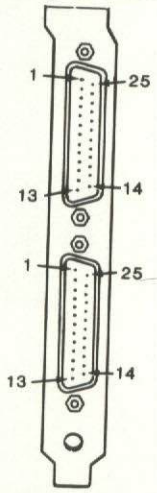


Figure 3.1. RS-232 Connector Pinout

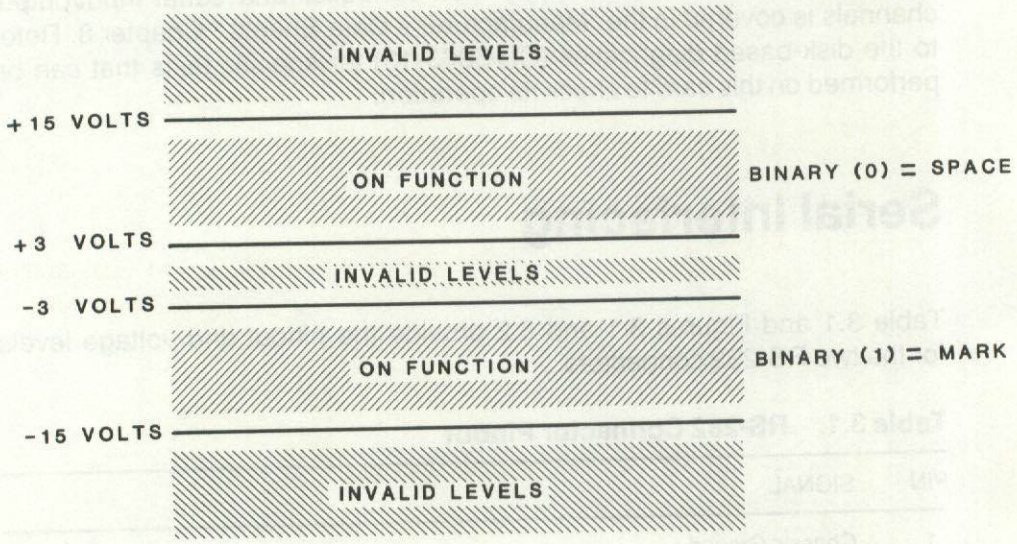


Figure 3.2. Serial Interface Voltage Levels

Chapter 4

Theory of Operation

The floppy disk controller card actually has two sections: the controller itself and a pair of serial input/output channels.

Serial Input/Output Interface

The serial input/output section of the board is limited to ten (10) active elements. Refer to the block diagram in Figure 4.1 for the following discussion.

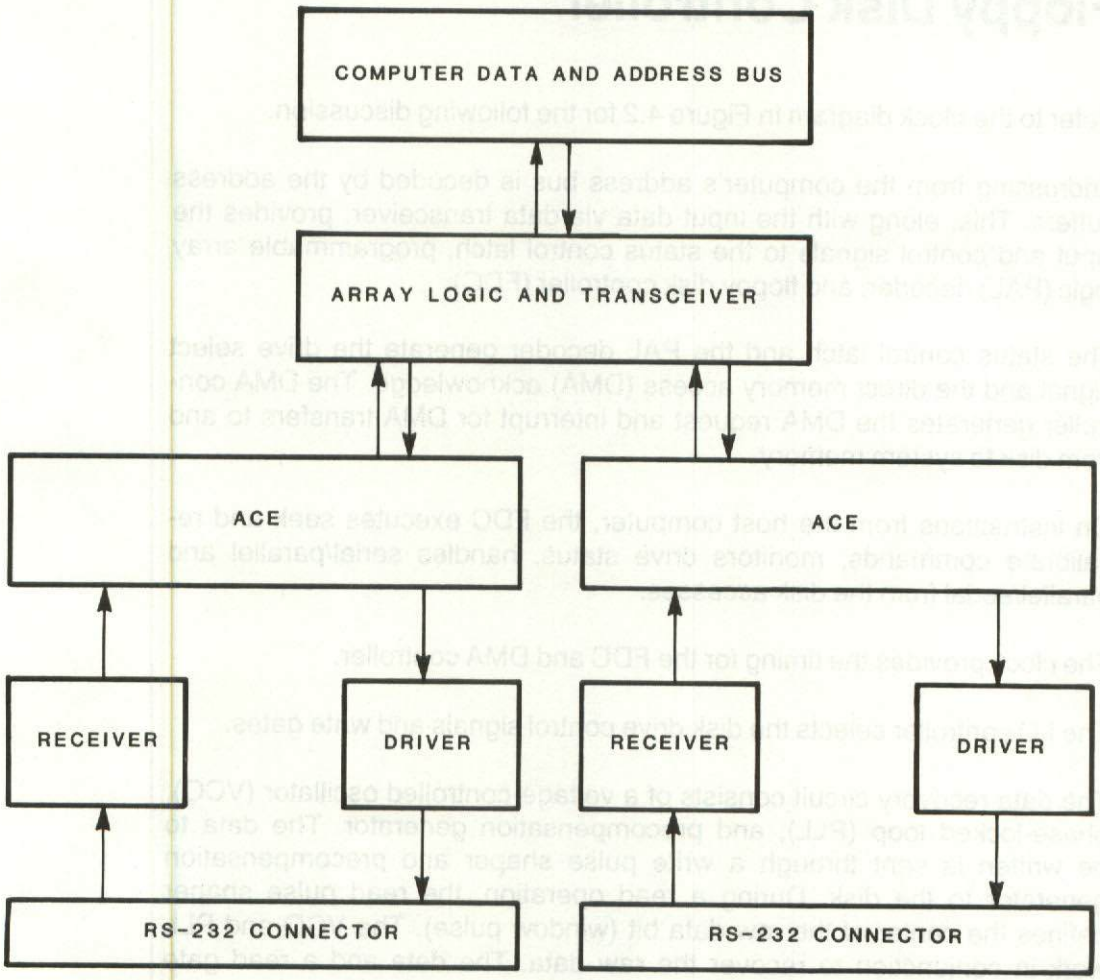


Figure 4.1. Block Diagram — Serial Input/Output Channels

Addressing from the computer's data and address bus is decoded by the array logic. The bidirectional transceiver provides the bus interface to each of two asynchronous communication elements (ACEs) — one for each channel. The ACEs convert a serial input into a parallel output, and vice versa, through internal receiver, transmitter, and control sections. In addition, the ACE provides management of the serial control signals (word length, start and stop bits, and parity) and speed. Refer to the "Manufacturer's Data Sheets," Chapter 8, for more information. The interfaces to the RS-232 connectors are provided by separate receivers and drivers.

Floppy Disk Controller

Refer to the block diagram in Figure 4.2 for the following discussion.

Addressing from the computer's address bus is decoded by the address buffers. This, along with the input data via data transceiver, provides the input and control signals to the status control latch, programmable array logic (PAL) decoder, and floppy disk controller (FDC).

The status control latch and the PAL decoder generate the drive select signal and the direct memory access (DMA) acknowledge. The DMA controller generates the DMA request and interrupt for DMA transfers to and from disk to system memory.

On instructions from the host computer, the FDC executes seek and recalibrate commands, monitors drive status, handles serial/parallel and parallel/serial from the disk accesses.

The clock provides the timing for the FDC and DMA controller.

The I/O controller selects the disk drive control signals and write gates.

The data recovery circuit consists of a voltage-controlled oscillator (VCO), phase-locked loop (PLL), and precompensation generator. The data to be written is sent through a write pulse shaper and precompensation generator to the disk. During a read operation, the read pulse shaper defines the center of the raw data bit (window pulse). The VCO and PLL work in conjunction to recover the raw data. The data and a read gate are then sent to the FDC.

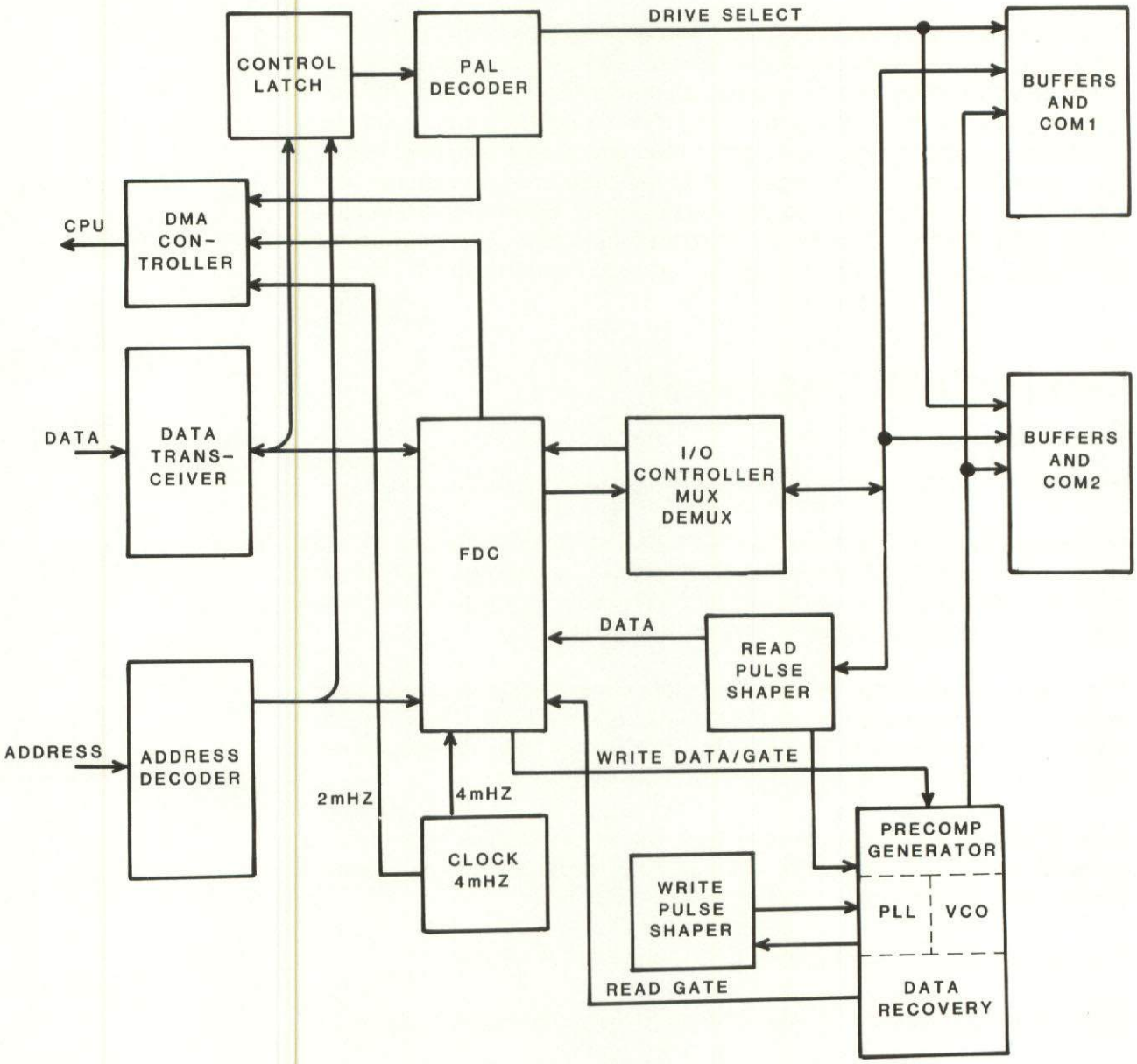


Figure 4.2. Block Diagram — Floppy Disk Controller

Chapter 5

Detailed Circuit Descriptions

The following pages describe the operation of the circuits on the floppy disk controller and serial input/output card for the Z-100 PC Series Computers.

Serial Input/Output

Refer to sheet one (1) of the schematic for the following description.

Card addressing from the bus is decoded by the array logic in U532 (when /AEN becomes active). COM1 (U507, U509, U523, and P503), or COM2 (U506, U535, U536, and P504) is selected by generating CSUA1* (addresses 03F8H-03FFH) or CSUA2* (addresses 02D0-02DF), respectively, depending upon the status of address bit A8. Refer to Table 5.1 and Figure 5.1 for the PAL equation and pinout. The direction of the signal is determined by the state of IORD*. (U522 controls both channels.)

Table 5.1. U532 Array Logic Equations

OUTPUT		INPUT
/CSUA1	=	A3*A4*A5*A6*A7*A8*A9*AEN
/CSUA2	=	A3*A4*A5*A6*A7*/A8*A9*AEN
/DELAYO	=	/IORD
/DIRC	=	A3*A4*A5*A6*A7*A9*AEN*IORD + A3*A4*A5*A6*A7*A9*DELAYI*AEN
/GATE	=	A3*A4*A5*A6*A7*A9*AEN

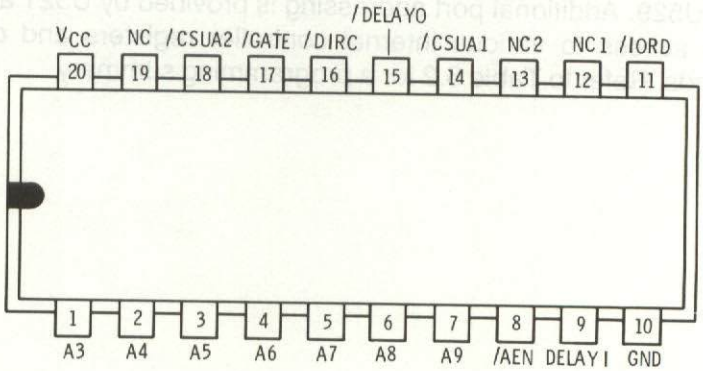


Figure 5.1. U532 Array Logic Pinout

Data flow is through the transceiver (U534); direction is determined by DIRC* and GATE* from the array logic (U532). In the ACEs, direction (function — receive or transmit) is determined by IORD* and IOWR* from the computer's bus.

RESET (from the computer's bus) clears the array logic and the internal buffers of the two ACEs (except the receive buffer, transmitter holding, and divisor latches) through pin 35 (MR — Master Reset).

U520 supplies the baud clock frequency base of 1.8432 MHz.

The output is driven by U523 (COM1) and U536 (COM2). The interfacing for the input is handled by U509 and U522, pin 4 (COM1), and U535 and U522, pin 1 (COM2).

U508 is a tri-state buffer that is used to detect and initiate an interrupt cycle through the jumpers at J502.

The L-C network (L599 and C574) and the passive L-C filters at the card's connectors are used to reduce RF emission levels.

Floppy Disk Controller

Refer to sheet two (2) of the schematic for the following discussion.

The floppy disk controller is hardwired for a base address of 03F0H by U519 and U529. Additional port addressing is provided by U521 and U511 to provide access to various internal controller registers and decoding of commands. Refer to Table 5.2 for a programming summary.

Table 5.2. Programming Summary

REGISTER	INPUT/OUTPUT PORT ADDRESS
Floppy Disk Controller Data Register	03F5H
Floppy Disk Controller Status Register	03F4H
Digital Output Register	03F1H

Bit	Description
0 & 1	Drive Select: 00 = drive A; 01 = B, 10 = C, and 11 = D
2	Not Floppy Disk Controller Reset
3	Enable INT and DMA Requests
4	Drive A Motor Enable
5	Drive B Motor Enable
6	Drive C Motor Enable
7	Drive D Motor Enable

Note: All bits are cleared with channel reset.

FDC Constants:

N	02H
SC	08H
HUT	0FH
SRT	0CH
GPL FORMAT	05H
GPL RD/WR	2AH
HLT	01H

Drive Constants:

HD Load	35ms[1]
HD Settle	25ms[2]
Motor Start	500ms[3]
Track-Track	6ms

Comments:

[1] The head will load with drive select; wait the HD load time before attempting read/write operations.

[2] Following disk access, wait the HD settle time before attempting read/write operations.

[3] The motor must be on for a drive to be selected.

Read (RD) and Write (WR) determination originate with the central processing unit (CPU) (IO/RD* and IO/WR*) and enter the card through U521. The output of U521 is sent to the floppy disk controller (U510) and controls the bidirectional transceiver (U533).

Data input and output is buffered by the octal transceiver (U533) onto an on-board data bus, and sent to the floppy disk controller (U510) and the octal flip-flop status control latch (U527). The array logic device (U528) maps which motor and drive is selected (DS1*-DS4*) from the data fed to it by the status control latch and CPU control signals. Refer to Table 5.3 and Figure 5.2.

Table 5.3. U528 Array Logic Equations

OUTPUT	INPUT
/DS1	/Q0*/Q1*/Q4
/DS2	Q0*/Q1*Q5
/DS3	/Q0*Q1*Q6
/DS4	Q0*Q1*Q7
MOTOR	/Q4*/Q5*/Q6*/Q7
/RDWR	SEL + DACK2*DMAGATE
TCO	/DACK2 + /TC
/DACK	DMAGATE*DACK2

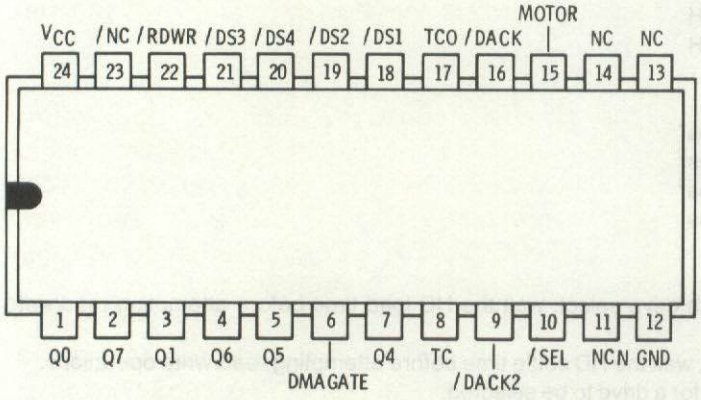


Figure 5.2. U528 Array Logic Pinout

DMA handling by the DMA processor on the CPU card is determined by the DRQ2 signal that originates with the floppy disk controller (DRQ = 1), delayed by U503 and driven by U530. Interrupt (INT) request IR6 also originates in the floppy disk controller and is driven by U530 onto the computer's backplane bus.

Timing for the floppy disk controller (U510) is determined by a 4.00 MHz clock (U501). U502 provides write timing to the floppy disk controller and produces the 2 MHz signal for the DMA delay flip-flop (U503).

Disk timing (soft-sectoring requires recognition of the beginning of each track) is provided by INDEX A* (COM1) or INDEX B* (COM2) from the disk selected by the MUX (U531) through an inverter (U512) to the floppy disk controller input at pin 17 (IDX).

The FDC outputs various floppy disk control signals through a tri-state buffer (U524) and MUX (U531) to the two drive connectors. See the μPD765 Data Sheet located in Chapter 8 for more information on the signals used and generated by the floppy disk controller.

One half of the multivibrator (U514A) is used to keep the drive motors enabled for 2 to 3 seconds after the last access. The timing of the multivibrator is determined by the R-C network (R509 and C529). Feedback into the circuitry is provided through the tri-state buffer (U508) back into D0. The board also supplies a means to feed back a ready signal from the drives through J501 and U508 to D1 (not currently used in Z-150/160 applications).

VCO U504 is biased by the +5 VDC regulator (U505); the input (of the VCO) is adjusted to 1.4 V by the BIAS R505 control. Measurement of this voltage can be taken at test point 2 (TP2). The output of the VCO (U504) is adjusted to 2 MHz (measured at TP1) with R501 and feeds the phase-locked loop (PLL) IC (U525). The VCO is used in conjunction with U525 and U513 for precompensation and data separation.

U514B (provides 40 ns pulses) and U516B (provides 250 ns pulses) shape the read data from the disk for use by the rest of the card. Timing is controlled by the two R-C networks (R512 and C549 and R514 and C541, respectively). U516A (provides 1 ms pulses) modifies the width of the write data sent to the disk. Timing is provided by an R-C network (R513 and C539).

Open collector output signal drive is provided by buffers U515, U517, and U518.

Chapter 6

Troubleshooting and Adjustments

Observe the normal precautions for electrostatic sensitive devices while handling this board or any of its components.

Adjustment Sequence and Tests

Serial Input/Output

The input/output portion of this card has no adjustments. U520 is the baud rate generator. Check to make sure that its output frequency is 1.8432 MHz.

Floppy Disk Controller

The following adjustment sequence is for the operation of the floppy disk controller only.

1. The following cards must be installed in the computer:
   - CPU card
   - Memory card; one or two — make sure the CPU switches are properly set
   - Video card
   - Floppy disk controller card

2. Turn on the computer. Check for +5 VDC and +12 VDC input voltage to the disk drives. Make sure the CPU, ROM, RAM, INT, DSK, and RDY LEDs on the CPU card go out. If all but the DSK or RDY LED go out, proceed to the troubleshooting chart in this service module. If one of the other LEDs remain on, proceed to the troubleshooting chart in either the *System CPU Card Service Module* or the *Memory Cards Service Module*.

NOTE: The DSK LED will be on if the disk is not booted.

NOTE: The RDY LED will not go out if the VCO is off frequency.

3. Refer to Figure 6.1. Set your voltmeter to the +5 VDC range and measure the voltage from ground (on the card) to TP2. It should read +1.4 volts. If it doesn't, adjust the BIAS control (R505) to read *exactly* 1.4 volts.

4. Measure the frequency at TP1 with an oscilloscope or frequency counter. It should read *exactly* 2 MHz. If it does not, adjust the FREQ control (R501) to read 2MHz. **NOTE:** This signal should be a clean square wave.

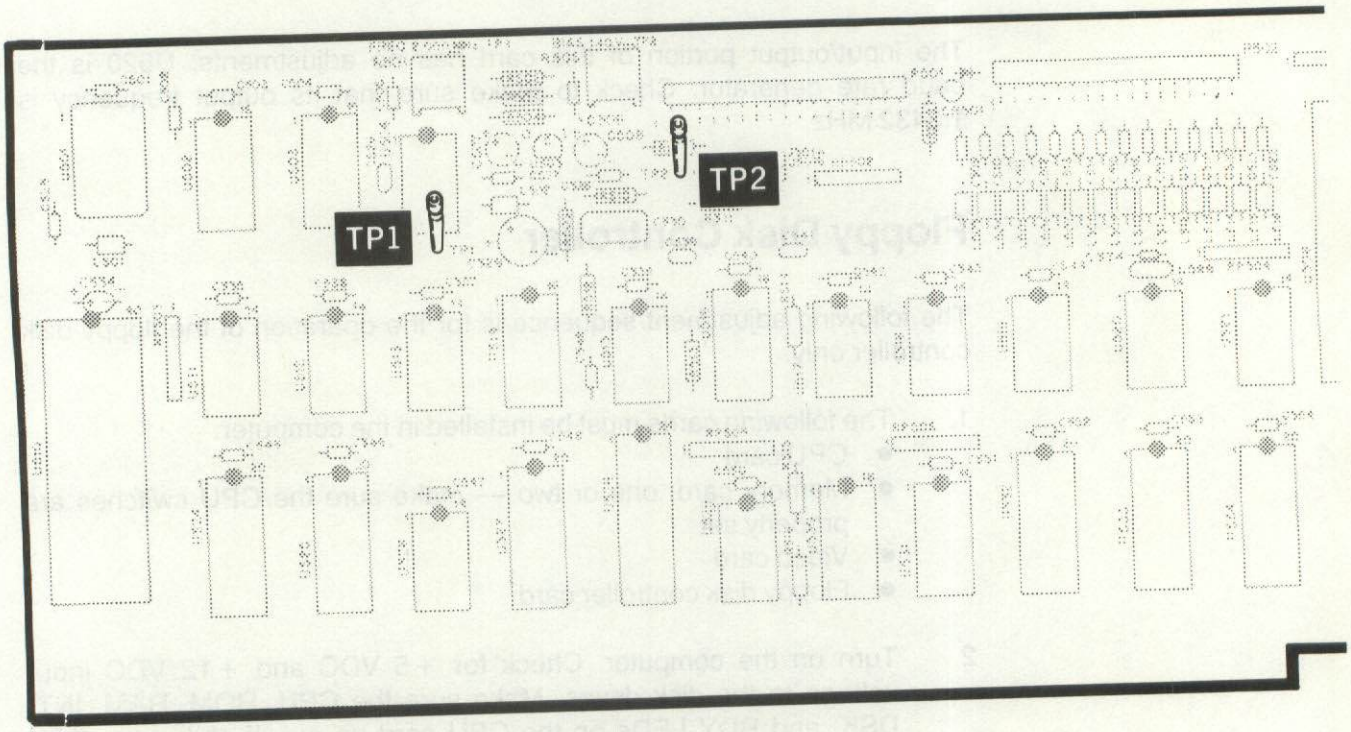


Figure 6.1. Card Test Points

Troubleshooting

General

Dirty contacts can cause intermittent problems. If you suspect dirty contacts, carefully clean all card edge contacts with a Gold Wipe.

Serial Input/Output

Power-up diagnostics do not check serial input/output. Therefore, if you are experiencing trouble with the output of one or both of the serial ports, you will need to check several things before assuming component or card failure. Most suspected problems in serial input/output situations are not hardware related, but originate with either the software or incorrect protocol for serial communications.

If you have the disk-based diagnostics (a purchase option), refer to the *Disk-Based Diagnostics Manual*, Chapter 4, "Input/Output Port Diagnostics," and run the input/output portion of the diagnostic programs. You will need to purchase two cables to complete these tests (part numbers 134-1433 and 438-64). If the diagnostics indicate no problem, use the following procedures in the order indicated.

1. Check for the correct serial cable. The two ports are DTE output devices and you cannot use the HCA-10, -11, or -12 cables as indicated in ZDS literature with this computer. You must use "null modem" cables, which are supplied under the HCA-50, -51, and -52 catalog numbers.

2. If you are sure the cable is correct, run the CONFIGUR utility (supplied with MS™-DOS) and reconfigure the output port as needed for the protocol required by the serial device with which you are attempting to communicate.

™MS is a trademark of Microsoft Corporation.

NOTE: MS-DOS normally routes the printer output through the *parallel* port. To use a *serial* printer, the customer **must** run CONFIGUR before the printer will operate correctly.

3. If you are still experiencing problems with a serial device, try it with another computer that is known to work. Try both the hardware and customer's software. This should establish whether or not the fault lies with the device, computer, or software.

4. If you have established that the problem appears to be hardware-oriented and in the customer's computer, try the other channel.

NOTE: Remember to run CONFIGUR to route your signals through the correct connector.

It is highly unlikely that both ports will give you identical symptoms; for the most part, the circuitry uses different components for each port.

5. If none of the preceding checks have resulted in any positive identification of the problem, replace the floppy disk controller serial input/output card and rerun your checks. This should isolate the problem to the card. If the card is at fault, use Table 6.1 for checking the individual components.

Table 6.1. Serial Input/Output Component Failures

SYMPTOM	SUSPECTED PARTS	THINGS TO CHECK
No output (both channels)	U532	Using Table 5.1 and Figure 5.1, check the input and output signals from this array logic.
	U520, L599, C574	Check for a base frequency of 1.8432 MHz.
	Power distribution	Check for +5 VDC on the Vcc input of any IC.
Data fault (both channels)	U534	Check for proper gating of signals through this IC. Pin 1 determines direction, pin 19 enables.
	U532	Using Table 5.1 and Figure 5.1, check the input and output signals from this array logic, particularly DIRCIO* and GATE*.
	U520, L599, C574	Check for a base frequency of 1.8432 MHz.
No output COM1	U523, U509, U522	Check the signal flow through the drivers and receivers.
	U507	Check the output signals from the ACE (refer to the data sheets for more information).
No output COM2	U535, U536, U522	Check the signal flow through the drivers and receivers.
	U506	Check the output signals from the ACE (refer to the data sheets for more information).
Wrong baud rate		
(COM1 & COM2)	U520, L599, C574	Check for a base frequency of 1.8432 MHz.
(COM1)	U507	Replace ACE.
(COM2)	U506	Replace ACE.
Active interrupt (COM1)	This may be a normal condition created by software. If checking another computer using the same software results in different symptoms or resolves the problem, then replace U508.	
Active interrupt (COM2)	This condition can be obtained only when J502 is jumpered. Make sure the customer desires this configuration. If this is desired, configure another computer with the appropriate jumper and try the same software on it. If this resolves the problem, then replace U508.	

Floppy Disk Controller

Floppy disk systems can exhibit a number of symptoms that can be traced to poor or bad disks, dirty or misaligned disk drive heads, or improper user operation. As a result of any of these problems, several different error messages can be generated by either the computer firmware (ROM) or operating system software. You should be familiar with normal disk operation in computers before attempting to service this section of the floppy disk controller card.

The following quick checks should isolate the problem to the card, disk drive, or other parts of the computer system.

1. On normal powerup, check the CPU diagnostic LEDs for proper sequencing.

   - With autoboot switched off (see CPU card switch settings), the DSK light on the CPU card should be the last light to go out (except for the RDY light, which will remain lit until a disk has been successfully booted).

   - With autoboot switched on (floppy disk boot), the DSK light will remain on until a disk is inserted. Otherwise, an error message will be generated, which reads:

     ```
     +++ DISK ERROR: DRIVE NOT READY! +++
     ```

     This is a normal error message and indicates that a bootable disk has not been placed in the disk drive. Timing of the timeout is controlled by the ROMs on the CPU card. Therefore, if you get this error message immediately after resetting the computer (press the **CTRL, ALT,** and **DEL** keys at the same time), you should check the ROM on the CPU card.

     Other conditions that can cause this error message include a disk improperly placed in the drive and a drive door (latch) which is not closed.

2. On normal powerup, the message:

```
+++ DISK ERROR: Seek failure! +++
```

can result from the disk drives not being plugged into the controller card or not receiving the correct power supply voltages. After having the computer off for at least five seconds, turn it back on and watch the drive access indicators. If they momentarily come on, the drive is probably receiving the correct power supply voltages and signals from the floppy disk controller. Make the next check.

3. On normal powerup, the messages:

```
+++ DISK ERROR: Invalid address mark detected! +++
+++ DISK ERROR: Sector not found! +++
+++ DISK ERROR: Seek failure! +++
+++ DISK ERROR: CRC error! +++
```

or no error message at all (but the system is attempting to boot a disk) can indicate a bad or unformatted disk, wrong format (CP/M instead of MS-DOS), or wrong operating system (Z-DOS instead of MS-DOS). The "sector not found" error message also may indicate a data disk (non-bootable disk).

In any of these cases, reset the computer (you probably will have to turn it off, wait five seconds, and then turn it back on), and attempt to boot the system with a *known* good disk. Do not use distribution disks for this purpose; use a backup.

4. The message:

```
System disk
```

indicates that the disk has the correct format, but not an operating system.

5. If you are servicing the computer with the drives out, make sure that all parts are free to move normally. Do not lay the drive flat on top of the power supply. The magnetic flux fields can interfere with normal disk movement and cause the "seek failure" error message, even with a good disk.

6. If you are using a known "good" disk and the drive does not "garbage" it (that is, erase or rewrite the information on it), then check the VCO bias voltage and output. (See the Adjustments section of this chapter.)

7. If the DSK LED on the CPU card does not go out and the disk access LED on the front(s) of the drive(s) glows, check to make sure that the drive cable is plugged in correctly. If it is reversed, the LEDs on the front of the disk drives will glow and the CPU DSK LED will not go out. Do not use P502 unless you have drives plugged into P501, or software that is configured to support drives 2 and 3 (hardware unit numbers — drives 0 and 1 should be plugged into P501).

8. Run the disk read test from the Monitor ROM (Test 1). This test will give the same results for both a drive plugged into P501 and a drive plugged into P502. However, you cannot boot an unmodified MS-DOS from P502 without the correct device drivers and/or a modified command interpreter.

9. If the diagnostic disk is available and can be booted, refer to the *Disk-Based Diagnostics Manual*, Chapter 6, "Floppy Disk Diagnostics," and run the tests. Be aware, however, that these tests are designed to check drive reliability and will not aid you in locating problems in the controller, especially if you used it to boot the diagnostic disk.

10. If none of the preceding checks have resulted in any positive identification of the problem, replace the floppy disk controller serial input/output card and rerun your checks. This should isolate the problem to the card. If the card is at fault, use Table 6.2 for checking the individual components.

Table 6.2. Floppy Disk Controller Component Failures

SYMPTOM	SUSPECTED PARTS	THINGS TO CHECK
General	Cables and cards	Check all cables and cards to make sure they are installed correctly. Improperly installed cables can create a number of problems, most of which should have shown up during the previous quick checks.
Display indicates no controller present.	U521	
Drive motors don't turn on.	U533, U527, U528, U514, U529, U518 power supply voltages	Check each chip for the MOTOR signal. U533 → U527 → U528 (pin 15). Check the input to U528 with the input and output signals in Table 5.3 and Figure 5.2.
Drive motors come on but don't stay on.	U514A, C529, R560	Check the width of the pulse after last access. It should last from 2 to 3 seconds.
Data is "garbaged" coming from a good disk.	U530, U503, U510	Read errors going into memory; DMA signals. Without proper DMA signals, the DMA processor may not be handling the signals correctly. Also check the DMA processor on the CPU card.
Bad card addressing or selection	U519, U529, U511, U527	Check for correct address decoding.
Read sector errors	U531, U512	Check for correct index line coming from the drives.
Precomp problems	U510, U525, U513, U516, U526 U505, U504	Check for correct precomp signals (early, late). Also check VCO bias voltage (TP2) and frequency (TP1).
Garbaged data	U514, U516, U525	Check signal pulse sizes (see circuit description for details).
Won't write to disk	U510, U525, U530, U511	Check for write gate (WRITE ENABLE from U510 through U511 to both U530 and U525).

Chapter 7

Parts List

The floppy disk controller card is part number HE 181-4647, or HE 181-5325. Refer to Figure 7.1 to identify replacement parts. An X in the parts list represents the presence of a particular part on the indicated floppy disk controller card.

CAUTION: This card contains electrostatic-sensitive devices (ESDs). Exercise extreme care in handling these devices to prevent damage.

NOTE: Refer to the Semiconductor Identification section of this chapter or Chapter 8, "Manufacturer's Data Sheets," for descriptions of semiconductor devices.

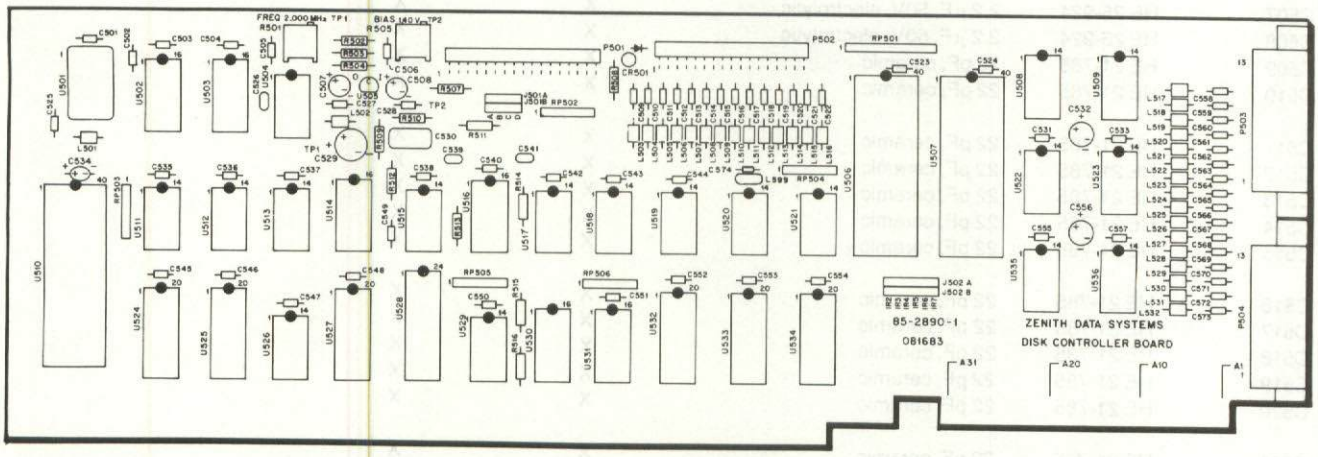


Figure 7.1. Floppy Disk Controller Card Component View

Floppy Disk Controller Card Parts

REFERENCE DESIGNATOR	HEATH PART NUMBER	DESCRIPTION	HE 181-4647	HE 181-5325
Capacitors				
C501	HE 21-786	.1 µF ceramic	X	X
C502	HE 21-786	.1 µF ceramic	X	X
C503	HE 21-786	.1 µF ceramic	X	X
C504	HE 21-786	.1 µF ceramic	X	X
C505	HE 21-769	.01 µF ceramic	X	X
C506	HE 21-769	.01 µF ceramic	X	X
C507	HE 25-924	2.2 µF, 50V, electrolytic	X	X
C508	HE 25-924	2.2 µF, 50V, electrolytic	X	X
C509	HE 21-785	22 pF, ceramic	X	X
C510	HE 21-785	22 pF, ceramic	X	X
C511	HE 21-785	22 pF, ceramic	X	X
C512	HE 21-785	22 pF, ceramic	X	X
C513	HE 21-785	22 pF, ceramic	X	X
C514	HE 21-785	22 pF, ceramic	X	X
C515	HE 21-785	22 pF, ceramic	X	X
C516	HE 21-785	22 pF, ceramic	X	X
C517	HE 21-785	22 pF, ceramic	X	X
C518	HE 21-785	22 pF, ceramic	X	X
C519	HE 21-785	22 pF, ceramic	X	X
C520	HE 21-785	22 pF, ceramic	X	X
C521	HE 21-785	22 pF, ceramic	X	X
C522	HE 21-785	22 pF, ceramic	X	X
C523	HE 21-786	.1 µF, ceramic	X	X
C524	HE 21-786	.1 µF, ceramic	X	X
C525	HE 21-786	.1 µF, ceramic	X	X
C526	HE 21-744	82 pF, ceramic	X	X
C527	HE 21-786	.1 µF, ceramic	X	X
C528	HE 21-786	.1 µF, ceramic	X	X
C529	HE 25-918	100 µF, electrolytic	X	X
C530	HE 21-786	.1 µF, ceramic	X	X
C531	HE 27-217	.68 µF, Mylar	X	X
C532	HE 25-917	10 µF, electrolytic	X	X
C533	HE 21-786	.1 µF, ceramic	X	X
C534	HE 25-841	4.7 µF, tantalum	X	X
C535	HE 21-786	.1 µF, ceramic	X	X
C536	HE 21-786	.1 µF, ceramic	X	X
C537	HE 21-786	.1 µF, ceramic	X	X
C538	HE 21-786	.1 µF, ceramic	X	X
C539	HE 21-744	82 pF, ceramic	X	X
C540	HE 21-786	.1 µF, ceramic	X	X

REFERENCE DESIGNATOR	HEATH PART NUMBER	DESCRIPTION	HE 181-4647	HE 181-5325
Capacitors (continued)				
C541	HE 21-744	82 pF, ceramic	X	X
C542	HE 21-786	.1 µF, ceramic	X	X
C543	HE 21-786	.1 µF, ceramic	X	X
C544	HE 21-786	.1 µF, ceramic	X	X
C545	HE 21-786	.1 µF, ceramic	X	X
C546	HE 21-786	.1 µf, ceramic	X	X
C547	HE 21-786	.1 µF, ceramic	X	X
C548	HE 21-786	.1 µF, ceramic	X	X
C549	HE 21-785	22 pF, ceramic	X	X
C550	HE 21-786	.1 µF, ceramic	X	X
C551	HE 21-786	.1 µF, ceramic	X	X
C552	HE 21-786	.1 µF, ceramic	X	X
C553	HE 21-786	.1 µF, ceramic	X	X
C554	HE 21-786	.1 µF, ceramic	X	X
C555	HE 21-786	.1 µF, ceramic	X	X
C556	HE 25-917	10 µF, electrolytic	X	X
C557	HE 21-786	.1 µF, ceramic	X	X
C558	HE 21-785	22 pF, ceramic	X	X
C559	HE 21-785	22 pF, ceramic	X	X
C560	HE 21-785	22 pF, ceramic	X	X
C561	HE 21-785	22 pF, ceramic	X	X
C562	HE 21-785	22 pF, ceramic	X	X
C563	HE 21-785	22 pF, ceramic	X	X
C564	HE 21-785	22 pF, ceramic	X	X
C565	HE 21-785	22 pF, ceramic	X	X
C566	HE 21-785	22 pF, ceramic	X	
C567	HE 21-785	22 pF, ceramic	X	
C568	HE 21-785	22 pF, ceramic	X	
C569	HE 21-785	22 pF, ceramic	X	
C570	HE 21-785	22 pF, ceramic	X	
C571	HE 21-785	22 pF, ceramic	X	
C572	HE 21-785	22 pF, ceramic	X	
C573	HE 21-785	22 pF, ceramic	X	
C574	HE 21-786	.1 µF, ceramic	X	X
LED				
CR501	HE 412-654 LED		X	X
Connectors				
J501 A	HE 432-1129	4-pin MOLEX	X	X
J501 B	HE 432-1129	4-pin MOLEX	X	X
J502 A	HE 432-1130	6-pin MOLEX	X	
J502 B	HE 432-1130	6-pin MOLEX	X	

Parts List

REFERENCE DESIGNATOR	HEATH PART NUMBER	DESCRIPTION	HE 181-4647	HE 181-5325
Connectors (continued)				
P501	HE 432-1302	34-pin	X	X
P502	HE 432-1302	34-pin	X	X
P503	HE 432-1381	25-pin (DTE-RS-232)	X	X
P504	HE 432-1381	25-pin (DTE-RS-232)	X	
TP1	HE 432-121	34-pin	X	X
TP2	HE 432-121	34-pin	X	X
RF Chokes				
L501	HE 475-33	Ferrite core	X	X
L502	HE 475-33	Ferrite core	X	X
L503	HE 475-33	Ferrite core	X	X
L504	HE 475-33	Ferrite core	X	X
L505	HE 475-33	Ferrite core	X	X
L506	HE 475-33	Ferrite core	X	X
L507	HE 475-33	Ferrite core	X	X
L508	HE 475-33	Ferrite core	X	X
L509	HE 475-33	Ferrite core	X	X
L510	HE 475-33	Ferrite core	X	X
L511	HE 475-33	Ferrite core	X	X
L512	HE 475-33	Ferrite core	X	X
L513	HE 475-33	Ferrite core	X	X
L514	HE 475-33	Ferrite core	X	X
L515	HE 475-33	Ferrite core	X	X
L516	HE 475-33	Ferrite core	X	X
L517	HE 475-33	Ferrite core	X	X
L518	HE 475-33	Ferrite core	X	X
L519	HE 475-33	Ferrite core	X	X
L520	HE 475-33	Ferrite core	X	X
L521	HE 475-33	Ferrite core	X	X
L522	HE 475-33	Ferrite core	X	X
L523	HE 475-33	Ferrite core	X	X
L524	HE 475-33	Ferrite core	X	X
L525	HE 475-33	Ferrite core	X	X
L526	HE 475-33	Ferrite core	X	
L527	HE 475-33	Ferrite core	X	
L528	HE 475-33	Ferrite core	X	
L529	HE 475-33	Ferrite core	X	
L530	HE 475-33	Ferrite core	X	
L531	HE 475-33	Ferrite core	X	
L532	HE 475-33	Ferrite core	X	
L599	HE 235-229	35 µH	X	X

REFERENCE DESIGNATOR	HEATH PART NUMBER	DESCRIPTION	HE 181-4647	HE 181-5325
Controls and Resistors				
R501	HE 10-1154	10KΩ, control	X	X
R502	HE 6-103	10KΩ, 5% resistor	X	X
R503	HE 6-103	10KΩ, 5% resistor	X	X
R504	HE 6-473	47KΩ, 5% resistor	X	X
R505	HE 10-1180	100KΩ, control	X	X
R506	Not Used		X	X
R507	HE 6-473	47KΩ, 5% resistor	X	X
R508	HE 6-561	560 Ω, 5% resistor	X	X
R509	HE 6-564	560KΩ, 5% resistor	X	X
R510	HE 6-680	68 Ω, 5% resistor	X	X
R511	HE 6-102	1000 Ω, 5% resistor	X	X
R512	HE 6-1001	1000 Ω, 1% resistor	X	X
R513	HE 6-103	10KΩ, 5% resistor	X	X
R514	HE 6-4991	4990 Ω, 1% resistor	X	X
R515	HE 6-202	2000 Ω, 5% resistor	X	X
R516	HE 6-202	2000 Ω, 5% resistor	X	X
Resistor Packs				
RP501	HE 9-133	4.7KΩ	X	X
RP502	HE 9-120	150 Ω	X	X
RP503	HE 9-124	4.7 KΩ	X	X
RP504	HE 9-120	150 Ω	X	X
RP505	HE 9-124	4.7 Ω	X	X
RP506	HE 9-120	150 Ω	X	X
Integrated Circuits				
U501	HE 150-132	4.000 MHz crystal oscillator	X	X
U502	HE 443-757	74LS161 4-bit counter	X	X
	HE 434-299	16-pin DIP IC socket	X	X
U503	HE 443-752	74LS175 Quad D flip-flop	X	X
	HE 434-299	16-pin DIP IC socket	X	X
U504	HE 443-999	74LS624 Voltage controlled oscillator	X	X
	HE 434-298	14-pin DIP IC socket	X	X
U505	HE 442-627	78L05 5-volt regulator	X	X
U506	HE 443-874	8250 ACE	X	
	HE 434-253	40-pin DIP IC socket	X	
U507	HE 443-874	8250 ACE	X	X
	HE 434-253	40-pin DIP IC socket	X	X
U508	HE 443-811	74LS125 Quad buffer, tri-state	X	X
	HE 434-298	14-pin DIP IC socket	X	X

Parts List

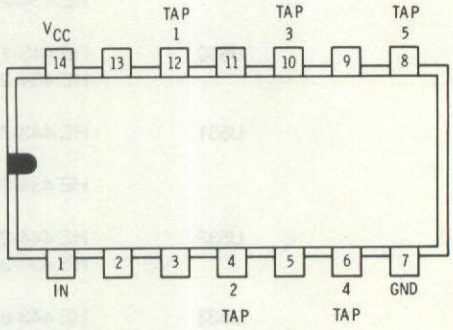
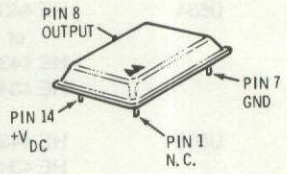
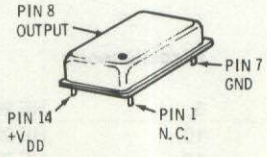
REFERENCE DESIGNATOR	HEATH PART NUMBER	DESCRIPTION	HE 181-4647	HE 181-5325
Integrated Circuits (continued)				
U509	Not Used			
U510	HE 443-944	µPD765 Floppy disk controller	X	X
	HE 434-253	40-pin DIP IC socket	X	X
U511	HE 443-875	74LS32 Quad 2-input OR gate	X	X
	or			
	HE 443-1072	74ALS32 Quad 2-input OR gate	X	X
	HE 434-298	14-pin DIP IC socket	X	X
U512	HE 443-755	74LS04 Hex inverter	X	X
	or			
	HE 443-1082	74ALS04 Hex inverter	X	X
	HE 434-298	14-pin DIP IC socket	X	X
U513	HE 41-17	125 ns Delay module	X	X
	HE 434-298	14-pin DIP IC socket	X	X
U514	HE 443-1040	96LS02 Multivibrator	X	X
	HE 434-299	16-pin DIP IC socket	X	X
U515	HE 443-72	7417 Hex buffer, open collector	X	X
	HE 434-298	14-pin DIP IC socket	X	X
U516	HE 443-1112	9602 Retriggerable monostable multivibrator	X	X
	HE 434-299	16-pin DIP IC socket	X	X
U517	HE 443-72	7417 Hex buffer, open collector	X	X
	HE 434-298	14-pin DIP IC socket	X	X
U518	HE 443-72	7417 Hex buffer, open collector	X	X
	HE 434-298	14-pin DIP IC socket	X	X
U519	HE 443-732	74LS30 8-input NAND gate	X	X
	or			
	HE 443-1231	74ALS30 8-input NAND gate	X	X
	HE 434-298	14-pin DIP IC socket	X	X
U520	HE 150-165	.8432 MHz crystal oscillator	X	X
U521	HE 443-875	74LS32 Quad 2-input OR gate	X	X
	or			
	HE 443-1072	74ALS32 Quad 2-input OR gate	X	X
	HE 434-298	14-pin DIP IC socket	X	X
U522	Not Used			
U523	HE 443-794	75188 TTL RS-232 Driver	X	X
	HE 434-298	14-pin DIP IC socket	X	X

REFERENCE DESIGNATOR	HEATH PART NUMBER	DESCRIPTION	HE 181-4647	HE 181-5325
Integrated Circuits (continued)				
U524	HE 443-754	74LS240 Octal buffer, tri-state	X	X
	HE 434-311	20-pin DIP IC socket	X	X
U525	HE 443-998	1691 Phase-locked loop	X	X
	HE 434-311	20-pin DIP IC socket	X	X
U526	HE 443-872	74LS14 Hex inverter	X	X
	HE 434-298	14-pin DIP IC socket	X	X
U527	HE 443-805	74LS273 Octal D flip-flop	X	X
	HE 434-311	20-pin DIP IC socket	X	X
U528	HE 444-226	PAL	X	X
	HE 434-368	24-pin DIP IC socket	X	X
U529	HE 443-779	74LS02 Quad 2-input NOR gate	X	X
	or			
	HE 443-1045	74ALS02 Quad 2-input NOR gate	X	X
	HE 434-298	14-pin DIP IC socket	X	X
U530	HE 443-1167	3487 Quad RS-422 line driver	X	X
	HE 434-299	16-pin DIP IC socket	X	X
U531	HE 443-799	74LS157 Quad 2-input multiplexer	X	X
	HE 434-299	16-pin DIP IC socket	X	X
U532	HE 444-227	PAL	X	X
	HE 434-311	20-pin DIP IC socket	X	X
U533	HE 443-885	74LS245 Transceiver	X	X
	HE 434-311	20-pin DIP IC socket	X	X
U534	HE 443-885	74LS245 Transceiver	X	X
	or			
	HE 443-1097	74ALS245 Transceiver	X	X
	HE 434-311	20-pin DIP IC socket	X	X
U535	HE 443-795	75189 TTL RS-232 Receiver	X	
	HE 434-298	14-pin DIP IC socket	X	
U536	HE 443-794	75188 TTL RS-232 Driver	X	
	HE 434-298	14-pin DIP IC socket	X	
Miscellaneous				
5	HE 204-2720	Bracket	X	X
10	HE 255-757	Spacer, hex 4-40 × .190	X	X
15	HE 255-757	Spacer, hex 4-40 × .190	X	X
20	HE 255-757	Spacer, hex 4-40 × .190	X	X
25	HE 255-757	Spacer, hex 4-40 × .190	X	X
30	HE 432-1041	2-pin BERG jumper	X	

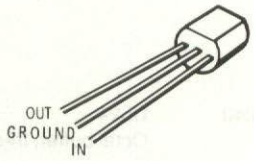
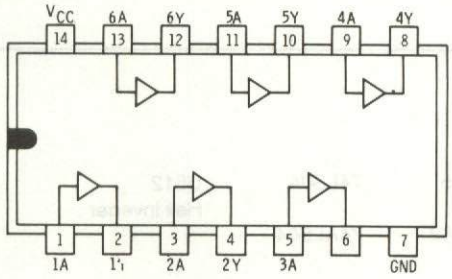
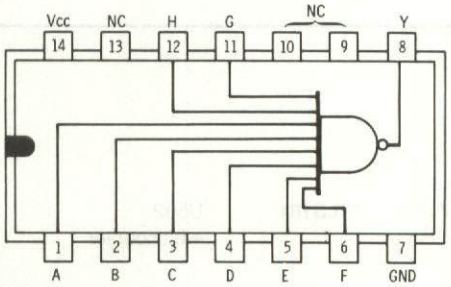
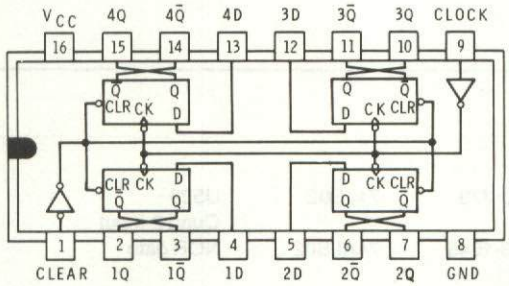
Semiconductor Identification

This section provides assistance in semiconductor identification by use of a cross reference between Heath part numbers and semiconductor part numbers. The Heath part numbers are listed in numerical order with replacement part numbers (if available), description, and lead configuration in adjacent columns. The PAL equations are repeated in this chapter.

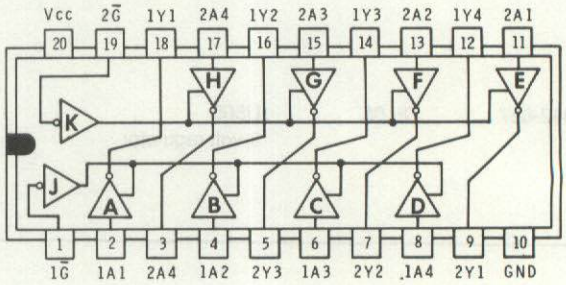
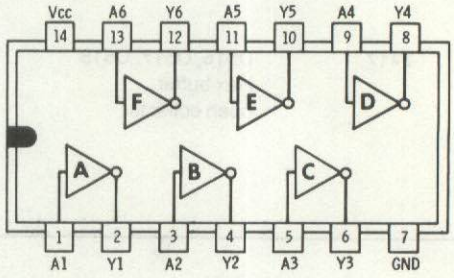
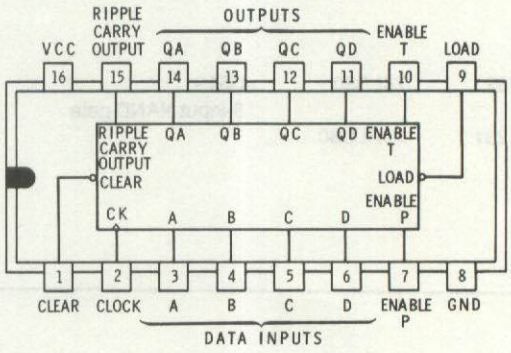
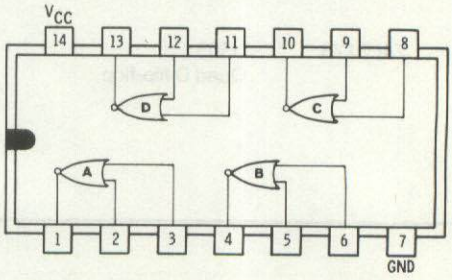
Part Number Index

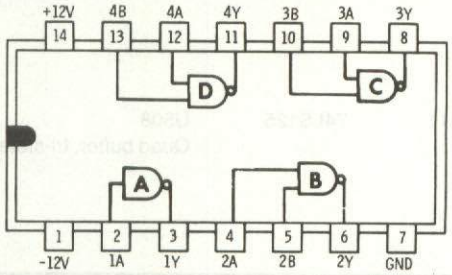
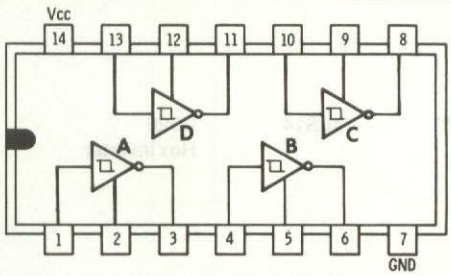
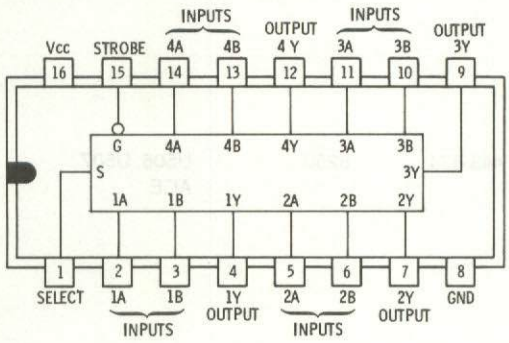
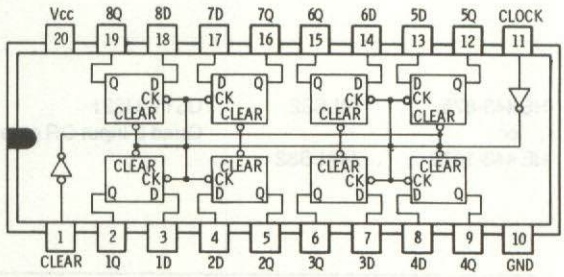
HEATH PART NUMBER	MAY BE REPLACED BY	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
HE 41-17		U513 125 ns Delay module	
HE 150-132		U501 4.000 MHz crystal oscillator	
HE 150-165		U520 1.8432 MHz crystal oscillator	

Parts List

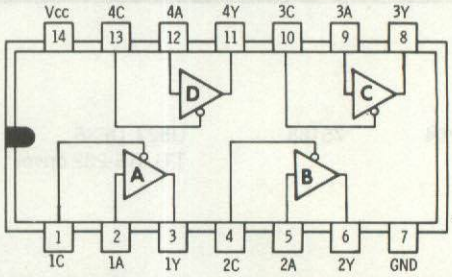
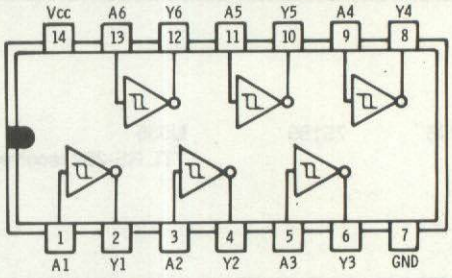
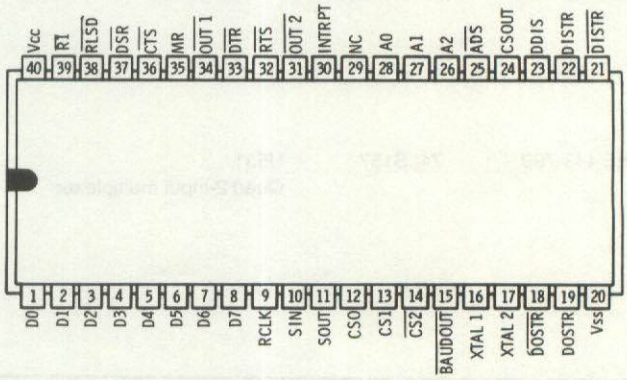
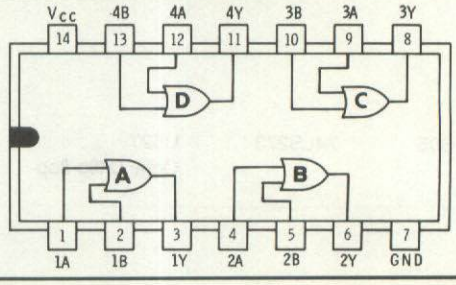
HEATH PART NUMBER	MAY BE REPLACED BY	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
HE 442-627	78L05	U505 5-volt regulator	
HE 443-72	7417	U515, U517, U518 Hex buffer, open collector	
HE 443-732 or HE 443-1231	74LS30 74ALS30	U519 8-input NAND gate	
HE 443-752	74LS175	U503 Quad D flip-flop	

Parts List

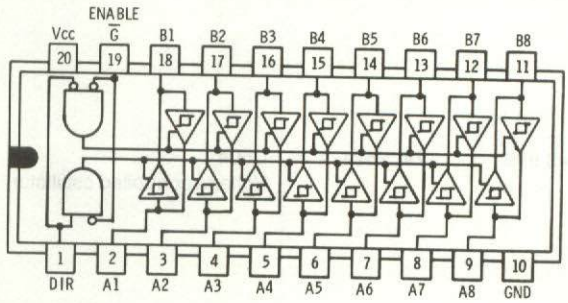
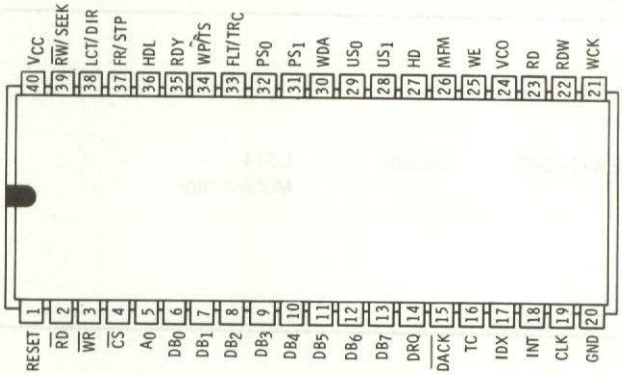
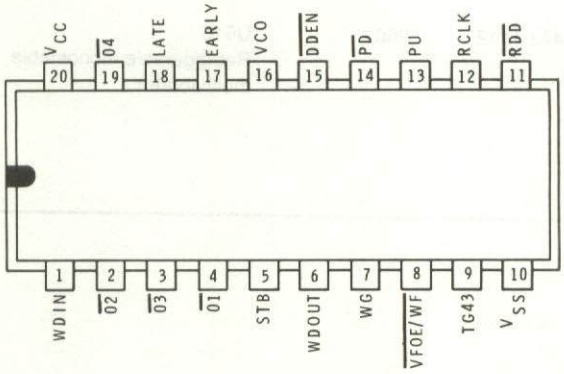
HEATH PART NUMBER	MAY BE REPLACED BY	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
HE 443-754	74LS240	U524 Octal buffer, tri-state	
HE 443-755 or HE 443-1082	74LS04 74ALS04	U512 Hex inverter	
HE 443-757	74LS161	U502 4-bit counter	
HE 443-779 or HE 443-1045	74LS02 74ALS02	U529 Quad 2-input NOR gate	

HEATH PART NUMBER	MAY BE REPLACED BY	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
HE 443-794	75188	U523, U536 TTL RS-232 driver	
HE 443-795	**75189**	**U535** **TTL RS-232 receiver**	
HE 443-799	74LS157	U531 Quad 2-input multiplexer	
HE 443-805	74LS273	U527 Octal D flip-flop	

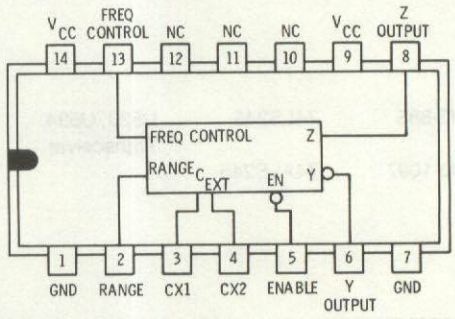
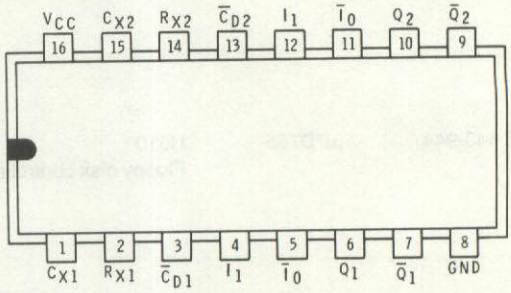
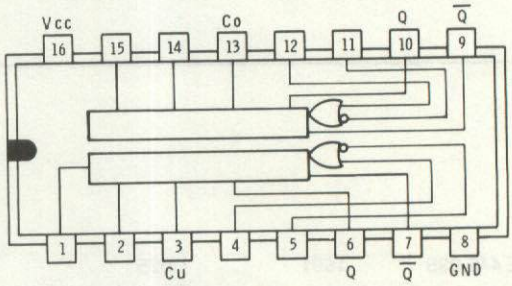
Parts List

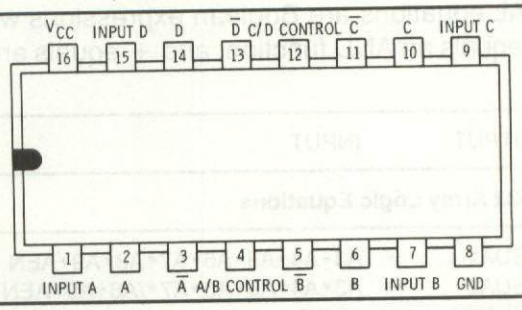
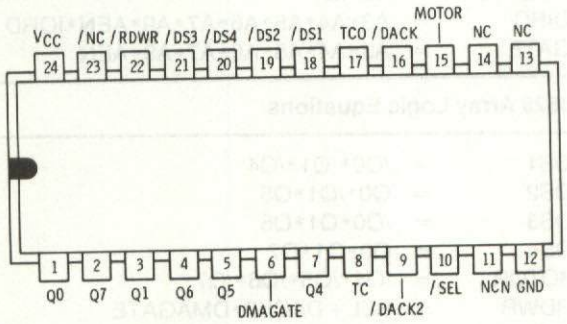
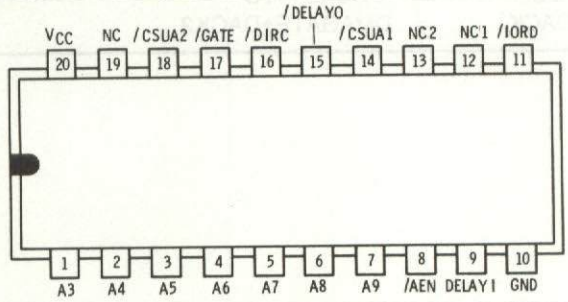
HEATH PART NUMBER	MAY BE REPLACED BY	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
HE 443-811	74LS125	U508 Quad buffer, tri-state	
HE 443-872	74LS14	U526 Hex inverter	
HE 443-874	8250	U506, U507 ACE	
HE 443-875 **or** **HE 443-1072**	**74LS32** **74ALS32**	**U511, U521** **Quad 2-input OR gate**	

Parts List

HEATH PART NUMBER	MAY BE REPLACED BY	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
HE 443-885 or HE 443-1097	74LS245 74ALS245	U533, U534 Transceiver	
HE 443-944	µPD765	U510 Floppy disk controller	
HE 443-998	1691	U525 Phase-locked loop	

Parts List

HEATH PART NUMBER	MAY BE REPLACED BY	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
HE 443-999	74LS624	U504 Voltage controlled oscillator	
HE 443-1040	96LS02	U514 Multivibrator	
HE 443-1112	9602	U516 Retriggerable monostable multivibrator	

HEATH PART NUMBER	MAY BE REPLACED BY	DESCRIPTION	LEAD CONFIGURATION (TOP VIEW)
HE 443-1167	3487	U530 Quad RS-422 line driver	
HE 444-226		U528 Programmable Array Logic (PAL)	
HE 444-227		U532 Programmable Array Logic (PAL)	

PAL Equations

PAL equations are Boolean expressions where / equals a negated signal, * equals an AND function, and + equals an OR function.

OUTPUT		INPUT
U532 Array Logic Equations		
/CSUA1	=	A3*A4*A5*A6*A7*A8*A9*AEN
/CSUA2	=	A3*A4*A5*A6*A7*/A8*A9*AEN
/DELAYO	=	/IORD
/DIRC	=	A3*A4*A5*A6*A7*A9*AEN*IORD + A3*A4*A5*A6*A7*A9*DELAYI*AEN
/GATE	=	A3*A4*A5*A6*A7*A9*AEN
U528 Array Logic Equations		
/DS1	=	/Q0*/Q1*/Q4
/DS2	=	Q0*/Q1*Q5
/DS3	=	/Q0*Q1*Q6
/DS4	=	Q0*Q1*Q7
MOTOR	=	/Q4*/Q5*/Q6*/Q7
/RDWR	=	SEL + DACK2*DMAGATE
TCO	=	/DACK2 + /TC
/DACK	=	DMAGATE*DACK2

Chapter 8

Manufacturer's Data Sheets

The following pages contain data sheets. The μPD765A Single/Double Density Floppy Disk Controller data sheet is reprinted with permission of, and licensed by, NEC Electronics Inc. Copyright NEC Electronics Inc. 1984.

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Western Digital WD8250 Asynchronous Communication Element
Western Digital 1691 Floppy Support Logic

NEC
NEC Electronics U.S.A. Inc.
Microcomputer Division

μPD765A

SINGLE/DOUBLE DENSITY FLOPPY DISK CONTROLLER

DESCRIPTION

The μPD765 is an LSI Floppy Disk Controller (FDC) Chip, which contains the circuitry and control functions for interfacing a processor to 4 Floppy Disk Drives. It is capable of supporting either IBM 3740 single density format (FM), or IBM System 34 Double Density format (MFM) including double sided recording. The μPD765 provides control signals which simplify the design of an external phase locked loop, and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a Floppy Disk Interface.

Hand-shaking signals are provided in the μPD765 which make DMA operation easy to incorporate with the aid of an external DMA Controller chip, such as the μPD8257. The FDC will operate in either DMA or Non-DMA mode. In the Non-DMA mode, the FDC generates interrupts to the processor every time a data byte is available. In the DMA mode, the processor need only load the command into the FDC and all data transfers occur under control of the μPD765 and DMA controller.

There are 15 separate commands which the μPD765 will execute. Each of these commands require multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available:

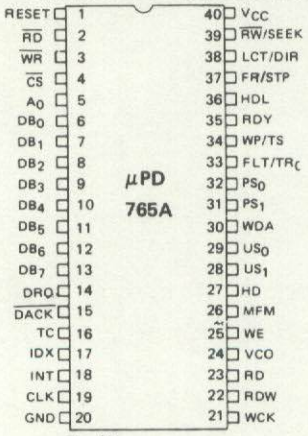
Read Data	Scan High or Equal	Write Deleted Data
Read ID	Scan Low or Equal	Seek
Read Deleted Data	Specify	Recalibrate (Restore to Track 0)
Read a Track	Write Data	Sense Interrupt Status
Scan Equal	Format a Track	Sense Drive Status

FEATURES

Address mark detection circuitry is internal to the FDC which simplifies the phase locked loop and read electronics. The track stepping rate, head load time, and head unload time may be programmed by the user. The μPD765 offers many additional features such as multiple sector transfers in both read and write with a single command, and full IBM compatibility in both single and double density modes.

- IBM Compatible in Both Single and Double Density Recording Formats
- Programmable Data Record Lengths: 128, 256, 512, or 1024 Bytes/Sector
- Multi-Sector and Multi-Track Transfer Capability
- Drive Up to 4 Floppy Disks
- Data Scan Capability — Will Scan a Single Sector or an Entire Cylinder's Worth of Data Fields, Comparing on a Byte by Byte Basis, Data in the Processor's Memory with Data Read from the Diskette
- Data Transfers in DMA or Non-DMA Mode
- Parallel Seek Operations on Up to Four Drives
- Compatible with Most Microprocessors Including 8080A, 8085A, μPD780 (Z80™)
- Single Phase 8 MHz Clock
- Single +5 Volt Power Supply
- Available in 40 Pin Plastic Dual-in-Line Package

PIN CONFIGURATION

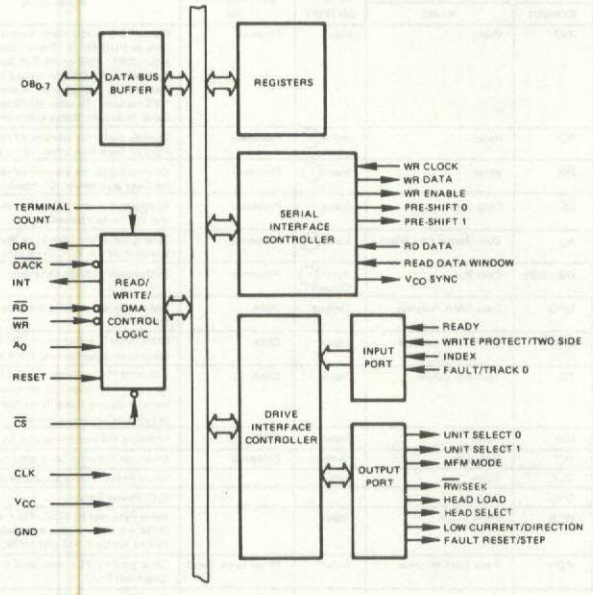


TM:Z80 is a registered trademark of Zilog, Inc.

Rev/3

μPD765A

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-10°C to +70°C
Storage Temperature	-55°C to +150°C
All Output Voltages	-0.5 to +7 Volts
All Input Voltages	-0.5 to +7 Volts
Supply Voltage V_{CC}	-0.5 to +7 Volts
Power Dissipation	1 Watt

T_a = 25°C

*COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

T_a = -10°C to +70°C; V_{CC} = +5V ± 5% unless otherwise specified.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP①	MAX		
Input Low Voltage	V_{IL}	-0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.5	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = -200 μA
Input Low Voltage (CLK + WR Clock)	$V_{IL(\Phi)}$	-0.5		0.65	V	
Input High Voltage (CLK + WR Clock)	$V_{IH(\Phi)}$	2.4		V_{CC} + 0.5	V	
V_{CC} Supply Current	I_{CC}			150	mA	
Input Load Current (All Input Pins)	I_{LI}			10	μA	V_{IN} = V_{CC}
				-10	μA	V_{IN} = 0V
High Level Output Leakage Current	I_{LOH}			10	μA	V_{OUT} = V_{CC}
Low Level Output Leakage Current	I_{LOL}			-10	μA	V_{OUT} = +0.45V

Note: ① Typical values for T_a = 25°C and nominal supply voltage.

μPD765A

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	INPUT/ OUTPUT	CONNECTION TO	FUNCTION
1	RST	Reset	Input	Processor	Places FDC in idle state. Resets output lines to FDD to "0" (low). Does not effect SRT, HUT or HLT in Specify command. If RDY pin is held high during Reset, FDC will generate interrupt 1-25 ms later. To clear this interrupt use Sense Interrupt Status command.
2	$\overline{RD}$	Read	Input(1)	Processor	Control signal for transfer of data from FDC to Data Bus, when "0" (low).
3	$\overline{WR}$	Write	Input(1)	Processor	Control signal for transfer of data to FDC via Data Bus, when "0" (low).
4	$\overline{CS}$	Chip Select	Input	Processor	IC selected when "0" (low), allowing $\overline{RD}$ and $\overline{WR}$ to be enabled.
5	A_0	Data/Status Reg Select	Input(1)	Processor	Selects Data Reg (A_0=1) or Status Reg (A_0=0) contents of the FDC to be sent to Data Bus.
6-13	DB_0-DB_7	Data Bus	Input/(1) Output	Processor	Bi-Directional 8-Bit Data Bus.
14	DRQ	Data DMA Request	Output	DMA	DMA Request is being made by FDC when DRQ="1".
15	$\overline{DACK}$	DMA Acknowledge	Input	DMA	DMA cycle is active when "0" (low) and Controller is performing DMA transfer.
16	TC	Terminal Count	Input	DMA	Indicates the termination of a DMA transfer when "1" (high). It terminates data transfer during Read/Write/Scan command in DMA or interrupt mode.
17	IDX	Index	Input	FDD	Indicates the beginning of a disk track.
18	INT	Interrupt	Output	Processor	Interrupt Request Generated by FDC.
19	CLK	Clock	Input		Single Phase 8 MHz Squarewave Clock.
20	GND	Ground			D.C. Power Return.
21	WCK	Write Clock	Input		Write data rate to FDD. FM = 500 kHz, MFM = 1 MHz, with a pulse width of 250 ns for both FM and MFM.
22	RDW	Read Data Window	Input	Phase Lock Loop	Generated by PLL, and used to sample data from FDD.
23	RDD	Read Data	Input	FDD	Read data from FDD, containing clock and data bits.
24	VCO	VCO Sync	Output	Phase Lock Loop	Inhibits VCO in PLL when "0" (low), enables VCO when "1."
25	WE	Write Enable	Output	FDD	Enables write data into FDD.
26	MFM	MFM Mode	Output	Phase Lock Loop	MFM mode when "1," FM mode when "0."
27	HD	Head Select	Output	FDD	Head 1 selected when "1" (high), Head 0 selected when "0" (low).
28,29	US_1,US_0	Unit Select	Output	FDD	FDD Unit Selected.
30	WDA	Write Data	Output	FDD	Serial clock and data bits to FDD.
31,32	PS_1,PS_0	Precompensation (pre-shift)	Output	FDD	Write precompensation status during MFM mode. Determines early, late, and normal times.
33	FLT/TR_0	Fault/Track 0	Input	FDD	Senses FDD fault condition, in Read/ Write mode; and Track 0 condition in Seek mode.
34	WP/TS	Write Protect/ Two-Side	Input	FDD	Senses Write Protect status in Read/Write mode; and Two Side Media in Seek mode.
35	RDY	Ready	Input	FDD	Indicates FDD is ready to send or receive data.
36	HDL	Head Load	Output	FDD	Command which causes read/write head in FDD to contact diskette.
37	FR/STP	Flt Reset/Step	Output	FDD	Resets fault F.F. in FDD in Read/Write mode, contains step pulses to move head to another cylinder in Seek mode.
38	LCT/DIR	Low Current/ Direction	Output	FDD	Lowers Write current on inner tracks in Read/Write mode, determines direction head will step in Seek mode. A fault reset pulse is issued at the beginning of each Read or Write command prior to the occurrence of the Head Load signal.
39	$\overline{RW}$/SEEK	Read Write/SEEK	Output	FDD	When "1" (high) Seek mode selected and when "0" (low) Read/Write mode selected.
40	V_{CC}	+5V			DC Power.

Note: (1) Disabled when CS = 1.

CAPACITANCE

$T_a = 25°C$; $f_c = 1$ MHz; $V_{CC} = 0V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Input Capacitance	$C_{IN(\Phi)}$			20	pF	All Pins Except Pin Under Test Tied to AC Ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

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T_a = -10°C to +70°C; V_{CC} = +5V ± 5% unless otherwise specified.

AC CHARACTERISTICS

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP①	MAX		
Clock Period	Φ_{CY}	120	125	500	ns	
Clock Active (High, Low)	Φ_0	40			ns	
Clock Rise Time	Φ_r			20	ns	
Clock Fall Time	Φ_f			20	ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Set Up Time to $\overline{RD}$ ↓	T_{AR}	0			ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Hold Time from $\overline{RD}$ ↑	T_{RA}	0			ns	
$\overline{RD}$ Width	T_{RR}	250			ns	
Data Access Time from $\overline{RD}$ ↓	T_{RD}			200	ns	C_L = 100 pf
DB to Float Delay Time from $\overline{RD}$ ↑	T_{DF}	20		100	ns	C_L = 100 pF
A_0, $\overline{CS}$, $\overline{DACK}$ Set Up Time to $\overline{WR}$ ↓	T_{AW}	0			ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Hold Time to $\overline{WR}$ ↑	T_{WA}	0			ns	
$\overline{WR}$ Width	T_{WW}	250			ns	
Data Set Up Time to $\overline{WR}$ ↑	T_{DW}	150			ns	
Data Hold Time from $\overline{WR}$ ↑	T_{WD}	5			ns	
INT Delay Time from $\overline{RD}$ ↑	T_{RI}			500	ns	
INT Delay Time from $\overline{WR}$ ↑	T_{WI}			500	ns	
DRQ Cycle Time	T_{MCY}	13			μs	
DRQ Delay Time from $\overline{DACK}$ ↓	T_{AM}			200	ns	
TC Width	T_{TC}	1			ΦCY	
Reset Width	T_{RST}	14			ΦCY	
WCK Cycle Time	T_{CY}		2 or 4② 1 or 2		μs	MFM = 0 MFM = 1
WCK Active Time (High)	T_0	80	250	350	ns	
WCK Rise Time	T_r			20	ns	
WCK Fall Time	T_f			20	ns	
Pre-Shift Delay Time from WCK ↑	T_{CP}	20		100	ns	
WDA Delay Time from WCK ↑	T_{CD}	20		100	ns	
RDD Active Time (High)	T_{RDD}	40			ns	
Window Cycle Time	T_{WCY}		2.0 1.0		μs	MFM = 0 MFM = 1
Window Hold Time to/from RDD	T_{RDW} T_{WRD}	15			ns	
$US_{0,1}$ Hold Time to $\overline{RW}$/SEEK ↑	T_{US}	12			μs	
SEEK/RW Hold Time to LOW CURRENT/ DIRECTION ↑	T_{SD}	7			μs	
LOW CURRENT/DIRECTION Hold Time to FAULT RESET/STEP ↑	T_{DST}	1.0			μs	
$US_{0,1}$ Hold Time from FAULT RESET/STEP ↑	T_{STU}	5.0			μs	8 MHz Clock Period
STEP Active Time (High)	T_{STP}	6.0	7.0		μs	
STEP Cycle Time	T_{SC}	33	③	③	μs	
FAULT RESET Active Time (High)	T_{FR}	8.0		10	μs	
Write Data Width	T_{WDD}	T_0-50			ns	
$US_{0,1}$ Hold Time After SEEK	T_{SU}	15			μs	
Seek Hold Time from DIR	T_{DS}	30			μs	8 MHz Clock Period
DIR Hold Time after STEP	T_{STD}	24			μs	
Index Pulse Width	T_{IDX}	10			ΦCY	
$\overline{RD}$ ↓ Delay from DRQ	T_{MR}	800			ns	
$\overline{WR}$ ↓ Delay from DRQ	T_{MW}	250			ns	8 MHz Clock Period
$\overline{WE}$ or $\overline{RD}$ Response Time from DRQ ↑	T_{MRW}			12	μs	

Notes: ① Typical values for T_a = 25°C and nominal supply voltage.

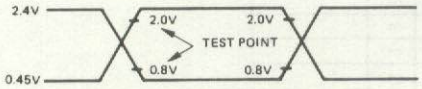
② The former value of 2 and 1 are applied to Standard Floppy, and the latter value of 4 and 2 are applied to Mini-floppy.

③ Under Software Control. The range is from 1 ms to 16 ms at 8 MHz Clock Period, and 2 to 32 ms at 4 MHz Clock Period.

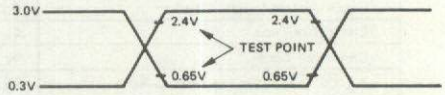
④ For mini-floppy applications, Φ_{CY} must be 4 mHz.

AC TEST CONDITION

INPUT/OUTPUT



CLOCK



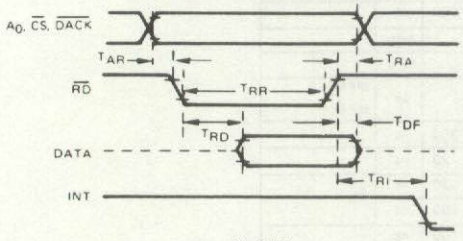
AC TESTING

Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0." Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0."

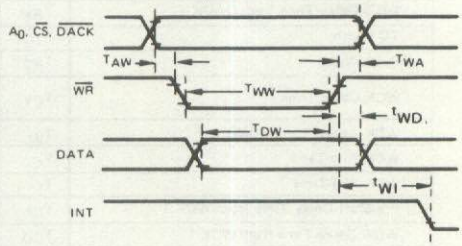
Clocks are driven at 3.0V for a logic "1" and 0.3V for a logic "0." Timing measurements are made at 2.4V for a logic "1" and 0.65V for a logic "0."

TIMING WAVEFORMS

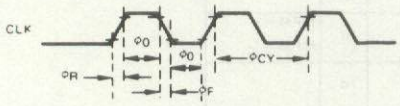
PROCESSOR READ OPERATION



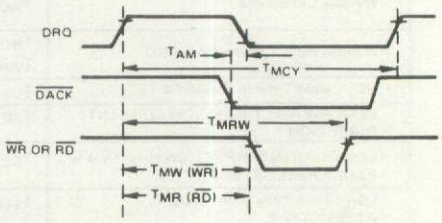
PROCESSOR WRITE OPERATION



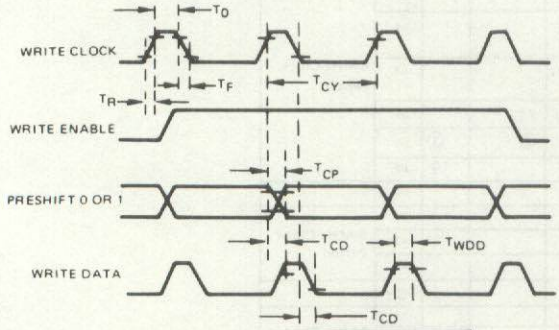
CLOCK



DMA OPERATION



FDD WRITE OPERATION



	PRESHIFT 0	PRESHIFT 1
NORMAL	0	0
LATE	0	1
EARLY	1	0
INVALID	1	1

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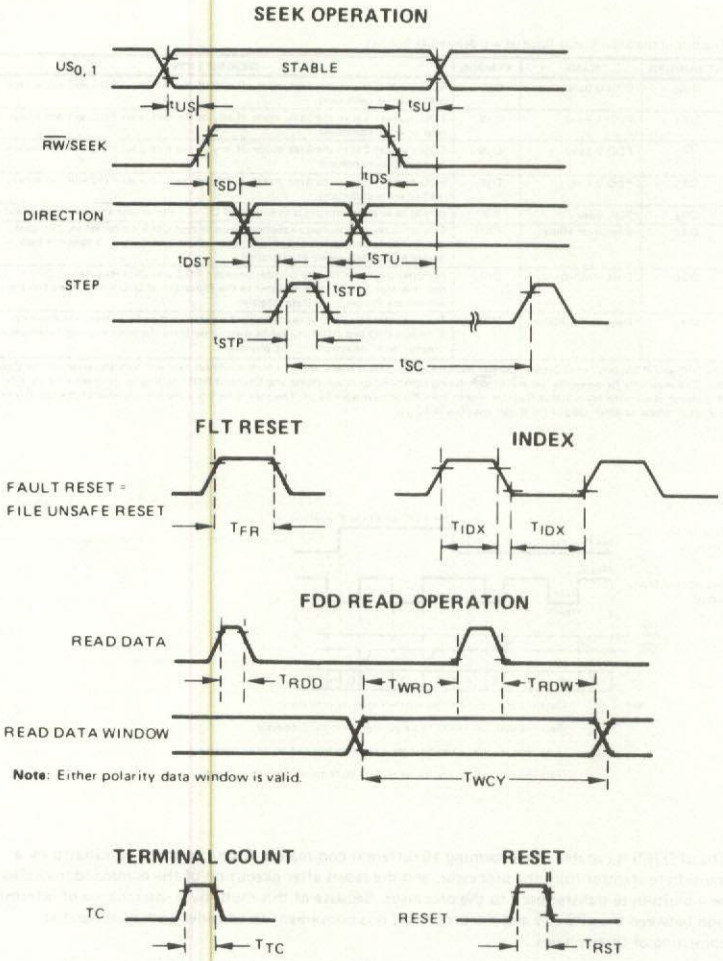
TIMING WAVEFORMS (CONT.)



INTERNAL REGISTERS

The μPD765 contains two registers which may be accessed by the main system processor; a Status Register and a Data Register. The 8-bit Main Status Register contains the status information of the FDC, and may be accessed at any time. The 8-bit Data Register (actually consists of several registers in a stack with only one register presented to the data bus at a time), which stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain the results after a particular command. The Status Register may only be read and is used to facilitate the transfer of data between the processor and μPD765.

The relationship between the Status/Data registers and the signals $\overline{RD}$, $\overline{WR}$, and A_0 is shown below.

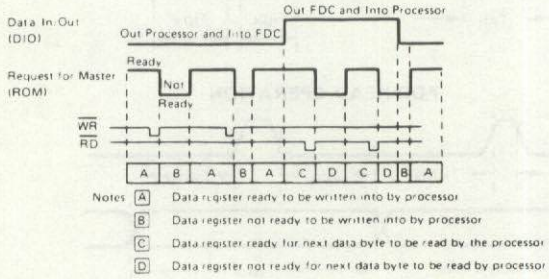
A_0	$\overline{RD}$	$\overline{WR}$	FUNCTION
0	0	1	Read Main Status Register
0	1	0	Illegal
0	0	0	Illegal
1	0	0	Illegal
1	0	1	Read from Data Register
1	1	0	Write into Data Register

INTERNAL REGISTERS (CONT.)

The bits in the Main Status Register are defined as follows:

BIT NUMBER	NAME	SYMBOL	DESCRIPTION
DB_0	FDD 0 Busy	D_0B	FDD number 0 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_1	FDD 1 Busy	D_1B	FDD number 1 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_2	FDD 2 Busy	D_2B	FDD number 2 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_3	FDD 3 Busy	D_3B	FDD number 3 is in the Seek mode. If any of the bits is set FDC will not accept read or write command.
DB_4	FDC Busy	CB	A read or write command is in process. FDC will not accept any other command.
DB_5	Execution Mode	EXM	This bit is set only during execution phase in non-DMA mode. When DB_5 goes low, execution phase has ended, and result phase was started. It operates only during NON-DMA mode of operation.
DB_6	Data Input/Output	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO = "1" then transfer is from Data Register to the Processor. If DIO = "0", then transfer is from the Processor to Data Register.
DB_7	Request for Master	RQM	Indicates Data Register is ready to send or receive data to or from the Processor. Both bits DIO and RQM should be used to perform the hand-shaking functions of "ready" and "direction" to the processor.

The DIO and RQM bits in the Status Register indicate when Data is ready and in which direction data will be transferred on the Data Bus. The max time between the last $\overline{RD}$ or $\overline{WR}$ during command or result phase and DIO and RQM getting set or reset is 12 μs. For this reason every time Main Status Register is read the CPU should wait 12 μs. The max time from the trailing edge of the last $\overline{RD}$ in the result phase to when DB_4 (FDC Busy) goes low is 12 μs.



COMMAND SEQUENCE

The μPD765 is capable of performing 15 different commands. Each command is initiated by a multi-byte transfer from the processor, and the result after execution of the command may also be a multi-byte transfer back to the processor. Because of this multi-byte interchange of information between the μPD765 and the processor, it is convenient to consider each command as consisting of three phases:

Command Phase:	The FDC receives all information required to perform a particular operation from the processor.
Execution Phase:	The FDC performs the operation it was instructed to do.
Result Phase:	After completion of the operation, status and other housekeeping information are made available to the processor.

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INSTRUCTION SET ① ②

PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
READ DATA										
Command	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
READ DELETED DATA										
Command	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
WRITE DATA										
Command	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the main-system and FDD
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
WRITE DELETED DATA										
Command	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are commanded against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
READ A TRACK										
Command	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system. FDC reads all data fields from index hole to EOT.
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
READ ID										
Command	W	0	MF	0	0	1	0	1	0	Commands
	W	X	X	X	X	X	HD	US1	US0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information read during Execution Phase from Floppy Disk
	R	H								
	R	R								
	R	N								
FORMAT A TRACK										
Command	W	0	MF	0	0	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	N								Bytes/Sector
	W	SC								Sectors/Track
	W	GPL								Gap 3
	W	D								Filler Byte
Execution										FDC formats an entire track
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								In this case, the ID information has no meaning
	R	H								
	R	R								
	R	N								
SCAN EQUAL										
Command	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data-compared between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

Note: ① Symbols used in this table are described at the end of this section.

② A_0 should equal binary 1 for all operations.

③ X = Don't care, usually made to equal binary 0.

INSTRUCTION SET (CONT.)

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PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
SCAN LOW OR EQUAL										
Command	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	———			C				———	Sector ID information prior Command execution
	W	———			H				———	
	W	———			R				———	
	W	———			N				———	
	W	———			EOT				———	
	W	———			GPL				———	
	W	———			STP				———	
Execution										Data-compared between the FDD and main-system
Result	R	———			ST 0				———	Status information after Command execution
	R	———			ST 1				———	
	R	———			ST 2				———	
	R	———			C				———	Sector ID information after Command execution
	R	———			H				———	
	R	———			R				———	
	R	———			N				———	
SCAN HIGH OR EQUAL										
Command	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	———			C				———	Sector ID information prior Command execution
	W	———			H				———	
	W	———			R				———	
	W	———			N				———	
	W	———			EOT				———	
	W	———			GPL				———	
	W	———			STP				———	
Execution										Data-compared between the FDD and main-system
Result	R	———			ST 0				———	Status information after Command execution
	R	———			ST 1				———	
	R	———			ST 2				———	
	R	———			C				———	Sector ID information after Command execution
	R	———			H				———	
	R	———			R				———	
	R	———			N				———	

PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
RECALIBRATE										
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	X	X	X	X	X	0	US1	US0	
Execution										Head retracted to Track 0
SENSE INTERRUPT STATUS										
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	———			STO				———	Status information at the end of seek-operation about the FDC
	R	———			PCN				———	
SPECIFY										
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	———	SRT			◄		HUT	———	
	W	———	HLT				►	ND	———	
SENSE DRIVE STATUS										
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
Result	R	———			ST 3				———	Status information about FDD
SEEK										
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	———			NCN				———	
Execution										Head is positioned over proper Cylinder on Diskette
INVALID										
Command	W	———			Invalid Codes				———	Invalid Command Codes (NoOp – FDC goes into Standby State)
Result	R	———			ST 0				———	ST 0 = 80 (16)

COMMAND SYMBOL DESCRIPTION

SYMBOL	NAME	DESCRIPTION
A_0	Address Line 0	A_0 controls selection of Main Status Register (A_0 = 0) or Data Register (A_0 = 1)
C	Cylinder Number	C stands for the current/selected Cylinder (track) number 0 through 76 of the medium.
D	Data	D stands for the data pattern which is going to be written into a Sector.
D_7-D_0	Data Bus	8-bit Data Bus, where D_7 stands for a most significant bit, and D_0 stands for a least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the Sector.
EOT	End of Track	EOT stands for the final Sector number on a Cylinder. During Read or Write operation FDC will stop date transfer after a sector # equal to EOT.
GPL	Gap Length	GPL stands for the length of Gap 3. During Read/Write commands this value determines the number of bytes that VCOs will stay low after two CRC bytes. During Format command it determines the size of Gap 3.
H	Head Address	H stands for head number 0 or 1, as specified in ID field.
HD	Head	HD stands for a selected head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words.)
HLT	Head Load Time	HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	HUT stands for the head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	If MF is low, FM mode is selected, and if it is high, MFM mode is selected.
MT	Multi-Track	If MT is high, a multi-track operation is to be performed. If MT = 1 after finishing Read/Write operation on side 0 FDC will automatically start searching for sector 1 on side 1.

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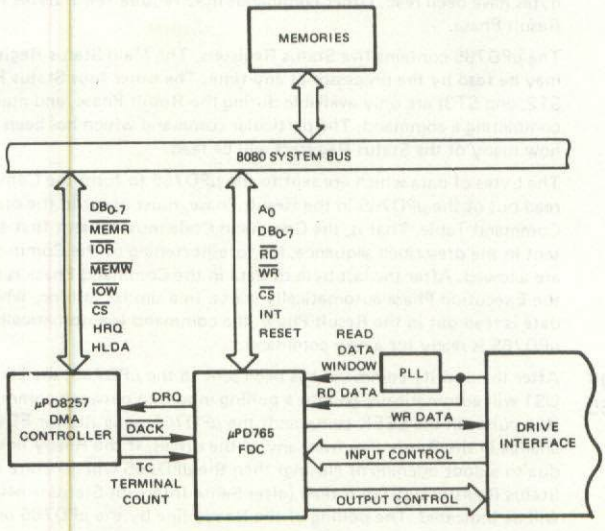
COMMAND SYMBOL DESCRIPTION (CONT.)

SYMBOL	NAME	DESCRIPTION
N	Number	N stands for the number of data bytes written in a Sector.
NCN	New Cylinder Number	NCN stands for a new Cylinder number, which is going to be reached as a result of the Seek operation. Desired position of Head.
ND	Non-DMA Mode	ND stands for operation in the Non-DMA Mode.
PCN	Present Cylinder Number	PCN stands for the Cylinder number at the completion of SENSE INTERRUPT STATUS Command. Position of Head at present time.
R	Record	R stands for the Sector number, which will be read or written.
R/W	Read/Write	R/W stands for either Read (R) or Write (W) signal.
SC	Sector	SC indicates the number of Sectors per Cylinder.
SK	Skip	SK stands for Skip Deleted Data Address Mark.
SRT	Step Rate Time	SRT stands for the Stepping Rate for the FDD. (1 to 16 ms in 1 ms increments.) Stepping Rate applies to all drives, (F = 1 ms, E = 2 ms, etc.).
ST 0 ST 1 ST 2 ST 3	Status 0 Status 1 Status 2 Status 3	ST 0-3 stand for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by $A_0 = 0$). ST 0-3 may be read only after a command has been executed and contain information relevant to that particular command.
STP		During a Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); and if STP = 2, then alternate sectors are read and compared.
US0, US1	Unit Select	US stands for a selected drive number 0 or 1.

SYSTEM CONFIGURATION



PROCESSOR INTERFACE

During Command or Result Phases the Main Status Register (described earlier) must be read by the processor before each byte of information is written into or read from the Data Register. After each byte of data read or written to Data Register, CPU should wait for 12 μs before reading MSR. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the μPD765. Many of the commands require multiple bytes, and as a result the Main Status Register must be read prior to each byte transfer to the μPD765. On the other hand, during the Result Phase, D6 and D7 in the Main Status Register must both be 1's (D6 = 1 and D7 = 1) before reading each byte from the Data Register. Note, this reading of the Main Status Register before each byte transfer to the μPD765 is required in only the Command and Result Phases, and NOT during the Execution Phase.

During the Execution Phase, the Main Status Register need not be read. If the μPD765 is in the NON-DMA Mode, then the receipt of each data byte (if μPD765 is reading data from FDD) is indicated by an Interrupt signal on pin 18 (INT = 1). The generation of a Read signal ($\overline{RD}$ = 0) or Write signal ($\overline{WR}$ = 0) will reset the Interrupt as well as output the Data onto the Data Bus. If the processor cannot handle Interrupts fast enough (every 13 μs) for MFM and 27 μs for FM mode, then it may poll the Main Status Register and then bit D7 (RQM) functions just like the Interrupt signal. If a Write Command is in process then the WR signal performs the reset to the Interrupt signal.

If the μPD765 is in the DMA Mode, no Interrupts are generated during the Execution Phase. The μPD765 generates DRQ's (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both a $\overline{DACK}$ = 0 (DMA Acknowledge) and a $\overline{RD}$ = 0 (Read signal). When the DMA Acknowledge signal goes low ($\overline{DACK}$ = 0) then the DMA Request is reset (DRQ = 0). If a Write Command has been programmed then a $\overline{WR}$ signal will appear instead of $\overline{RD}$. After the Execution Phase has been completed (Terminal Count has occurred) or EOT sector was read/written, then an Interrupt will occur (INT = 1). This signifies the beginning of the Result Phase. When the first byte of data is read during the Result Phase, the Interrupt is automatically reset (INT = 0).

It is important to note that during the Result Phase all bytes shown in the Command Table must be read. The Read Data Command, for example has seven bytes of data in the Result Phase. All seven bytes must be read in order to successfully complete the Read Data Command. The μPD765 will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result Phase.

The μPD765 contains five Status Registers. The Main Status Register mentioned above may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are only available during the Result Phase, and may be read only after completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

The bytes of data which are sent to the μPD765 to form the Command Phase, and are read out of the μPD765 in the Result Phase, must occur in the order shown in the Command Table. That is, the Command Code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result Phases are allowed. After the last byte of data in the Command Phase is sent to the μPD765, the Execution Phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result Phase, the command is automatically ended and the μPD765 is ready for a new command.

POLLING FEATURE OF THE μPD765

After the Specify command has been sent to the μPD765, the Unit Select line US0 and US1 will automatically go into a polling mode. In between commands (and between step pulses in the SEEK command) the μPD765 polls all four FDD's looking for a change in the Ready line from any of the drives. If the Ready line changes state (usually due to a door opening or closing) then the μPD765 will generate an interrupt. When Status Register 0 (ST0) is read (after Sense Interrupt Status is issued), Not Ready (NR) will be indicated. The polling of the Ready line by the μPD765 occurs continuously between commands, thus notifying the processor which drives are on or off line. Each drive is polled every 1.024 ms except during the Read/Write commands.

μPD765A

FUNCTIONAL DESCRIPTION OF COMMANDS

READ DATA

A set of nine (9) byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Data Command may be terminated by the receipt of a Terminal Count signal. TC should be issued at the same time that the DACK for the last byte of data is sent. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminate the Read Data Command.
The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track), MF (MFM/FM), and N (Number of Bytes/Sector). Table 1 below shows the Transfer Capacity.

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskette
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

Table 1. Transfer Capacity

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector, is not sent to the Data Bus. The FDC reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to FF Hexidecimal.

At the completion of the Read Data Command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to a 1 (high), and if a CRC error occurs in the Data Field the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27 μs in the FM Mode, and every 13 μs in the MFM Mode, or the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID Information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 2 shows the values for C, H, R, and N, when the processor terminates the Command.

FUNCTIONAL DESCRIPTION OF COMMANDS (CONT.)

MT	HD	Final Sector Transferred to Processor	ID Information at Result Phase			
			C	H	R	N
0	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	C + 1	NC	R = 01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	C + 1	NC	R = 01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	NC	LSB	R = 01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	C + 1	LSB	R = 01	NC

Notes: 1 NC (No Change): The same value as the one at the beginning of command execution.

2 LSB (Least Significant Bit): The least significant bit of H is complemented.

WRITE DATA

A set of nine (9) bytes are required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified Head Settling Time (defined in the Specify Command), and begins reading ID Fields. When all four bytes loaded during the command (C, H, R, N) match the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus, and outputs it to the FDD.

After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written into. The FDC continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written then the remainder of the data field is filled with 00 (zeros).

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (incorrect CRC) in one of the ID Fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write Command operates in much the same manner as the Read Command. The following items are the same, and one should refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head Unload Time Interval
- ID Information when the processor terminates command (see Table 2)
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC, via the Data Bus, must occur every 27 μs if the FM mode, and every 13 μs in the MFM mode. If the time interval between data transfers is longer than this then the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bit 7 and 6 set to 0 and 1 respectively.)

WRITE DELETED DATA

This command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

READ DELETED DATA

This command is the same as the Read Data Command except that when the FDC detects a Data Address Mark at the beginning of a Data Field (and SK = 0 (low), it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address Mark and reads the next sector.

READ A TRACK

This command is similar to READ DATA Command except that this is a continuous READ operation where the entire data field from each of the sectors are read. Immediately after encountering the INDEX HOLE, the FDC starts reading all data fields on the track, as continuous blocks of data. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multi-track or skip operations are not allowed with this command.

This command terminates when number of sectors read is equal to EOT. If the FDC does not find an ID Address Mark on the diskette after it encounters the INDEX HOLE for the second time, then it sets the MA (missing address mark) flag in Status Register 1 to a 1 (high), and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

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FUNCTIONAL DESCRIPTION OF COMMANDS (CONT.)

READ ID

The READ ID Command is used to give the present position of the recording head. The FDC stores the values from the first ID Field it is able to read. If no proper ID Address Mark is found on the diskette, before the INDEX HOLE is encountered for the second time then the MA (Missing Address Mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high). The command is then terminated with Bits 7 and 6 in Status Register 0 set to 0 and 1 respectively. During this command there is no data transfer between FDC and the CPU except during the result phase.

FORMAT A TRACK

The Format Command allows an entire track to be formatted. After the INDEX HOLE is detected, Data is written on the Diskette: Gaps, Address Marks, ID Fields and Data Fields, all per the IBM System 34 (Double Density) or System 3740 (Single Density) Format are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (Gap Length), and D (Data Pattern) which are supplied by the processor during the Command Phase. The Data Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (Cylinder Number), H (Head Number), R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with non-sequential sector numbers, if desired.

The processor must send new values for C, H, R, and N to the μPD765 for each sector on the track. If FDC is set for DMA mode, it will issue 4 DMA requests per sector. If it is set for interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R and N load for each sector. The contents of the R register is incremented by one after each sector is formatted, thus, the R register contains a value of R when it is read during the Result Phase. This incrementing and formatting continues for the whole track until the FDC encounters the INDEX HOLE for the second time, whereupon it terminates the command.

If a FAULT signal is received from the FDD at the end of a write operation, then the FDC sets the EC flag of Status Register 0 to a 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also the loss of a READY signal at the beginning of a command execution phase causes bits 7 and 6 of Status Register 0 to be set to 0 and 1 respectively.

Table 3 shows the relationship between N, SC, and GPL for various sector sizes:

	8" STANDARD FLOPPY					5¼" MINI FLOPPY				
FORMAT	SECTOR SIZE	N	SC	GPL ①	GPL ②	SECTOR SIZE	N	SC	GPL ①	GPL ②
FM Mode	128 bytes/Sector	00	1A	07	1B	128 bytes/Sector	00	12	07	09
	256	01	0F	0E	2A	128	00	10	10	19
	512	02	08	1B	3A	256	01	08	18	30
	1024 bytes/Sector	03	04	47	8A	512	02	04	46	87
	2048	04	02	C8	FF	1024	03	02	C8	FF
	4096	05	01	C8	FF	2048	04	01	C8	FF
MFM Mode	256	01	1A	0E	36	256	01	12	0A	0C
	512	02	0F	1B	54	256	01	10	20	32
	1024	03	08	35	74	512	02	08	2A	50
	2048	04	04	99	FF	1024	03	04	80	F0
	4096	05	02	C8	FF	2048	04	02	C8	FF
	8192	06	01	C8	FF	4096	05	01	C8	FF

Table 3

Note: ① Suggested values of GPL in Read or Write Commands to avoid splice point between data field and ID field of contiguous sections.

② Suggested values of GPL in format command.

③ In MFM mode FDC can not perform a read/write/format operation with 128 bytes/sector. (N = 00)

④ All the values are hexidecimal.

SCAN COMMANDS

The SCAN Commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC compares the data on a byte-by-byte basis, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{Processor}$, $D_{FDD} < D_{Processor}$, or $D_{FDD} \geq D_{Processor}$. The hexidecimal byte of FF either from memory or from FDD can be used as a mask byte because it always meet the condition of the compare. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremental (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occur: the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

FUNCTIONAL DESCRIPTION OF COMMANDS (CONT.)

If the conditions for scan are met then the FDC sets the SH (Scan Hit) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. The receipt of a TERMINAL COUNT signal from the Processor or DMA Controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 4 shows the status of bits SH and SN under various conditions of SCAN.

COMMAND	STATUS REGISTER 2		COMMENTS
	BIT 2 = SN	BIT 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$
Scan Low or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} > D_{Processor}$
Scan High or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} > D_{Processor}$
	1	0	$D_{FDD} < D_{Processor}$

Table 4

If the FDC encounters a Deleted Data Address Mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address Mark, and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted Sector had been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02 sectors are read) or the MT (Multi-Track) are programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and we start the Scan Command at sector 21; the following will happen. Sectors 21, 23, and 25 will be read, then the next sector (26) will be skipped and the Index Hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan Command would be completed in a normal manner.

During the Scan Command data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Over Run) flag set in Status Register 1, it is necessary to have the data available in less than 27 μs (FM Mode) or 13 μs (MFM Mode). If an Overrun occurs the FDC ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

SEEK

The read/write head within the FDD is moved from cylinder to cylinder under control of the Seek Command. FDC has four independent Present Cylinder Registers for each drive. They are clear only after Recalibrate command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number), and if there is a difference performs the following operation:

PCN < NCN: Direction signal to FDD set to a 1 (high), and Step Pulses are issued. (Step In.)
PCN > NCN: Direction signal to FDD set to a 0 (low), and Step Pulses are issued. (Step Out.)

The rate at which Step Pulses are issued is controlled by SRT (Stepping Rate Time) in the SPECIFY Command. After each Step Pulse is issued NCN is compared against PCN, and when NCN = PCN, then the SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated. At this point FDC interrupt goes high. Bits DB_0-DB_3 in Main Status Register are set during seek operation and are cleared by Sense Interrupt Status command.

During the Command Phase of the Seek operation the FDC is in the FDC BUSY state, but during the Execution Phase it is in the NON BUSY state. While the FDC is in the NON BUSY state, another Seek Command may be issued, and in this manner parallel seek operations may be done on up to 4 Drives at once. No other command could be issued for as long as FDC is in process of sending Step Pulses to any drive.

If an FDD is in a NOT READY state at the beginning of the command execution phase or during the seek operation, then the NR (NOT READY) flag is set in Status Register 0 to a 1 (high), and the command is terminated after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

If the time to write 3 bytes of seek command exceeds 150 μs, the timing between first two Step Pulses may be shorter than set in the Specify command by as much as 1 ms.

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FUNCTIONAL DESCRIPTION OF COMMANDS (CONT.)

RECALIBRATE

The function of this command is to retract the read/write head within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 0 (low) and Step Pulses are issued. When the Track 0 signal goes high, the SE (SEEK END) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 Step Pulse have been issued, the FDC sets the SE (SEEK END) and EC (EQUIPMENT CHECK) flags of Status Register 0 to both 1s (highs), and terminates the command after bits 7 and 6 of Status Register 0 is set to 0 and 1 respectively.

The ability to do overlap RECALIBRATE Commands to multiple FDDs and the loss of the READY signal, as described in the SEEK Command, also applies to the RECALIBRATE Command.

SENSE INTERRUPT STATUS

An Interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data Command
   b. Read a Track Command
   c. Read ID Command
   d. Read Deleted Data Command
   e. Write Data Command
   f. Format a Cylinder Command
   g. Write Deleted Data Command
   h. Scan Commands
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate Command
4. During Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in NON-DMA Mode, DB5 in Main Status Register is high. Upon entering Result Phase this bit gets clear. Reason 1 and 4 does not require Sense Interrupt Status command. The interrupt is cleared by reading/writing data to FDC. Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status Command. This command when issued resets the interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

SEEK END BIT 5	INTERRUPT CODE		CAUSE
	BIT 6	BIT 7	
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate Command
1	1	0	Abnormal Termination of Seek or Recalibrate Command

Table 5

Neither the Seek or Recalibrate Command have a Result Phase. Therefore, it is mandatory to use the Sense Interrupt Status Command after these commands to effectively terminate them and to provide verification of where the head is positioned (PCN).

Issuing Sense Interrupt Status Command without interrupt pending is treated as an invalid command.

SPECIFY

The Specify Command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution Phase of one of the Read/Write Commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 = 32 ms . . . . OF = 240 ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and when the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms . . . 7F = 254 ms).

The time intervals mentioned above are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock, if the clock was reduced to 4 MHz (mini-floppy application) then all time intervals are increased by a factor of 2.

The choice of DMA or NON-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1) the NON-DMA mode is selected, and when ND = 0 the DMA mode is selected.

SENSE DRIVE STATUS

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information stored internally in FDC registers.

INVALID

If an invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of Status Register 0 are set to 1 and 0 respectively. No interrupt is generated by the μPD765 during this condition. Bit 6 and bit 7 (DIO and RQM) in the Main Status Register are both high ("1") indicating to the processor that the μPD765 is in the Result Phase and the contents of Status Register 0 (ST0) must be read. When the processor reads Status Register 0 it will find a 80 hex indicating an invalid command was received.

A Sense Interrupt Status Command must be sent after a Seek or Recalibrate Interrupt, otherwise the FDC will consider the next command to be an Invalid Command.

In some applications the user may wish to use this command as a No-Op command, to place the FDC in a standby or no operation state.

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STATUS REGISTER IDENTIFICATION

BIT NO.	BIT NAME	BIT SYMBOL	DESCRIPTION
STATUS REGISTER 0			
D_7	Interrupt Code	IC	$D_7 = 0$ and $D_6 = 0$ Normal Termination of Command, (NT). Command was completed and properly executed.
D_6			$D_7 = 0$ and $D_6 = 1$ Abnormal Termination of Command, (AT). Execution of Command was started, but was not successfully completed.
			$D_7 = 1$ and $D_6 = 0$ Invalid Command issue, (IC). Command which was issued was never started.
			$D_7 = 1$ and $D_6 = 1$ Abnormal Termination because during command execution the ready signal from FDD changed state.
D_5	Seek End	SE	When the FDC completes the SEEK Command, this flag is set to 1 (high).
D_4	Equipment Check	EC	If a fault Signal is received from the FDD, or if the Track 0 Signal fails to occur after 77 Step Pulses (Recalibrate Command) then this flag is set.
D_3	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single sided drive, then this flag is set.
D_2	Head Address	HD	This flag is used to indicate the state of the head at Interrupt.
D_1	Unit Select 1	US 1	These flags are used to indicate a Drive Unit. Number at Interrupt.
D_0	Unit Select 0	US 0	
STATUS REGISTER 1			
D_7	End of Cylinder	EN	When the FDC tries to access a Sector beyond the final Sector of a Cylinder, this flag is set.
D_6			Not used. This bit is always 0 (low).
D_5	Data Error	DE	When the FDC detects a CRC error in either the ID field or the data field, this flag is set.
D_4	Over Run	OR	If the FDC is not serviced by the main-systems during data transfers, within a certain time interval, this flag is set.
D_3			Not used. This bit always 0 (low).
D_2	No Data	ND	During execution of READ DATA, WRITE DELETED DATA or SCAN Command, if the FDC cannot find the Sector specified in the IDR Register, this flag is set.
			During executing the READ ID Command, if the FDC cannot read the ID field without an error, then this flag is set.
			During the execution of the READ A Cylinder Command, if the starting sector cannot be found, then this flag is set.

μPD765A

STATUS REGISTER IDENTIFICATION (CONT.)

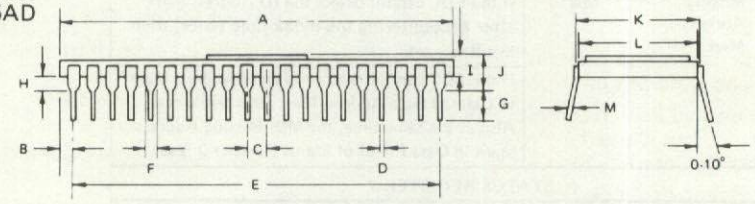
BIT NO.	BIT NAME	BIT SYMBOL	DESCRIPTION
		STATUS REGISTER 1 (CONT.)	
D_1	Not Writable	NW	During execution of WRITE DATA, WRITE DELETED DATA or Format A Cylinder Command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D_0	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set.
			If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in Data Field) of Status Register 2 is set.
		STATUS REGISTER 2	
D_7			Not used. This bit is always 0 (low).
D_6	Control Mark	CM	During executing the READ DATA or SCAN Command, if the FDC encounters a Sector which contains a Deleted Data Address Mark, this flag is set.
D_5	Data Error in Data Field	DD	If the FDC detects a CRC error in the data field then this flag is set.
D_4	Wrong Cylinder	WC	This bit is related with the ND bit, and when the contents of C on the medium is different from that stored in the IDR, this flag is set.
D_3	Scan Equal Hit	SH	During execution, the SCAN Command, if the condition of "equal" is satisfied, this flag is set.
D_2	Scan Not Satisfied	SN	During executing the SCAN Command, if the FDC cannot find a Sector on the cylinder which meets the condition, then this flag is set.
D_1	Bad Cylinder	BC	This bit is related with the ND bit, and when the content of C on the medium is different from that stored in the IDR and the content of C is FF, then this flag is set.
D_0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.
		STATUS REGISTER 3	
D_7	Fault	FT	This bit is used to indicate the status of the Fault signal from the FDD.
D_6	Write Protected	WP	This bit is used to indicate the status of the Write Protected signal from the FDD.
D_5	Ready	RY	This bit is used to indicate the status of the Ready signal from the FDD.
D_4	Track 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
D_3	Two Side	TS	This bit is used to indicate the status of the Two Side signal from the FDD.
D_2	Head Address	HD	This bit is used to indicate the status of Side Select signal to the FDD.
D_1	Unit Select 1	US 1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D_0	Unit Select 0	US 0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

It is suggested that you utilize the following applications notes:

① #8 – for an example of an actual interface, as well as a "theoretical" data separator.

② #10 – for a well documented example of a working phase lock loop.

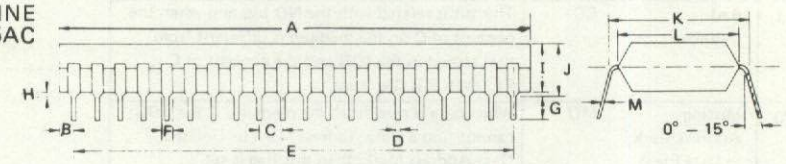
PACKAGE OUTLINE
μPD765AD



Ceramic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.03 MAX
B	1.62 MAX	0.06 MAX
C	2.54 ± 0.1	0.1 ± 0.004
D	0.5 ± 0.1	0.02 ± 0.004
E	48.26 ± 0.1	1.9 ± 0.004
F	1.02 MIN	0.04 MIN
G	3.2 MIN	0.13 MIN
H	1.0 MIN	0.04 MIN
I	3.5 MAX	0.14 MAX
J	4.5 MAX	0.18 MAX
K	15.24 TYP	0.6 TYP
L	14.93 TYP	0.59 TYP
M	0.25 ± 0.05	0.01 ± 0.0019

PACKAGE OUTLINE
μPD765AC



Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{0.05}$	$0.010^{+0.004}_{0.002}$

WESTERN DIGITAL
CORPORATION

WD8250 Asynchronous Communications Element

FEATURES

- Designed to be Easily Interfaced to Most Popular Microprocessors (Z-80, 8080A, 6800, etc.)
- Full Double Buffering
- Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts
- Programmable Baud Rate Generator Allows Division of Any Input Clock by 1 to (2^{16} - 1) and Generates the Internal 16x Clock
- Independent Receiver Clock Input
- Fully Programmable Serial-Interface Characteristics
  - —5-, 6-, 7-, or 8-Bit Characters
  - —Even, Odd, or No-Parity Bit Generation and Detection
  - —1-, 1½-, or 2-Stop Bit Generation
  - —Baud Rate Generation (DC to 56K Baud)
- False Start Bit Detector
- Complete Status Reporting Capabilities
- THREE-STATE TTL Drive Capabilities for Bi-directional Data Bus and Control Bus
- Line Break Generation and Detection
- Internal Diagnostic Capabilities
  - —Loopback Controls for Communications Link Fault Isolation
  - —Break, Parity, Overrun, Framing Error Simulation
- Full Prioritized Interrupt System Controls
- Single +5-Volt Power Supply

GENERAL DESCRIPTION

The WD8250 is a programmable Asynchronous Communication Element (ACE) in a 40-pin package. The device is fabricated in N/MOS silicon gate technology.

The ACE is a software-oriented device using a three-state 8-bit bi-directional data bus.

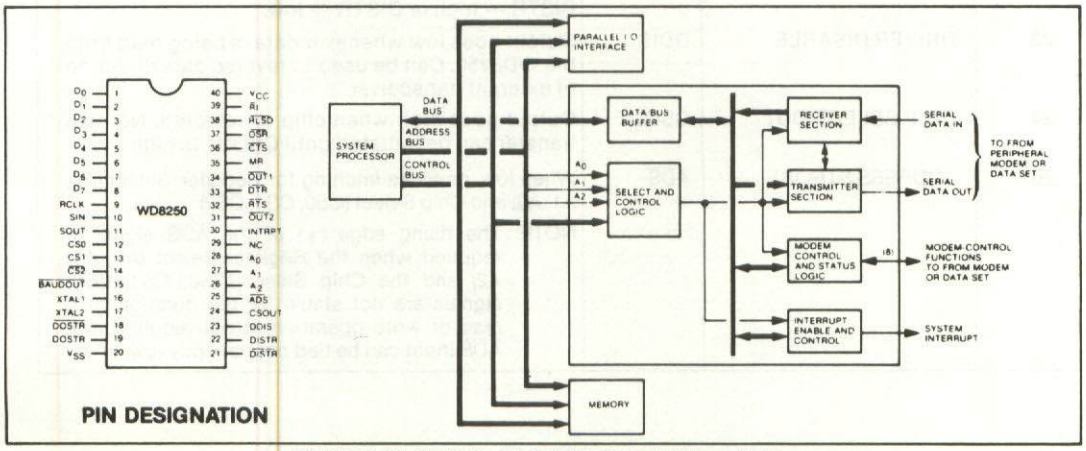
The ACE is used to convert parallel data to a serial format on the transmit side, and convert serial data to parallel on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and one half (five bit format only) or two stop bits. The maximum recommended data rate is 56K baud.

Internal registers enable the user to program various types of interrupts, modem controls, and character formats. The user can read the status of the ACE at any time monitoring word conditions, interrupts and modem status.

An additional feature of the ACE is a programmable baud rate generator that is capable of dividing an internal XTAL or TTL signal clock by a division of 1 to 2^{16} – 1.

The ACE is designed to work in either a polling or interrupt driven system, which is programmable by users software controlling an internal register.

PIN DESIGNATION



WD8250 GENERAL SYSTEM CONFIGURATION

PIN DEFINITIONS

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1-8	DATA BUS	D0-D7	3-state input/output lines. Bi-directional communication lines between WD8250 and Data Bus. All assembled data TX and RX, control words, and status information are transferred via the D0-D7 data bus.
9	RECEIVE CLK.	RCLK	This input is the 16X baud rate clock for the receiver section of the chip (may be tied to BAUDOUT pin 15).
10	SERIAL INPUT	SIN	Received Serial Data In from the communications link (Peripheral device, modem or data set).
11	SERIAL OUTPUT	SOUT	Transmitted Serial Data Out to the communication link. The SOUT signal is set to a (logic 1) marking condition upon a MASTER RESET.
12 13 14	CHIP SELECT CHIP SELECT CHIP SELECT	CS0 CS1 $\overline{CS2}$	When CS0 and CS1 are high, and $\overline{CS2}$ is low, chip is selected. Selection is complete when the address strobe $\overline{ADS}$ latches the chip select signals.
15	BAUDOUT	$\overline{BAUDOUT}$	16X clock signal for the transmitter section of the WD8250. The clock rate is equal to the oscillator frequency divided by the divisor loaded into the divisor latches. The BAUDOUT signal may be used to clock the receiver by tying to (pin 9) RCLK.
16 17	EXTERNAL CLOCK IN EXTERNAL CLOCK OUT	XTAL 1 XTAL 2	These pins connect the crystal or signal clock to the WD8250 baud rate divisor circuit. See Fig. 3 and Fig. 4 for circuit connection diagrams.
18 19	DATA OUT STROBE DATA OUT STROBE	$\overline{DOSTR}$ DOSTR	When the chip has been selected, a low $\overline{DOSTR}$ or high DOSTR will latch data into the selected WD8250 register (a CPU write). Only one of these lines need be used. Tie unused line to its inactive state. $\overline{DOSTR}$ — high or DOSTR — low.
20	GROUND	V_{SS}	System signal ground.
21 22	DATA IN STROBE DATA IN STROBE	$\overline{DISTR}$ DISTR	When chip has been selected, a low $\overline{DISTR}$ or high DISTR will allow a read of the selected WD8250 register (a CPU read). Only one of these lines need be used. Tie unused line to its inactive state. $\overline{DISTR}$ — high or DISTR — low.
23	DRIVER DISABLE	DDIS	Output goes low whenever data is being read from the WD8250. Can be used to reverse data direction of external transceiver.
24	CHIP SELECT OUT	CSOUT	Output goes high when chip is selected. No data transfer can be initiated until CSOUT is high.
25	ADDRESS STROBE	$\overline{ADS}$	When low, provides latching for Register Select (A0, A1, A2) and Chip Select (CS0, CS1, $\overline{CS2}$) NOTE: The rising edge (↓) of the $\overline{ADS}$ signal is required when the Register Select (A0, A1, A2) and the Chip Select (CS0, CS1, $\overline{CS2}$) signals are not stable for the duration of a read or write operation. If not required, the $\overline{ADS}$ input can be tied permanently low.

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
26 27 28	REGISTER SELECT A2 REGISTER SELECT A1 REGISTER SELECT A0	A2 A1 A0	These three inputs are used to select a WD8250 internal register during a data read or write. See Table below.
29	NO CONNECT	NC	No Connect
30	INTERRUPT	INTRPT	Output goes high whenever an enabled interrupt is pending.
31	OUTPUT 2	$\overline{OUT2}$	User-designated output that can be programmed by Bit 3 of the modem control register = 1, causes $\overline{OUT2}$ to go low.
32	REQUEST TO SEND	$\overline{RTS}$	Output when low informs the modem or data set that the WD8250 is ready to transmit data. See Modem Control Register.
33	DATA TERMINAL READY	$\overline{DTR}$	Output when low informs the modem or data set that the WD8250 is ready to communicate.
34	OUTPUT 1	$\overline{OUT1}$	User designated output can be programmed by Bit 2 of Modem Control Register = 1 causes $\overline{OUT1}$ to go low.
35	MASTER RESET	MR	When high clears the registers to states as indicated in Table 1.
36	CLEAR TO SEND	$\overline{CTS}$	Input from DCE indicating remote device is ready to transmit. See Modem Control Register.
37	DATA SET READY	$\overline{DSR}$	Input from DCE used to indicate the status of the local data set. See Modem Control Register.
38	RECEIVED LINE SIGNAL DETECT	$\overline{RSLD}$	Input from DCE indicating that it is receiving a signal which meets its signal quality conditions. See Modem Control Register.
39	RING INDICATOR	$\overline{RI}$	Input, when low, indicates that a ringing signal is being received by the modem or data set. See Modem Control Register.
40	+5V	V_{CC}	+5 Volt Supply.

CHIP SELECTION AND REGISTER ADDRESSING

Address Strobe (ADS pin 25): When low provides latching for register select (A0, A1, A2) and chip select ($\overline{CS0}$, CS1, $\overline{CS2}$).

NOTE: The rising edge (↓) of the $\overline{ADS}$ input is required when Register Select (A0, A1, A2) and Chip Select ($\overline{CS0}$, CS1, $\overline{CS2}$) signals are not stable for the duration of a read or write operation. If $\overline{ADS}$ is not required for latching, this input can be tied permanently low.

Chip Select ($\overline{CS0}$, CS1, $\overline{CS2}$) pins 12-14: The definition of chip selected is $\overline{CS0}$, CS1 both high and $\overline{CS2}$ is low. Chip selection is complete when latched by $\overline{ADS}$ or $\overline{ADS}$ is tied low.

Register Select (A0, A1, A2) pins 26-28: To select a register for read or write operation, see Register Table.

NOTE: (DLAB) Divisor Latch access bit is the MSB of the Line Control Register. DLAB must be programmed high logic 1 by the system software to access the Baud Rate Generator Divisor Latches.

DLAB	A2	A1	A0	Register
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	None
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

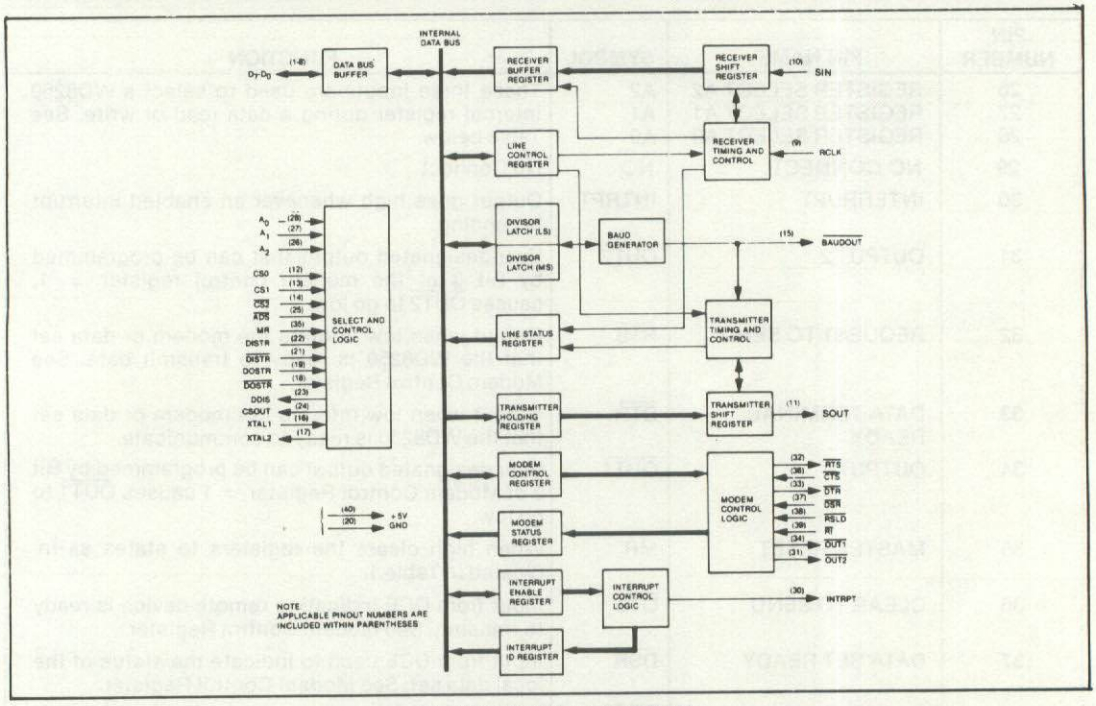
WD8250 OPERATIONAL DESCRIPTION

Master Reset

A high-level input on pin 35 causes the WD8250 to reset to the condition listed in Table 1.

WD8250 Accessible Registers

The system programmer has access to any of the registers summarized in Table 2. For individual register descriptions, refer to the following pages under register heading.



WD8250 BLOCK DIAGRAM

Table 1. Reset Control of Registers and Pinout Signals

Register/Signal	Reset Control	Reset State
Receiver Buffer Register	First Word Received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Master Reset	All Bits Low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High and Bits 1-7 Are Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, Except Bits 5 and 6 Are High
Modem Status Register	Master Reset MODEM Signal Inputs	Bits 0-3 Low Bits 4-7 — Input Signal
Divisor Latch (low order bits)	Writing into the Latch	Data
Divisor Latch (high order bits)	Writing into the Latch	Data
SOUT	Master Reset	High
$\overline{\text{BAUDOUT}}$	Writing into either Divisor Latch	Low
CSOUT	$\overline{\text{ADS}}$ Strobe Signal and State of Chip Select Lines	High/Low
DDIS	DDIS = $\overline{\text{CSOUT}} \cdot \text{RCLK} \cdot \overline{\text{DISTR}}$ (At Master Reset, the CPU sets RCLK and DISTR low.)	High
INTRPT	Master Reset	Low

$\overline{OUT\ 2}$	Master Reset	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
$\overline{OUT\ 1}$	Master Reset	High
D7-D0 Data Bus Lines	In THREE-STATE Mode, Unless CSOUT • DISTR = High or CSOUT • DOSTR = High	THREE-STATE Data (ACE to CPU) Data (CPU to ACE)

Table 2. Summary of WD8250 Accessible Registers

	Register Address									
	0 DLAB=0	0 DLAB=0	1DLAB=0	2	3	4	5	6	0DLAB=1	1DLAB=1
Bit No.	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Identification Register	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Divisor Latch (LS)	Divisor Latch (MS)
0	Data Bit 0*	Data Bit 0*	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	Word Length Select Bit 1 WLS1)	Request to Send (RTS)	Overrun Error (OR)	Delta Data Set Ready (DDSR)	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Receive Line Signal Detect (DSLSD)	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Shift Register Empty (TSRE)	Ring Indicator (RI)	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Received Line Signal Detect (RLSD)	Bit 7	Bit 15

*Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Line Control Register

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of stop bits in each transmitted or received serial character. If bit 2 is a logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, 1½ Stop bits are generated or checked. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, 2 Stop bits are generated or checked.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state and remains there (until reset by a low-level bit 6) regardless of other transmitter activity. The feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

WD8250 Programmable Baud Rate Generator

The WD8250 contains a programmable Baud Rate Generator that is capable of taking any clock input (DC to 3.1 MHz) and dividing it by any divisor from 1 to $(2^{16} - 1)$. The output frequency of the Baud Generator is 16x the Baud rate. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 3 and 4 illustrate the use of the Baud Generator with two different driving frequencies. One is referenced to a 1.8432 MHz crystal. The other is a 3.072 MHz crystal.

NOTE

The maximum operating frequency of the Baud Generator is 3.1 MHz. However, when using divisors of 6 and below, the maximum frequency is equal to 1/2 the divisor in MHz. For example, if the divisor is 1, then the maximum frequency is 1/2 MHz. In no case should the data rate be greater than 56K Baud.

Line Status Register

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of

Table 3. Baud Rates Using 1.8432 MHz Crystal.

Desired Baud Rate	Divisor Used to Generate 16x Clock	Percent Error Difference Between Desired and Actual
50	2304	—
75	1536	—
110	1047	0.026
134.5	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.86

NOTE: 1.8432 MHz is the standard 8080 frequency divided by 10.

Table 4. Baud Rates Using 3.072 MHz Crystal.

Desired Baud Rate	Divisor Used to Generate 16x Clock	Percent Error Difference Between Desired and Actual
50	3840	—
75	2560	—
110	1745	0.026
134.5	1428	0.034
150	1280	—
300	640	—
600	320	—
1200	160	—
1800	107	—
2000	96	—
2400	80	—
3600	53	0.628
4800	40	—
7200	27	1.23
9600	20	—
19200	10	—
38400	5	—
56000	3	14.285

the Line Status Register are indicated in table 2 and are described below.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 will be reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register or by writing a logic 0 into it from the CPU.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level).

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (Logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits).

NOTE

Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the WD8250 is ready to accept a new character for transmission. In addition, this bit causes the WD8250 to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Shift Register Empty (TSRE) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Shift Register is idle. It is reset to logic 0 upon a data transfer from the Transmitter Holding Register to the Transmitter Shift Register. Bit 6 is a read-only bit.

Bit 7: This bit is permanently set to logic 0.

Interrupt Identification Register

The WD8250 has an on chip interrupt capability that allows for complete flexibility in interfacing to all popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the WD8250 prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and source of that interrupt are stored in the Interrupt Identification Register (refer to table 5). The Interrupt Identification Register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in table 2 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in table 5.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Interrupt Enable Register

This 8-bit register enables the four interrupt sources of the WD8250 to separately activate the chip Interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are indicated in table 2 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to a logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Table 5. Interrupt Control Functions.

Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

MODEM Control Register

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in table 2 and are described below.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

NOTE

The $\overline{DTR}$ output of the WD8250 may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 ($\overline{OUT\ 1}$) signal, which is an auxiliary user-designated output. Bit 2 affects the $\overline{OUT\ 1}$ output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 ($\overline{OUT\ 2}$) signal, which is an auxiliary user-designated output. Bit 3 affects the $\overline{OUT\ 2}$ output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a loopback feature for diagnostic testing of the WD8250. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to a logic one (high) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control Inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$, and $\overline{RI}$) are disconnected; and the four MODEM Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT\ 1}$, and $\overline{OUT\ 2}$) are internally connected to the four MODEM Control Inputs. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the WD8250.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

The WD8250 interrupt system can be tested by writing into the lower six bits of the Line Status Register

and the lower four bits of the MODEM Status Register. Setting any of these bits to a logic 1 generates the appropriate interrupt (if enabled). The resetting of these interrupts is the same as in normal WD8250 operation. To return to this operation, the registers must be reprogrammed for normal operation and then bit 4 must be reset to logic 0.

Bits 5 through 7: These bits are permanently set to logic 0.

MODEM Status Register

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in table 2 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the $\overline{RLSD}$ input to the chip has changed state.

NOTE

Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input.

Bit 7: This bit is the complement of the Received Line Signal Detect ($\overline{RLSD}$) input.

Typical Applications

Figures 1 and 2 show how to use the WD8250 chip in an 8080A system and in a microcomputer system with a high-capacity data bus.

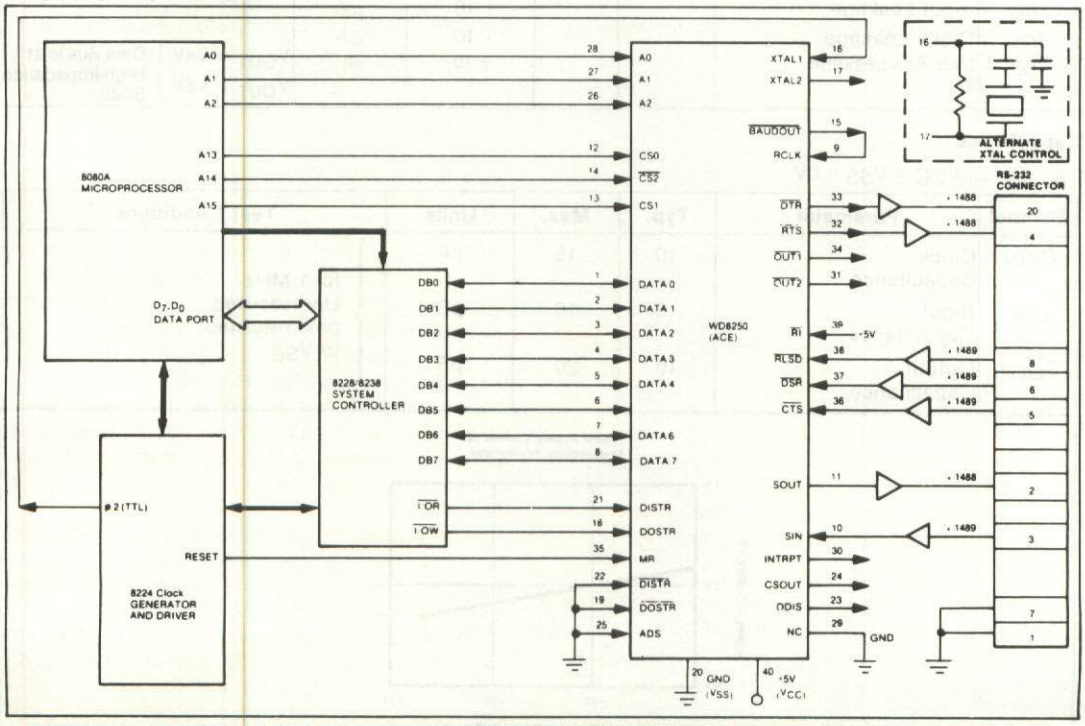


FIGURE 1. TYPICAL 8-BIT MICROPROCESSOR/RS-232 TERMINAL INTERFACE USING THE ACE.

Typical Applications (continued)

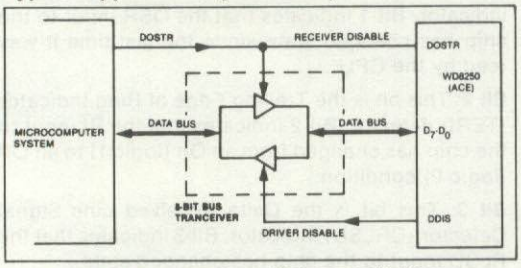


FIGURE 2. TYPICAL INTERFACE FOR A HIGH-CAPACITY DATA BUS.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... 0°C to +70°C
Storage Temperature -65°C to +150°C (Ceramic)
-50°C to +125°C (Plastic)
All Input or Output Voltages with
Respect to V_{SS} ..... -0.5 V to +7.0 V
Power Dissipation ..... 750 mW

Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.

DC Electrical Characteristics

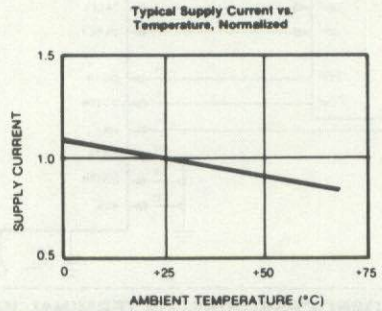
T_A = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{SS} = 0V, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V_{ILX}	Clock Input Low Voltage	-0.5		0.8	V	
V_{IHX}	Clock Input High Voltage	2.4		V_{CC}	V	
V_{IL}	Input Low Voltage	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.4		V_{CC}	V	
V_{OL}	Output Low Voltage			.45	V	I_{OL}=1.6mA on all outputs
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-100 μA
$I_{CC(AV)}$	Avg Power Supply Current (V_{CC})			150	ma	
I_{IL}	Input Leakage			± 10	μA	
I_{CL}	Clock Leakage			± 10	μA	
I_{DL}	Data Bus Leakage			± 10	μA	V_{OUT} = 0.4V, V_{OUT} = 4.6V: Data Bus is at High-Impedance State

Capacitance

T_A = 25°C, V_{CC} = V_{SS} = 0V

Symbol	Parameter	Typ.	Max.	Units	Test Conditions
C_{XIN}	Clock Capacitance	10	15	pF	fc=1 MHz, Unmeasured pins returned to V_{SS}
C_{IN}	Input Capacitance	6	10	pF	
C_{OUT}	Output Capacitance	10	20	pF	

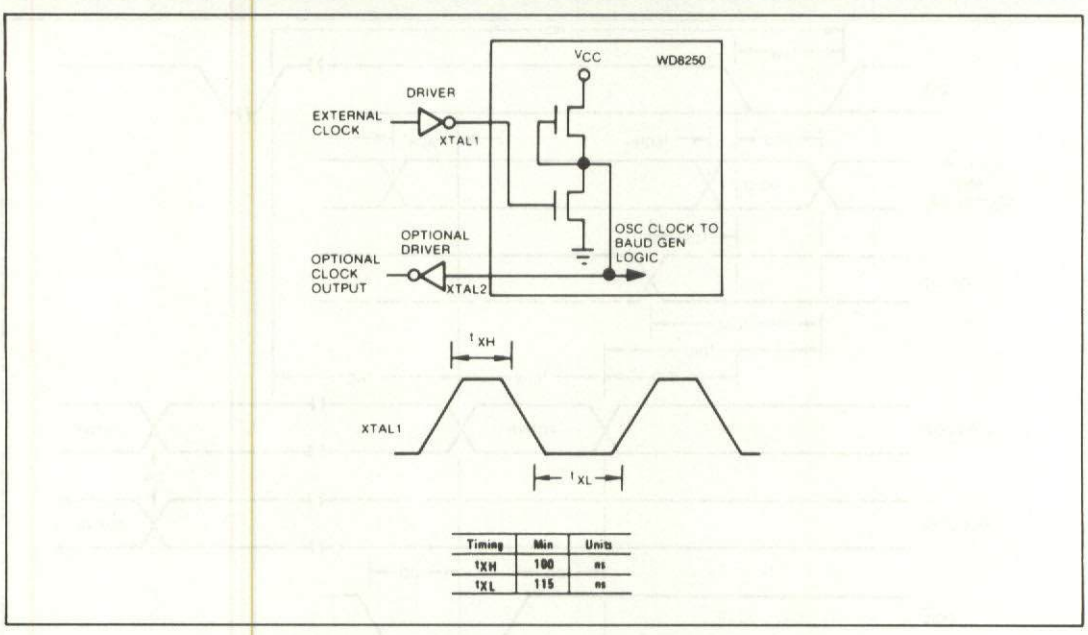


AC Electrical Characteristic TA = 0°C to +70°C. V_{CC} = +5V ± 5%

Symbol	Parameter	Units	Test Conditions Min	Max	
t_{AW}	Address Strobe Width	ns	120		1TTL Load
t_{ACS}	Address and Chip Select Setup Time	ns	100		1TTL Load
t_{ACH}	Address and Chip Select Hold Time	ns	10		1TTL Load
t_{CSS}	CSOUT Delay from Latch	ns		160	1TTL Load
t_{DID}	$\overline{DISTR}$/DISTR Delay from Latch	ns	50		1TTL Load
t_{DIW}	$\overline{DISTR}$/DISTR Strobe Width	ns	300		1TTL Load
t_{RC}	Read Cycle Delay	ns	655		1TTL Load
RC	Read Cycle = $t_{ACS} + t_{DID} + t_{DIW} + t_{RC}$ + 20 ns	ns	1125		1TTL Load
t_{DD}	$\overline{DISTR}$/DISTR to Driver Disable Delay	ns		200	1TTL Load
t_{DDD}	Delay from $\overline{DISTR}$/DISTR to Data	ns		300	1TTL Load
t_{HZ}	$\overline{DISTR}$/DISTR to Floating Data Delay	ns	60		1TTL Load
t_{DOD}	$\overline{DOSTR}$/DOSTR Delay From Latch	ns	20		1TTL Load
t_{DOW}	$\overline{DOSTR}$/DOSTR Strobe Width	ns	175		1TTL Load
t_{WC}	Write Cycle Delay	ns	685		1TTL Load
WC	Write Cycle = $t_{ACS} + t_{DOD} + t_{DOW} + t_{WC}$ + 20 ns	ns	1000		1TTL Load
t_{DS}	Data Setup Time	ns	175		1TTL Load
t_{DH}	Data Hold Time	ns	60		1TTL Load
t_{CSC}*	CSOUT Delay from Select	ns		260	1TTL Load
t_{DIC}*	$\overline{DISTR}$/DISTR Delay from Select	ns	150		1TTL Load
t_{DOC}*	$\overline{DOSTR}$/DOSTR Delay from Select	ns	150		1TTL Load
t_{ACR}*	Address and Chip Select Hold Time from $\overline{DISTR}$/DISTR	ns	10		1TTL Load
t_{ACW}*	Address and Chip Select Hold Time fom $\overline{DOSTR}$/DOSTR	ns	10		1TTL Load
t_{MR}	Master Reset Pulse Width	ns	500		1TTL Load

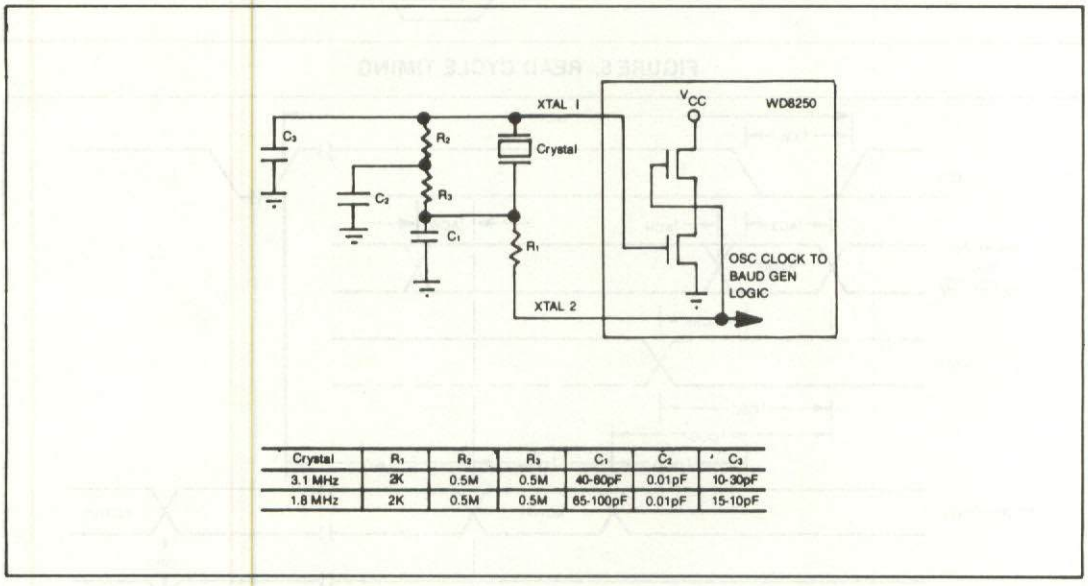
*Only applicable when ADS is permanently low.

Symbol	Parameter	Min.	Max.	Units	Test Conditions
Baud Generator					
N	Baud Rate Divisor	1	$2^{16}-1$		
t_{BLD}	Baud Output Negative Edge Delay		250	ns	100pF Load
t_{BHD}	Baud Output Positive Edge Delay		250	ns	100pF Load
t_{LW}	Baud Output Down Time	425		ns	100pF Load
t_{HW}	Baud Output Up Time	330		ns	100pF Load
Receiver					
t_{SCD}	Delay from RCLK to Sample Time		2	μs	
t_{SINT}	Delay from Stop to Set Interrupt		2	μs	100pF Load
t_{RINT}	Delay from $\overline{DISTR}$/DISTR (RD RBR) to Reset Interrupt	.250	1	μs	100pF Load
Transmitter					
t_{HR}	Delay from $\overline{DOSTR}$/DOSTR (WR THR) to Reset Interrupt	.250	1	μs	100pF Load
t_{IRS}	Delay from Initial INTR Reset to Transmit Start		16	$\overline{BAUDOUT}$ Cycles	
t_{SI}	Delay from Initial Write to Interrupt		24	$\overline{BAUDOUT}$ Cycles	
t_{SS}	Delay from Stop to Next Start	.250	1	μs	
t_{STI}	Delay from Stop to Interrupt (THRE)		8	$\overline{BAUDOUT}$ Cycles	
T_{IR}	Delay from $\overline{DISTR}$/DISTR (RD IIR) to Reset Interrupt (THRE)	.250	1	μs	100pF Load
Modem Control					
t_{MDO}	Delay from DOSTR/$\overline{DOSTR}$ (WR MCR) to Output	.250	1	μs	100pF Load
t_{SIM}	Delay to Set Interrupt from MODEM Input	.250	1	μs	100pF Load
t_{RIM}	Delay to Reset Interrupt from $\overline{DISTR}$/DISTR (RD MSR)	.250	1	μs	100pF Load



Timing	Min	Units
tXH	100	ns
tXL	115	ns

FIGURE 3. EXTERNAL CLOCK INPUT (3.1 MHz MAX.)



Crystal	R_1	R_2	R_3	C_1	C_2	C_3
3.1 MHz	2K	0.5M	0.5M	40-60pF	0.01pF	10-30pF
1.8 MHz	2K	0.5M	0.5M	65-100pF	0.01pF	15-10pF

FIGURE 4. TYPICAL CRYSTAL OSCILLATOR NETWORK

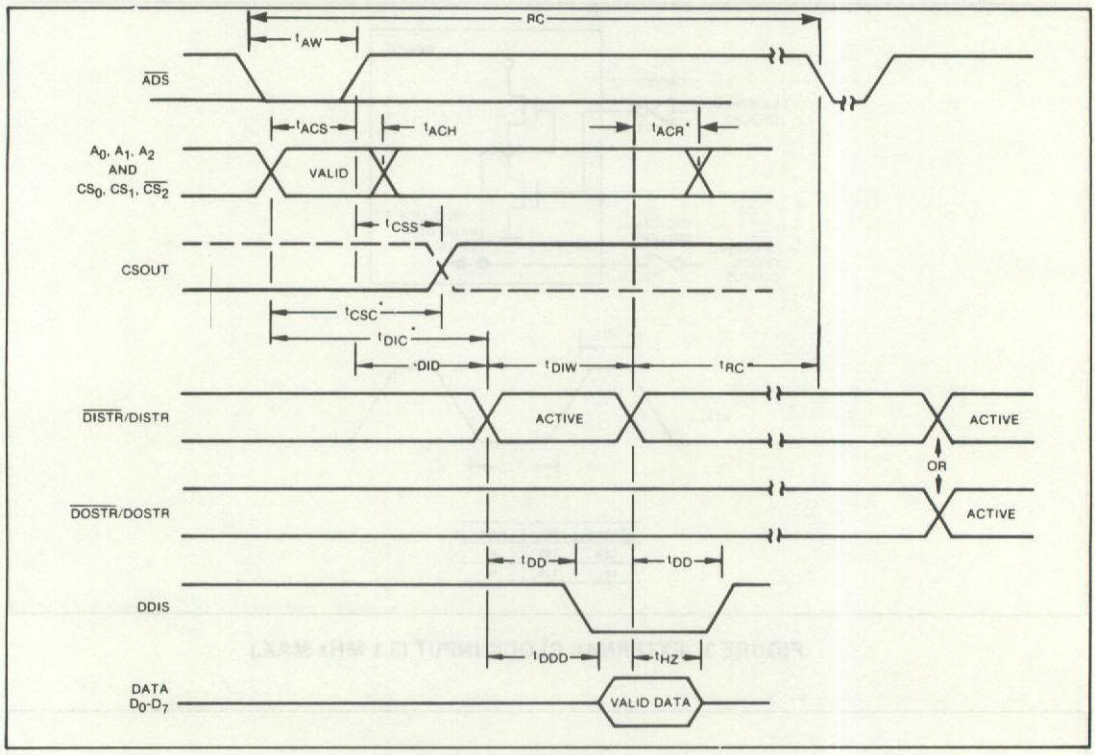


FIGURE 5. READ CYCLE TIMING

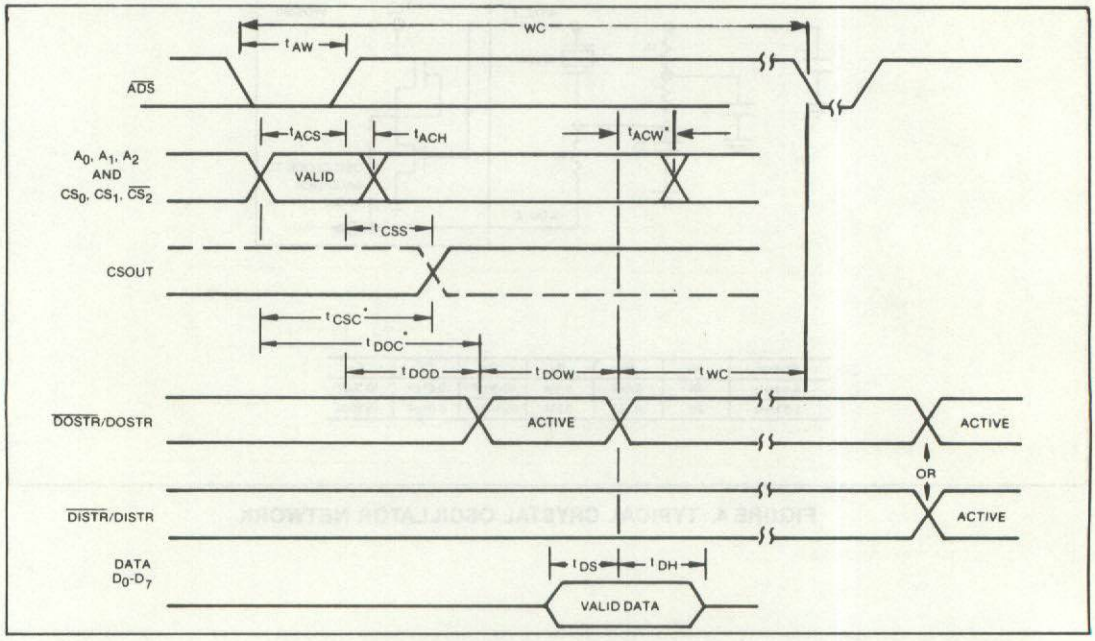


FIGURE 6. WRITE CYCLE TIMING

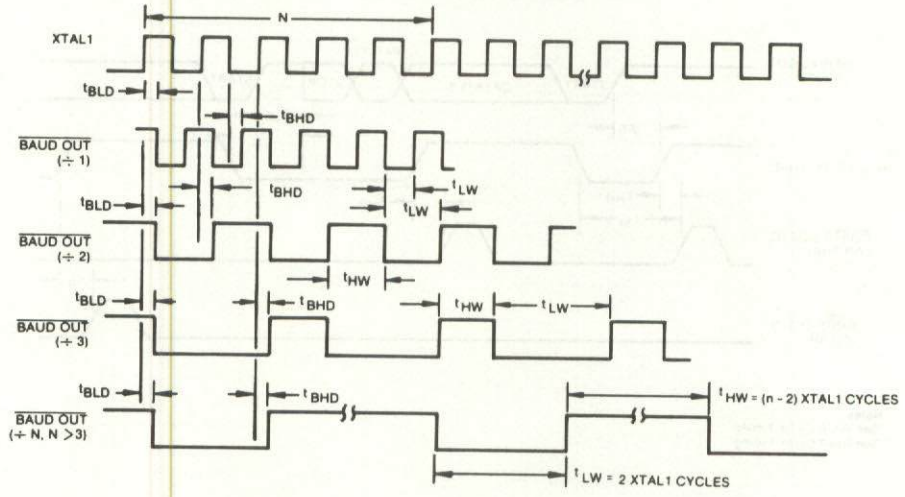


FIGURE 7. BAUDOUT TIMING

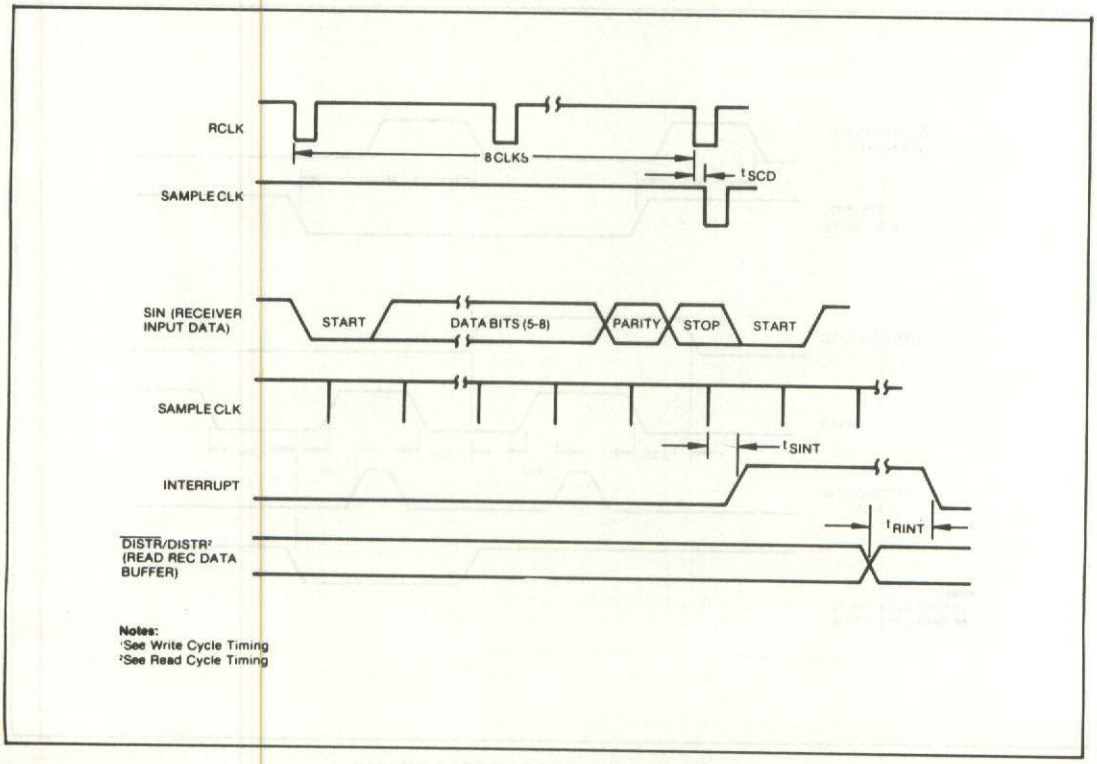


FIGURE 8. RECEIVER TIMING

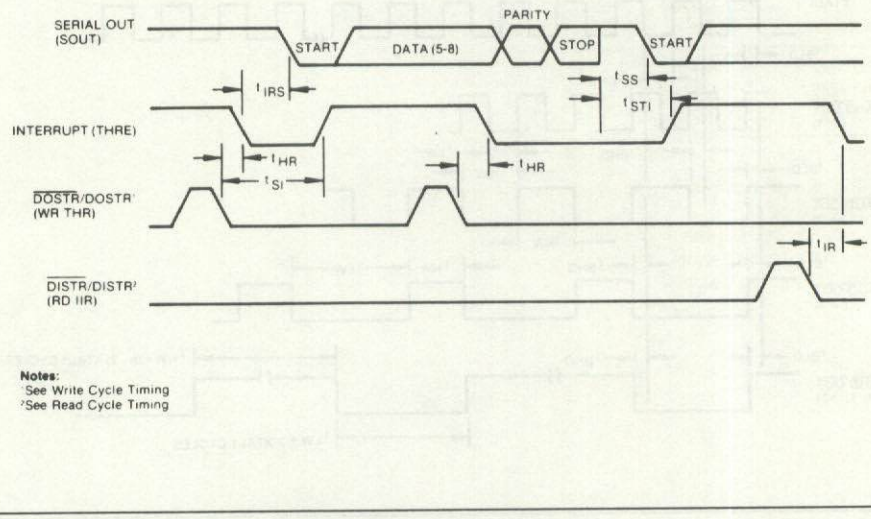


FIGURE 9. TRANSMITTER TIMING

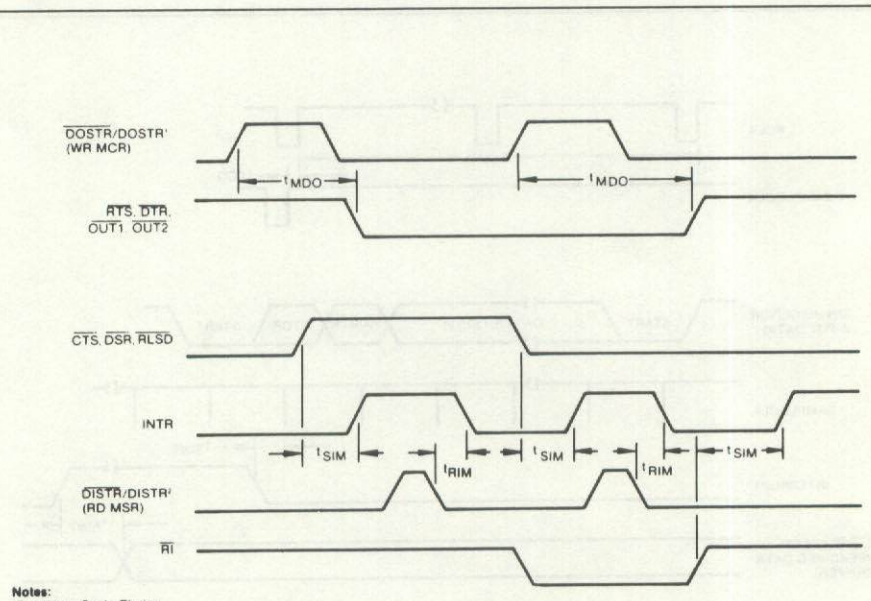


FIGURE 10. MODEM CONTROLS TIMING

ORDERING INFORMATION

Part Number	Max Clock Rate[1]	Bits/Character
WD8250*-00	3.1 MHz	5, 6, 7, 8
WD8250*-20	3.1 MHz	6, 7, 8
WD8250*-30	500 kHz	5, 6, 7, 8

NOTES:

1. This is the maximum clock rate that can be applied to pins 16 or 17.

* Consult your local Western Digital Sales Representative for information regarding package availability, price, and delivery.

See page 429 for ordering information.

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WESTERN DIGITAL
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WD1691 FLOPPY SUPPORT LOGIC (F.S.L.)

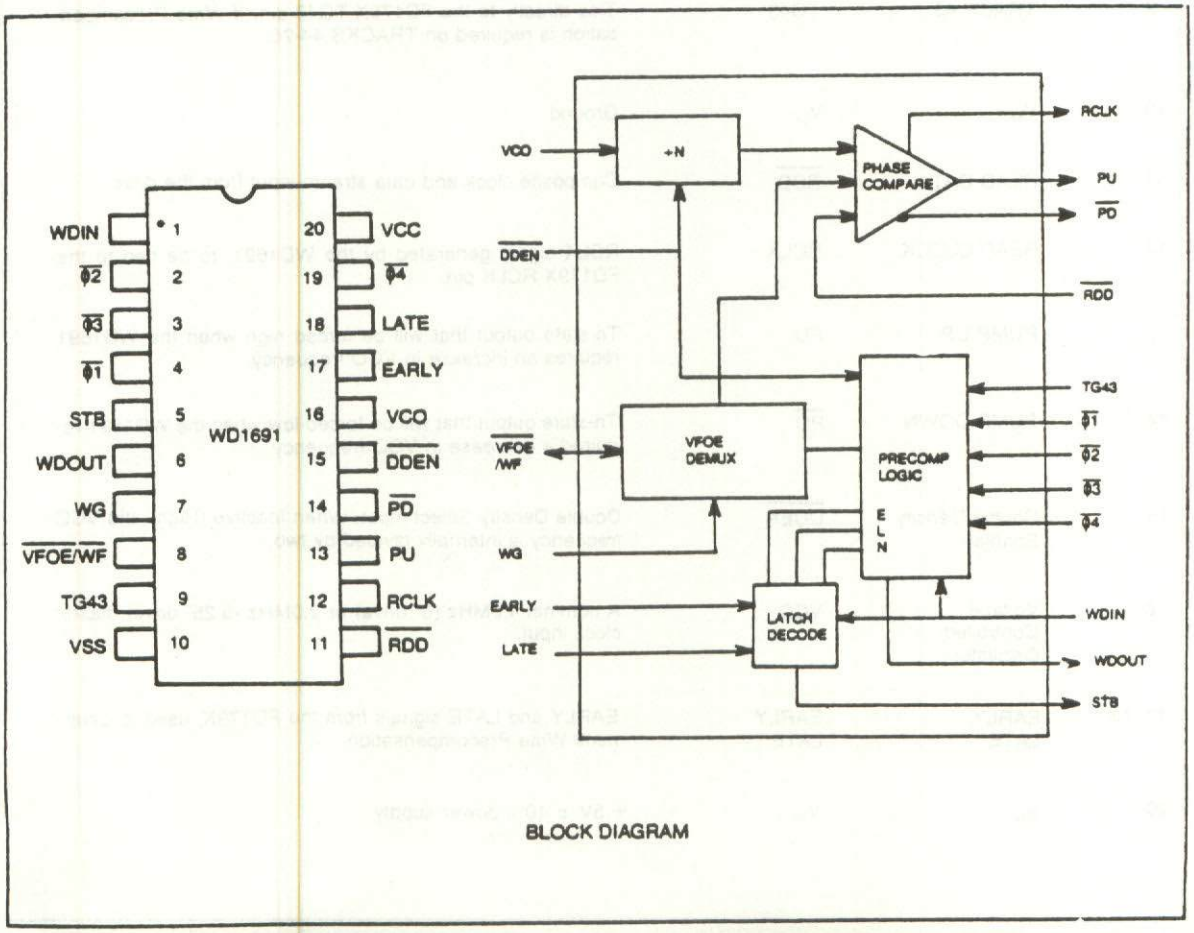
FEATURES

- Direct interface to the FD179X
- Eliminates external FDC Logic
- Data Separation/RCLK GENERATION
- Write Precompensation Signals
- VFOE/WF Demultiplexing
- Programmable Density
- 8" or 5.25" Drive Compatible
- All inputs and outputs TTL Compatible
- Single +5V Supply

GENERAL DESCRIPTION

The WD1691 F.S.L. has been designed to minimize the external logic required to interface the 179X Family of Floppy Disk Controllers to a drive. With the use of an external VCO, the WD 1691 will generate the RCLK signal for the WD179X, while providing an adjustment pulse (PUMP) to control the VCO frequency. VFOE/WF de-multiplexing is also accomplished and Write Precompensation signals have been included to interface directly with the WD2143 Clock Generator.

The WD1691 is implemented in N-MOS silicon gate technology and is available in a plastic or ceramic 20 pin dual-in-line package.



BLOCK DIAGRAM

PIN	NAME	SYMBOL	FUNCTION
1	WRITE DATA INPUT	WDIN	Ties directly to the FD179X WD pin.
2, 3, 4, 19	PHASE 2, 3, 1, 4	$\overline{\phi 2}$ $\overline{\phi 3}$ $\overline{\phi 1}$ $\overline{\phi 4}$	4 Phase inputs to generate a desired Write Precompensation delay. These signals tie directly to the WD2143 Clock Generator.
5	STROBE	STB	Strobe output from the 1691. Strobe will latch at a high level on the leading edge of WDIN and reset to a low level on the leading edge of 04.
6	WRITE DATA OUTPUT	WDOUT	Serial, pre-compensated Write data stream to be sent to the disk drive's WD line.
7	WRITE GATE	WG	Ties directly to the FD179X WG pin.
8	VFO ENABLE/ WRITE FAULT	$\overline{\text{VFOE}}/\overline{\text{WF}}$	Ties directly to the FD179X $\overline{\text{VFOE}}/\overline{\text{WF}}$ pin.
9	TRACK 43	TG43	Ties directly to the FD179X TG43 pin, If Write Precompensation is required on TRACKS 44-76.
10	V_{ss}	V_{ss}	Ground
11	READ DATA	$\overline{\text{RDD}}$	Composite clock and data stream input from the drive.
12	READ CLOCK	RCLK	RCLK signal generated by the WD1691, to be tied to the FD179X RCLK pin.
13	PUMP UP	PU	Tri-state output that will be forced high when the WD1691 requires an increase in VCO frequency.
14	PUMP DOWN	$\overline{\text{PD}}$	Tri-state output that will be forced low when the WD1691 required a decrease in VCO frequency.
15	Double Density Enable	$\overline{\text{DDEN}}$	Double Density Select input. When Inactive (High), the VCO frequency is internally divided by two.
16	Voltage Controlled Oscillator	VCO	A nominal 4.0MHz (8" drive) or 2.0MHz (5.25" drive) master clock input.
17, 18	EARLY LATE	EARLY LATE	EARLY and LATE signals from the FD179X, used to determine Write Precompensation.
20	V_{cc}	V_{cc}	+ 5V ± 10% power supply

DEVICE DESCRIPTION

The WD1691 is divided into two sections:

1) Data Recovery Circuit
2) Write precompensation Circuit

The Data Separator or Recovery Circuit has four inputs: $\overline{DDEN}$, VCO, $\overline{RDD}$, and $\overline{VFOE/WF}$; and three outputs: PU, $\overline{PD}$ and RCLK. The $\overline{VFOE/WF}$ input is used in conjunction with the Write Gate signal to enable the Data recovery circuit. When Write Gate is high, a write operation is taking place, and the data recovery circuits are disabled, regardless of the state on any other inputs.

When $\overline{VFOE/WF}$ and WRITE GATE are low, the data recovery circuit is enabled. When the $\overline{RDD}$ line goes Active Low, the PU or $\overline{PD}$ signals will become active. If the $\overline{RDD}$ line has made its transition in the beginning of the RCLK window, PU will go from a HI-Z state to a Logic I, requesting an *increase* in VCO frequency. If the $\overline{RDD}$ line has made its transition at the end of the RCLK window, PU will remain in a HI-Z state while PD will go to a logic zero, requesting a *decrease* in VCO frequency. When the leading edge of $\overline{RDD}$ occurs in the center of the RCLK window, both PU and $\overline{PD}$ will remain tri-stated, indicating that no adjustment of the VCO frequency is needed. The RCLK signal is a divide-by-16 (DDEN=1) or a divide-by-8 (DDEN=0) of the VCO frequency.

WG	VFOE/WF	RDD	PU+PD
1	X	X	HI-Z
0	1	X	HI-Z
0	0	1	HI-Z
0	0	0	Enable

The Write Precompensation circuit has been designed to be used with the WD2143-01 clock generator. When the WD1691 is operated in a "single density only" mode, write precompensation as well as the WD2143-01 is not needed. In this case, $\overline{\phi 1}$, $\overline{\phi 2}$, $\overline{\phi 3}$, $\overline{\phi 4}$, and STB should be tied together, $\overline{DDEN}$ left open, and TG43 tied to ground.

In the double-density mode ($\overline{DDEN}$=0), the signals Early and Late are used to select a phase input ($\overline{\phi 1}$ – $\overline{\phi 4}$) on the leading edge of WDIN. The STB line is latched high when this occurs, causing the WD2143-01 to start its pulse generation. $\overline{\phi 2}$ is used as the write data pulse on nominal (Early=Late=$\overline{\phi}$), $\overline{\phi 2}$ is used for early, and $\overline{\phi 3}$ is used for late. The leading edge of $\overline{\phi 4}$ resets the STB line in anticipation of the next write data pulse. When TG43=0 or $\overline{DDEN}$=1, Precompensation is disabled and any transitions on the WDIN line will appear on the WDout line. If write precompensation is desired on all tracks, leave TG43 open (an internal pull-up will force a Logic I) while $\overline{DDEN}$=0.

The signals, $\overline{DDEN}$, TG43, and $\overline{RDD}$ have internal pull-up resistors and may be left open if a logic I is desired on any of these lines.

The minimum Voh level on PU is specified at 2.4V, sourcing 200ua. During PUMP UP time, this output will "drift" from a tri-state to .4V minimum. By tying PU and PD together, a PUMP signal is created that will be forced low for a decrease in VCO frequency and forced high for an increase in VCO frequency. To speed up rise times and stabilize the output voltage, a resistor divider can be used to set the tri-state level to approximately 1.4V. This yields a worst case swing of ± 1V; acceptable for most VCO chips with a linear voltage-to-frequency characteristic.

Both PU and $\overline{PD}$ signals are affected by the width of the RAW READ (RDD) pulse. The wider the RAW READ pulse, the longer the PU or $\overline{PD}$ signal (depending upon the phase relationship to RCLK) will remain active. If the RAW READ pulse exceeds 250ns, (VCO = 4MHz, DDEN = 0) or 500ns. (VCO = 4MHz, DDEN = 1), then both a PU and PD will occur in the same window. This is undesirable and reduces the accuracy of the external integrator or low-pass filter to convert the PUMP signals into a slow moving D.C. correction voltage.

Eventually, the PUMP signals will have corrected the VCO input to exactly the same frequency multiple as the RAW READ signal. The leading edge of the RAW READ pulse will then occur in the exact center of the RCLK window, and ideal condition for the FD179X internal recovery circuits.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature under Bias ..... −25° to 70°C
Voltage on any pin with respect to Ground (vss) ..... −0.2 to +7V
Power Dissipation 1W
Storage Temp.—Ceramic—65°C to +150°C
Plastic—55°C to +125°C

NOTE: Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical characteristics.

DC ELECTRICAL CHARACTERISTICS

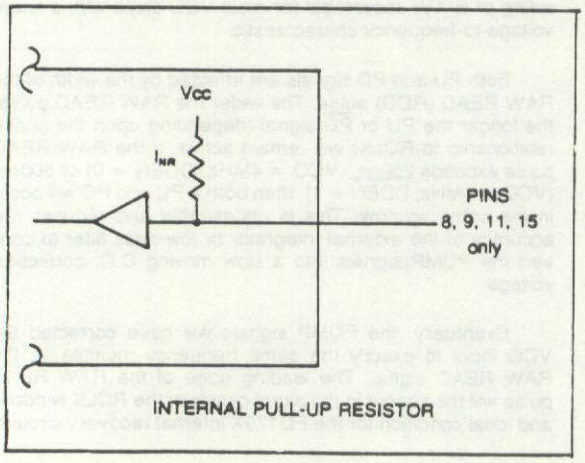
$T_A = \phi$ to 70°C; V_{CC} = 5.0V±10%; V_{ss}=OV

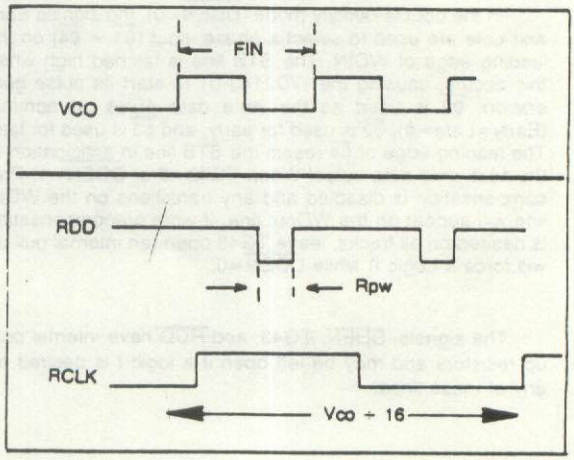
SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	−0.2		+0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL}=3.2MA
V_{OH}	High Level Output Voltage	2.4			V	I_{OH}=−200μa
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current		40	100	MA	All outputs open

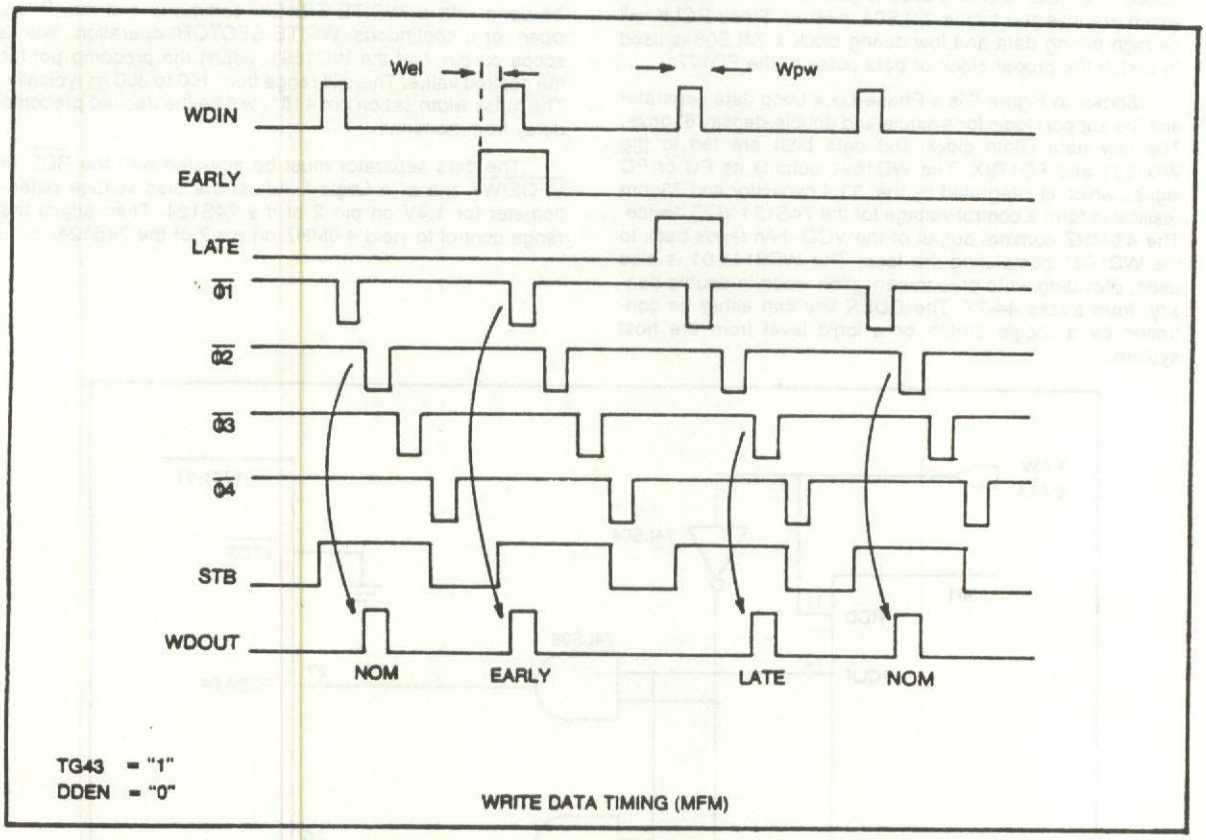
AC ELECTRICAL CHARACTERISTCS

T_A = 0° to 70°C; V_{cc} = 5V± 10%; Vss = OV

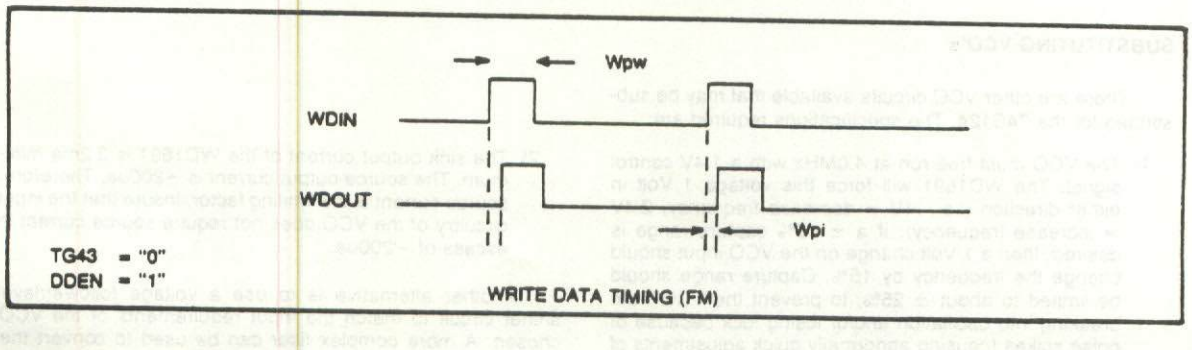
SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
FIN	VCO Input Frequency	.5	4	6	MHz	$\overline{DDEN}$=0
		.5	2	6	MHz	$\overline{DDEN}$=1
R_{pw}	$\overline{RDD}$ Pulse Width	100	200		ns.	
W_{el}	EARLY (LATE) to WDIN	100			ns.	
P_{on}	PUMP UP/DN Time	0		250	ns.	
W_{pi}	WDIN to WDOUT			80	ns.	$\overline{DDEN}$=1
I_{NR}	Internal Pull-up Resistor	4.0	6.5	10	KΩ	







WRITE DATA TIMING (MFM)



WRITE DATA TIMING (FM)

TYPICAL APPLICATIONS

Figure 1 illustrates the 1691 to FD1771-01 floppy disk controller. The RCLK signal is used to gate the RAW data pulses which are inverted by the 74LS04 inverter. Since RCLK will be high during data and low during clock a 74LS08 is used to switch the proper clock or data pulse to the FD1771.

Shown in Figure 2 is a Phase-Lock Loop data separator and the support logic for a single and double-density 8" drive. The raw data (Both clock and data bits) are fed to the WD1691 and FD179X. The WD1691 outputs its PU or PD signal, which is integrated by the .33uf capacitor and 33ohm resistor to form a control voltage for the 74S124 VCO device. The 4.0MHZ nominal output of the VCO then feeds back to the WD1691 completing the loop. The WD2143-01 is also used, providing write precompensation when in double-density, from tracks 44-77. The $\overline{\text{DDEN}}$ line can either be controlled by a toggle switch or a logic level from the host system.

To adjust write precompensation, issue a command to the FD179X so that write data pulses are present. This can be done with a 'WRITE TRACK' command and the IP line open, or a continuous 'WRITE SECTOR' operation. With a scope on pin 4 of the WD1691, adjust the precomp pot for the desired value. This will range from 100 to 300 ns typically. The pulse width set on pin 4 (ϕ1) will be the desired precomp delay from nominal.

The data separator must be adjusted with the $\overline{\text{RDD}}$ or $\overline{\text{VFOE}}$/WF line at a Logic I. Adjust the bias voltage potentiometer for 1.4V on pin 2 of the 74S124. Then adjust the range control to yield 4.0MHZ on pin 7 of the 74S124.

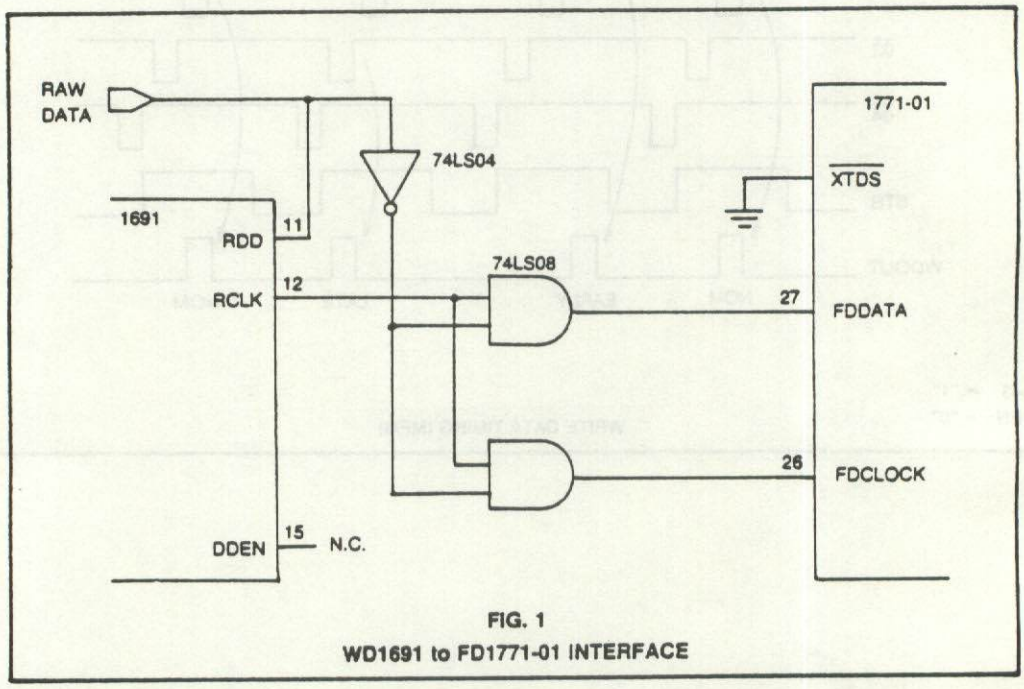


FIG. 1

WD1691 to FD1771-01 INTERFACE

SUBSTITUTING VCO's

There are other VCO circuits available that may be substituted for the 74S124. The specifications required are:

1) The VCO must free run at 4.0MHz with a 1.4V control signal. The WD1691 will force this voltage 1 Volt in either direction (i.e., .4V = decrease frequency, 2.4V = increase frequency). If a ± 15% capture range is desired, then a 1 Volt change on the VCO input should change the frequency by 15%. Capture range should be limited to about ± 25%, to prevent the VCO from breaking into oscillation and/or losing lock because of noise spikes (causing abnormally quick adjustments of the VCO frequency). Jitter in the VCO output frequency may further be reduced by increasing the integration capacitor/resistor, but this will also decrease the final capture range and lock-up time.

2) The sink output current of the WD1691 is 3.2ma minimum. The source output current is −200ua. Therefore, source current is the limiting factor. Insure that the input circuitry of the VCO does not require source current in excess of −200ua.

Another alternative is to use a voltage follower/level shifter circuit to match the input requirements of the VCO chosen. A more complex filter can be used to convert the PUMP UP/PUMP DOWN pulses to the varying DC voltage signal required by the VCO, achieving an optimum condition between lock-up time and high frequency rejection.

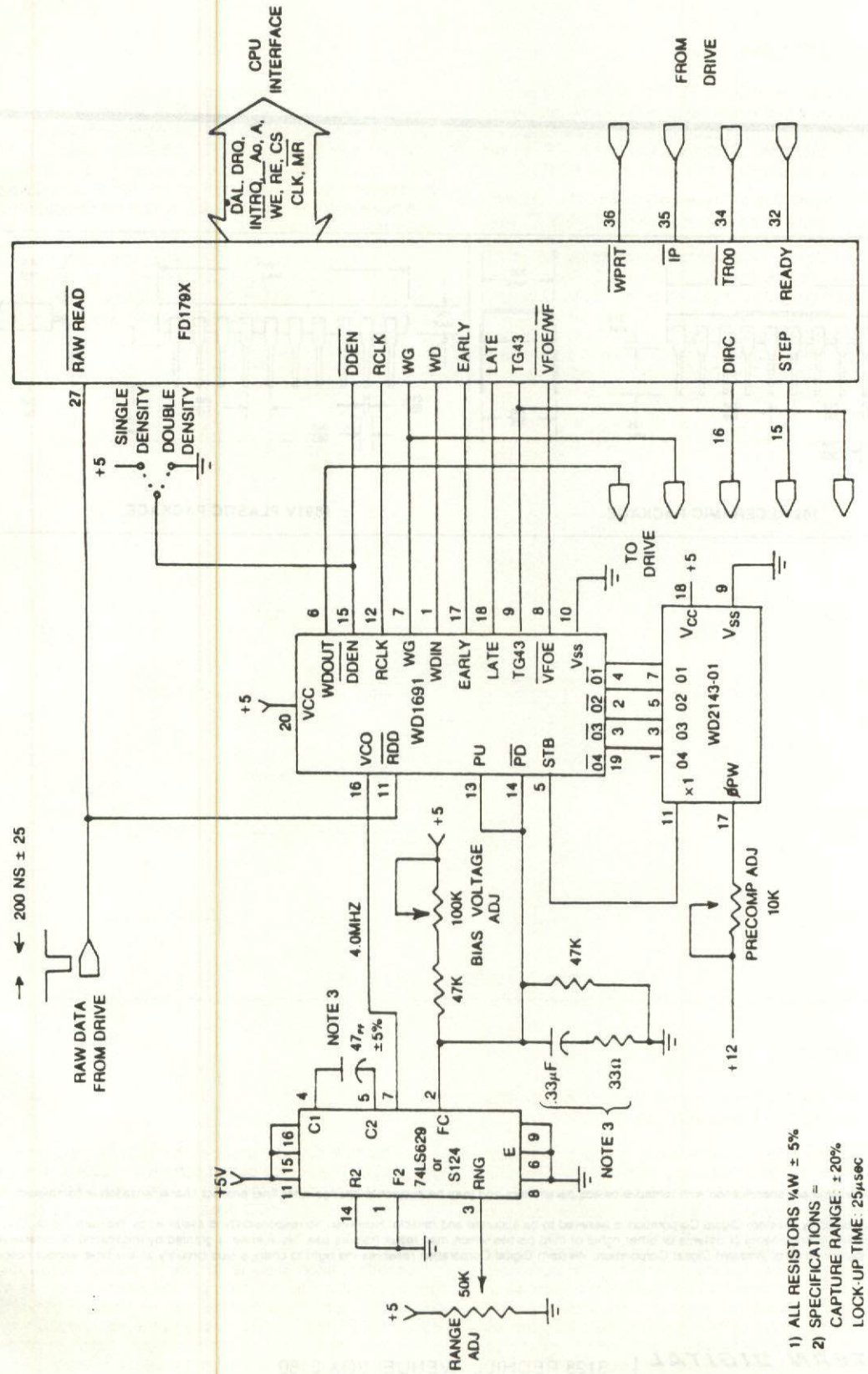
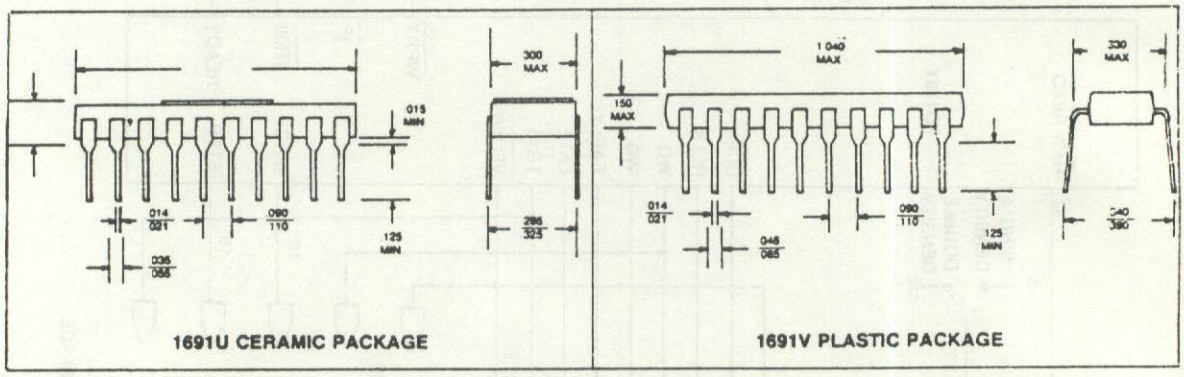


FIG. 2

8" SINGLE/DOUBLE DENSITY FLOPPY INTERFACE

1) ALL RESISTORS ¼W ± 5%
2) SPECIFICATIONS =
   CAPTURE RANGE: ± 20%
   LOCK-UP TIME: 25µsec
   (ALL ONE'S PATTERN, MFM)
3) FOR 5 1/4" 8"
   68µf 33µf
   680Ω 330Ω
   80PF 47PF



1691U CERAMIC PACKAGE

1691V PLASTIC PACKAGE

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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